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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323hap4008c">https://www.e-xfl.com/product-detail/zilog/zgp323hap4008c</a>



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**Table 6. 40- and 48-Pin Configuration (Continued)**

40-Pin PDIP #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V <sub>DD</sub>
31	24, 37, 38	V <sub>SS</sub>
25	29	Pref1/P30
	48	NC
	6	NC
	14	NC
	30	NC
	36	NC



**Table 11. GP323HA DC Characteristics (Continued)**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = -40°C to +125°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
V <sub>HVD</sub>	V <sub>CC</sub> High Voltage Detection			2.7		V		

**Notes:**

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V<sub>CC</sub> falls below V<sub>BO</sub> limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V<sub>CC</sub> and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

**Table 12. EPROM/OTP Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	100			Cycles	1

**Notes:**

1. For windowed cerdip package only.
2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

$$AF = \exp[(E_a/k) * (1/T_{use} - 1/T_{stress})]$$

Where:

E<sub>a</sub> is the intrinsic activation energy (eV; typ. 0.8)

k is Boltzman's constant (8.67 x 10<sup>-5</sup> eV/°K)

°K = -273.16°C

T<sub>use</sub> = Use Temperature in °K

T<sub>stress</sub> = Stress Temperature in °K

3. At a stable UV Lamp output of 20mW/CM<sup>2</sup>



### Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 22. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

- **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

### Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

## RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP asserts (Low) the RESET pin, the internal pull-up is disabled. The Z8 GP does not assert the RESET pin when under VBO.

- **Note:** The external Reset does not initiate an exit from STOP mode.

## Functional Description

This device incorporates special functions to enhance the Z8<sup>®</sup> functionality in consumer and battery-operated applications.

### Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

### RAM

This device features 256B of RAM. See Figure 14.



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

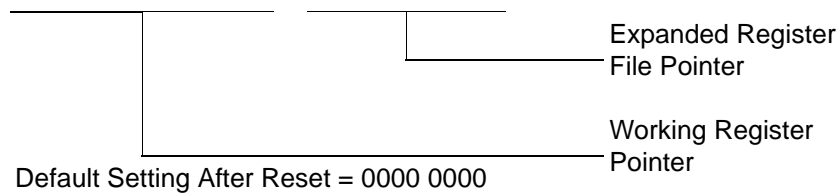
- **Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).



The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



**Figure 16. Register Pointer**

**Example: Z8 GP: (See Figure 15 on page 28)**

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTR0

R1 = CTR1

R2 = CTR2

R3 = Reserved



### T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16\_OUT is a 1; if it is a 1, T16\_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H \* 256 + TC16L is loaded, and T16\_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16\_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.

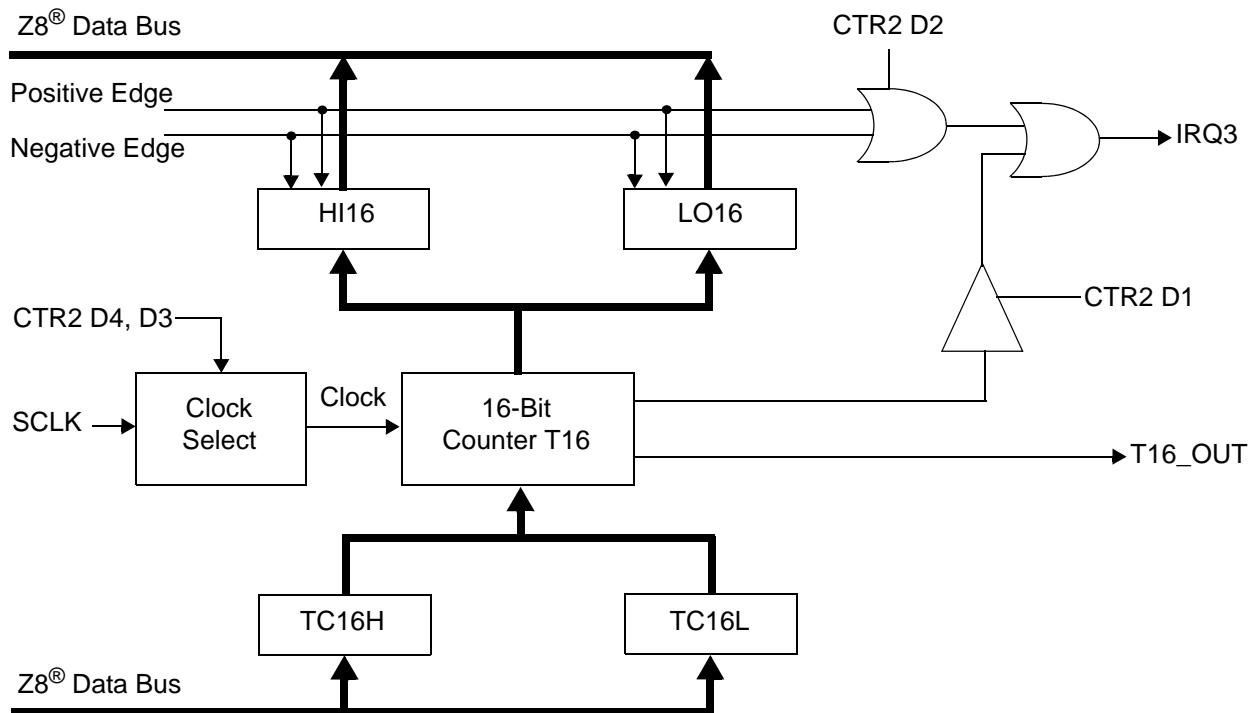


Figure 25. 16-Bit Counter/Timer Circuits

► **Note:** Global interrupts override this function as described in “Interrupts” on page 50.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H \* 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.



### **During PING-PONG Mode**

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

### **Interrupts**

The ZGP323H features six different interrupts (Table 19). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 19) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 59.

**Table 19. Interrupt Types, Sources, and Vectors**

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T <sub>IN</sub>	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All ZGP323H interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 20.

**Table 20. IRQ Register**

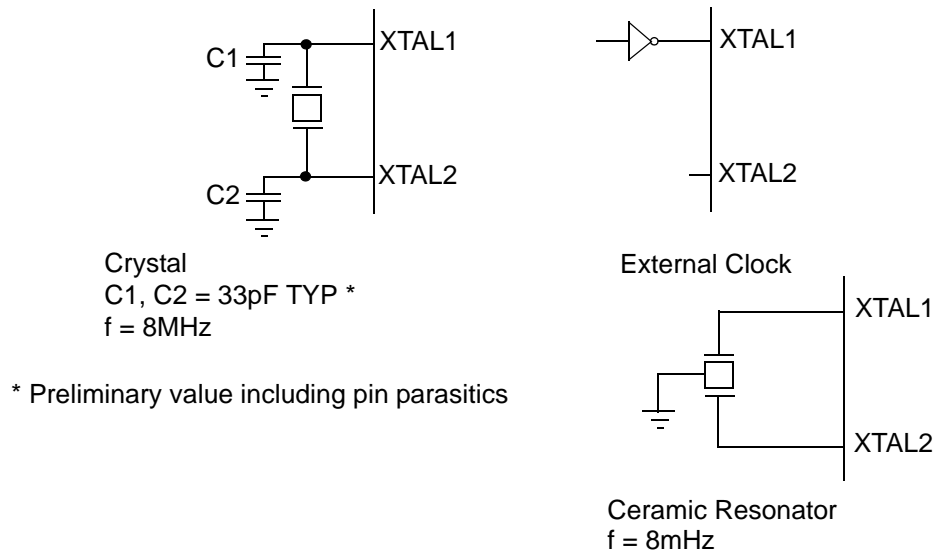
IRQ		Interrupt Edge	
D7	D6	IRQ2 (P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

**Note:** F = Falling Edge; R = Rising Edge

## Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal or ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100  $\Omega$ . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.



**Figure 31. Oscillator Configuration**



### Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows  $V_{DD}$  and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from  $V_{BO}$  Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

### HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

### STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10  $\mu$ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:

### Low-Voltage Detection Register—LVD(D)0Ch

- **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position	Description
LVD	76543---	Reserved No Effect
	----2--	R 1 HVD flag set 0* HVD flag reset
	-----1-	R 1 LVD flag set 0* LVD flag reset
	-----0	R/W 1 Enable VD 0* Disable VD

\*Default after POR

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the  $V_{CC}$  voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the  $V_{CC}$  level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if  $V_{CC}$  is higher than  $V_{HVD}$ . The LVD flag (bit 1 of the LVD register) is set only if  $V_{CC}$  is lower than the  $V_{LVD}$ . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

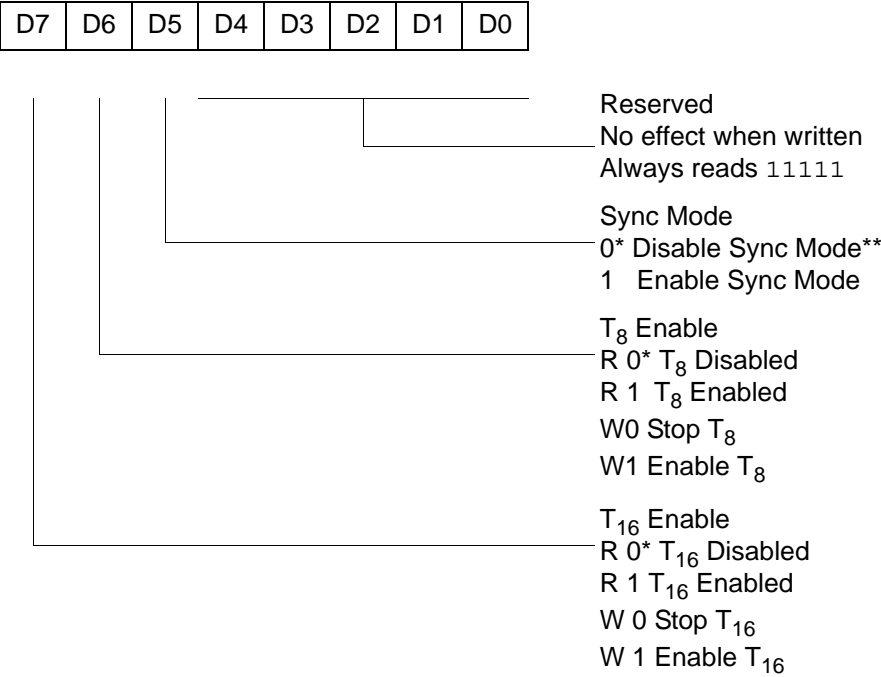


- **Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



CTR3(0D)03H



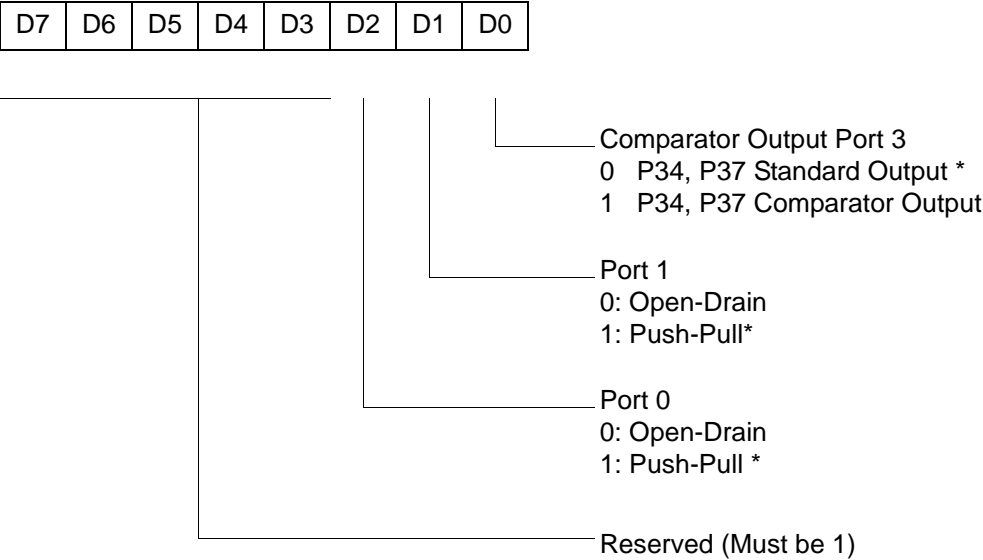
\* Default setting after reset.  
\*\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)





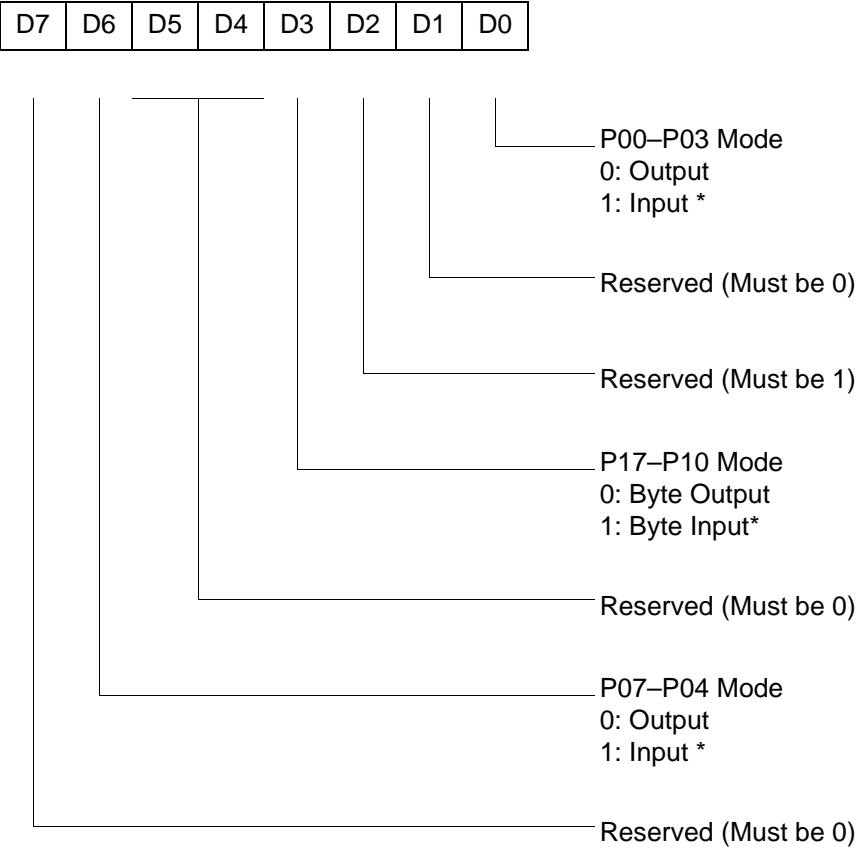
PCON(0F)00H



\* Default setting after reset

Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)

R248 P01M(F8H)



\* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)



R252 Flags(FCH)

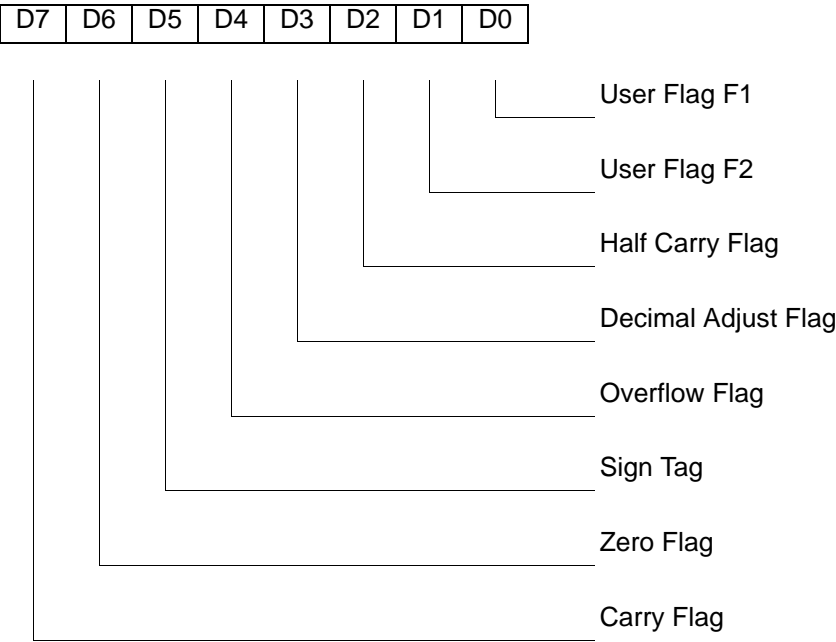
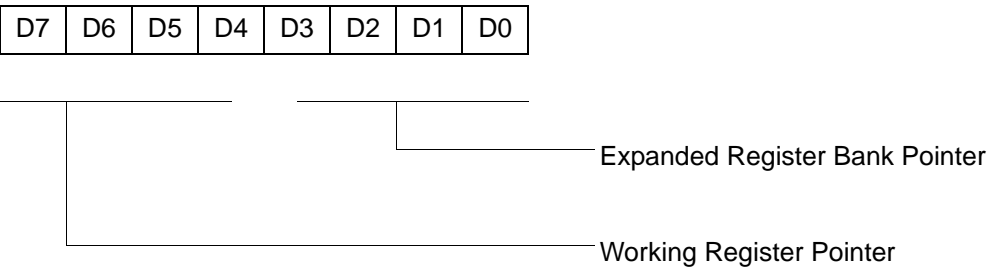


Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)



**4KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323HSH4804C	48-pin SSOP 4K OTP	ZGP323HSS2804C	28-pin SOIC 4K OTP
ZGP323HSP4004C	40-pin PDIP 4K OTP	ZGP323HSH2004C	20-pin SSOP 4K OTP
ZGP323HSH2804C	28-pin SSOP 4K OTP	ZGP323HSP2004C	20-pin PDIP 4K OTP
ZGP323HSP2804C	28-pin PDIP 4K OTP	ZGP323HSS2004C	20-pin SOIC 4K OTP

**4KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323HEH4804C	48-pin SSOP 4K OTP	ZGP323HES2804C	28-pin SOIC 4K OTP
ZGP323HEP4004C	40-pin PDIP 4K OTP	ZGP323HEH2004C	20-pin SSOP 4K OTP
ZGP323HEH2804C	28-pin SSOP 4K OTP	ZGP323HEP2004C	20-pin PDIP 4K OTP
ZGP323HEP2804C	28-pin PDIP 4K OTP	ZGP323HES2004C	20-pin SOIC 4K OTP

**4KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323HAH4804C	48-pin SSOP 4K OTP	ZGP323HAS2804C	28-pin SOIC 4K OTP
ZGP323HAP4004C	40-pin PDIP 4K OTP	ZGP323HAH2004C	20-pin SSOP 4K OTP
ZGP323HAH2804C	28-pin SSOP 4K OTP	ZGP323HAP2004C	20-pin PDIP 4K OTP
ZGP323HAP2804C	28-pin PDIP 4K OTP	ZGP323HAS2004C	20-pin SOIC 4K OTP

Replace C with G for Lead-Free Packaging

**Additional Components**

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM (For 3.6V Emulation only)	Emulator/programmer	ZGP32300100ZPR (Ethernet)	Programming system
		ZGP32300200ZPR (USB)	Programming system

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