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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	· ·
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hap4008g

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- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0-7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

General Description

The ZGP323H is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG[®]'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The ZGP323H architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8[®] offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

Note: All signals with an overline, "", are active Low. For example, B/W, in which WORD is active Low, and B/W, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 3.





Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.



	T ₄ =0°C to +70°C							
Symbol	Parameter	V _{CC}	Min	Typ(7)	Мах	Units	Conditions	Notes
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0V, V_{CC}$	
Icc	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I _{CC1}	Standby Current	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
	(HALT Mode)	3.6V		0.8	2.0	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I _{CC2}	Standby Current (Stop	2.0V		1.6	8	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
	Mode)	3.6V		1.8	10	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
		5.5V		1.9	12	μΑ	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
		2.0V		5	20	μΑ	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		3.6V		8	30	μΑ	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		5.5V		15	45	μΑ	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage			1.9	2.0	V	8MHz maximum	
20	Protection						Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage			2.4		V		
	Detection							
V _{HVD}	Vcc High Voltage			2.7		V		
	Detection							

Table 9. GP323HS DC Characteristics (Continued)

Notes:

1. All outputs unloaded, inputs at rail.

2. CL1 = CL2 = 100 pF.

3. Oscillator stopped.

4. Oscillator stops when V_{CC} falls below V_{BO} limit.

 It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VCC and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

- 6. Comparator and Timers are on. Interrupt disabled.
- 7. Typical values shown are at 25 degrees C.

Table 10. GP323HE DC Characteristics

T _A = -40°C to +105°C								
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} 0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	I _{OH} = -0.5mA	



Table 11. GP323HA DC Characteristics

T _A = -40°C to +125°C								
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} –0.3		0.4	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	I _{OH} = -0.5mA	
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V		
IIL	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled	
R _{PU}	Pull-up Resistance	2.0V	200		700	KΩ	V _{IN} = 0V; Pullups selected by mask	
		3.6V	50		300	KΩ	option	
		5.0V	25		175	KΩ	_	
I _{OL}	Output Leakage	2.0-5.5	-1		1	μΑ	$V_{IN} = 0V, V_{CC}$	
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I _{CC1}	Standby Current	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
	(HALI Mode)	3.6V		0.8	2.0	mA	$V_{IN} = 0V$, Clock at 8.0MHz	1, 2, 6
<u> </u>		5.5V		1.3	3.2	mA	$V_{IN} = 0V$, Clock at 8.0MHz	1, 2, 6
I _{CC2}	Standby Current (Stop	2.0V		1.6	15	μA	$V_{IN} = 0$ V, V_{CC} WDT not Running	3
	Mode)	3.6V		1.8	20	μA	$V_{IN} = 0$ V, V_{CC} WDT not Running	3
		5.5V		1.9	25	μΑ	$v_{IN} = 0$ V, v_{CC} WDT not Running	3
		2.00		о 0	30	μΑ	$v_{IN} = 0$ V, v_{CC} WDT is Running	ა ი
		3.0V 5.5V		0 15	40 60	μΑ	$v_{IN} = 0.0$, v_{CC} wDT is Running	ა ვ
	Chan allow Course at	5.57		10	00	μΑ	$V_{\rm IN} = 0.0$, $V_{\rm CC}$ with the Ruthing	3
	(Low Voltage)			1.2	0	μΑ		4
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V		



The counter/timers are mapped into ERF group D. Access is easily performed using the following:

LD	RP, #0Dh	;	Select ERF D
for access to bank D			
		;	(working
register group 0)			
LD	R0,#xx	;	load CTR0
LD	1, #xx	;	load CTR1
LD	R1, 2	;	CTR2→CTR1
LD	RP, #0Dh	;	Select ERF D
for access to bank D			
		;	(working
register group 0)			
LD	RP, #7Dh	;	Select
expanded register bank	D and working	;	register
group 7 of bank 0 for a	ccess.		
LD	71h, 2		
; CTRL2 \rightarrow register 71h			
LD	R1, 2		
; CTRL2→register 71h			

Register File

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The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 15) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.





In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 47.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03H

Table 18 lists and briefly describes the fields for this register. This register allows the T_8 and T_{16} counters to be synchronized.

Field	Bit Position		Value	Description
T ₁₆ Enable	7	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T ₈ Enable	-6	R	0*	Counter Disabled
-		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	5	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode

Table 18. CTR3 (D)03H: T8/T16 Control Register







Figure 19. Transmit Mode Flowchart



into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFH (see Figure 23 and Figure 24).



Figure 23. Demodulation Mode Count Capture Flowchart



T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.



Figure 25. 16-Bit Counter/Timer Circuits

Note: Global interrupts override this function as described in "Interrupts" on page 50.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.



If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

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Note: Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.



During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Interrupts

The ZGP323H features six different interrupts (Table 19). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 19) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 59.



Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal or ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.



f = 8mHz

Figure 31. Oscillator Configuration



SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

* * Default setting after Reset and Stop Mode Recovery

* * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.



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Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8[®] CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



* Default setting after reset

Figure 37. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 23.









Figure 58. 20-Pin CDIP Package





Figure 59. 20-Pin PDIP Package Diagram





CONTROLLING DIMENSIONS : INCH













Figure 63. 28-Pin CDIP Package Diagram



SVMBOI	OPT #	MILLIN	IETER	INCH		
SIMDOL			MAX	MIN	MAX	
A1		0.38	1.02	.015	.040	
A2		3.18	4.19	.125	.165	
В		0.38	0.53	.015	.021	
D1	01	1.40	1.65	.055	.065	
	02	1.14	1.40	.045	.055	
С		0.23	0.38	.009	.015	
п	01	36.58	37.34	1.440	1.470	
	02	35.31	35.94	1.390	1.415	
E		15.24	15.75	.600	.620	
E1	01	13.59	14.10	.535	.555	
	02	12.83	13.08	.505	.515	
e		2.54	TYP	.100 BSC		
eA		15.49	16.76	.610	.660	
L		3.05	3.81	.120	.150	
01	01	1.40	1.91	.055	.075	
	02	1.40	1.78	.055	.070	
•	01	1.52	2.29	.060	.090	
5	02	1.02	1.52	.040	.060	

CONTROLLING DIMENSIONS : INCH



01

02

STANDARD

Figure 64. 28-Pin PDIP Package Diagram







Figure 68. 48-Pin SSOP Package Design

Note: Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.



Example



ZGP323H Z8[®] OTP Microcontroller with IR Timers



28-pin DIP/SOIC/SSOP 6 40- and 48-pin 8 40-pin DIP 7 48-pin SSOP 8 pin functions port 0 (P07 - P00) 18 port 0 (P17 - P10) 19 port 0 configuration 19 port 1 configuration 20 port 2 (P27 - P20) 20 port 2 (P37 - P30) 21 port 2 configuration 21 port 3 configuration 22 port 3 counter/timer configuration 24 reset) 25 XTAL1 (time-based input 18 XTAL2 (time-based output) 18 ping-pong mode 48 port 0 configuration 19 port 0 pin function 18 port 1 configuration 20 port 1 pin function 19 port 2 configuration 21 port 2 pin function 20 port 3 configuration 22 port 3 pin function 21 port 3counter/timer configuration 24 port configuration register 55 power connections 3 power supply 5 program memory 25 map 26 R ratings, absolute maximum 10 register 61 CTR(D)01h 35 CTR0(D)00h 33 CTR2(D)02h 37 CTR3(D)03h 39 flag 80 HI16(D)09h 32

HI8(D)0Bh 32 interrupt priority 78 interrupt request 79 interruptmask 79 L016(D)08h 32 L08(D)0Ah 32 LVD(D)0Ch 65 pointer 80 port 0 and 1 77 port 2 configuration 75 port 3 mode 76 port configuration 55, 75 SMR2(F)0Dh 40 stack pointer high 81 stack pointer low 81 stop mode recovery 57 stop mode recovery 2 61 stop-mode recovery 73 stop-mode recovery 274 T16 control 69 T8 and T16 common control functions 67 T8/T16 control 70 TC16H(D)07h 32 TC16L(D)06h 33 TC8 control 66 TC8H(D)05h 33 TC8L(D)04h 33 voltage detection 71 watch-dog timer 75 register description Counter/Timer2 LS-Byte Hold 33 Counter/Timer2 MS-Byte Hold 32 Counter/Timer8 Control 33 Counter/Timer8 High Hold 33 Counter/Timer8 Low Hold 33 CTR2 Counter/Timer 16 Control 37 CTR3 T8/T16 Control 39 Stop Mode Recovery2 40 T16 Capture LO 32 T8 and T16 Common functions 35 T8_Capture_HI 32