



Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |   |
|----------------------------|---|
| Product Status             | Obsolete  |
| Core Processor             | Z8  |
| Core Size                  | 8-Bit   |
| Speed                      | 8MHz  |
| Connectivity               | -   |
| Peripherals                | HLVD, POR, WDT  |
| Number of I/O              | 16  |
| Program Memory Size        | 8KB (8K x 8)  |
| Program Memory Type        | OTP   |
| EEPROM Size                | -   |
| RAM Size                   | 237 x 8   |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V   |
| Data Converters            | -   |
| Oscillator Type            | Internal  |
| Operating Temperature      | -40°C ~ 125°C (TA)  |
| Mounting Type              | Surface Mount   |
| Package / Case             | 20-SOIC (0.295", 7.50mm Width)  |
| Supplier Device Package    | -   |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/zilog/zgp323has2008c00tr">https://www.e-xfl.com/product-detail/zilog/zgp323has2008c00tr</a> |



This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

**ZiLOG Worldwide Headquarters**

532 Race Street  
San Jose, CA 95126-3432  
Telephone: 408.558.8500  
Fax: 408.558.8300  
[www.zilog.com](http://www.zilog.com)

ZiLOG is a registered trademark of ZiLOG Inc. in the United States and in other countries. All other products and/or service names mentioned herein may be trademarks of the companies with which they are associated.

**Document Disclaimer**

©2005 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZiLOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Devices sold by ZiLOG, Inc. are covered by warranty and limitation of liability provisions appearing in the ZiLOG, Inc. Terms and Conditions of Sale. ZiLOG, Inc. makes no warranty of merchantability or fitness for any purpose. Except with the express written approval of ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.



# Table of Contents

|   |     |
|---|-----|
| Revision History . . . . .                              | iii |
| Development Features . . . . .                          | 1   |
| General Description . . . . .                           | 2   |
| Pin Description . . . . .                               | 4   |
| Absolute Maximum Ratings . . . . .                      | 10  |
| Standard Test Conditions . . . . .                      | 10  |
| DC Characteristics . . . . .                            | 11  |
| AC Characteristics . . . . .                            | 16  |
| Pin Functions . . . . .                                 | 18  |
| XTAL1 Crystal 1 (Time-Based Input) . . . . .            | 18  |
| XTAL2 Crystal 2 (Time-Based Output) . . . . .           | 18  |
| Port 0 (P07–P00) . . . . .                              | 18  |
| Port 1 (P17–P10) . . . . .                              | 19  |
| Port 2 (P27–P20) . . . . .                              | 20  |
| Port 3 (P37–P30) . . . . .                              | 21  |
| RESET (Input, Active Low) . . . . .                     | 25  |
| Functional Description . . . . .                        | 25  |
| Program Memory . . . . .                                | 25  |
| RAM . . . . .   | 25  |
| Expanded Register File . . . . .                        | 26  |
| Register File . . . . .                                 | 30  |
| Stack . . . . .   | 31  |
| Timers . . . . .  | 32  |
| Counter/Timer Functional Blocks . . . . .               | 40  |
| Expanded Register File Control Registers (0D) . . . . . | 66  |
| Expanded Register File Control Registers (0F) . . . . . | 71  |
| Standard Control Registers . . . . .                    | 75  |
| Package Information . . . . .                           | 81  |
| Ordering Information . . . . .                          | 90  |



# ***List of Tables***

|           |  |     |
|-----------|--|-----|
| Table 1.  | Revision History of this Document . . . . .              | iii |
| Table 2.  | Features . . . . .                                       | 1   |
| Table 3.  | Power Connections . . . . .                              | 3   |
| Table 4.  | 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification . . . . . | 5   |
| Table 5.  | 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification . . . . . | 6   |
| Table 6.  | 40- and 48-Pin Configuration . . . . .                   | 8   |
| Table 7.  | Absolute Maximum Ratings . . . . .                       | 10  |
| Table 8.  | Capacitance . . . . .                                    | 11  |
| Table 9.  | GP323HS DC Characteristics . . . . .                     | 11  |
| Table 10. | GP323HE DC Characteristics . . . . .                     | 12  |
| Table 11. | GP323HA DC Characteristics . . . . .                     | 14  |
| Table 12. | EPROM/OTP Characteristics . . . . .                      | 15  |
| Table 13. | AC Characteristics . . . . .                             | 17  |
| Table 14. | Port 3 Pin Function Summary. . . . .                     | 23  |
| Table 15. | CTR1(0D)01H T8 and T16 Common Functions . . . . .        | 35  |
| Table 16. | Interrupt Types, Sources, and Vectors . . . . .          | 52  |
| Table 17. | IRQ Register. . . . .                                    | 52  |
| Table 18. | SMR2(F)0DH:Stop Mode Recovery Register 2* . . . . .      | 58  |
| Table 19. | Stop Mode Recovery Source . . . . .                      | 60  |
| Table 20. | Watch-Dog Timer Time Select . . . . .                    | 63  |
| Table 21. | EPROM Selectable Options . . . . .                       | 64  |



**Table 11. GP323HA DC Characteristics (Continued)**

| Symbol           | Parameter                              | V <sub>CC</sub> | T <sub>A</sub> = -40°C to +125°C |        |     | Units | Conditions | Notes |
|------------------|--|-----------------|----------------------------------|--------|-----|-------|------------|-------|
|                  |  |                 | Min                              | Typ(7) | Max |       |            |       |
| V <sub>HVD</sub> | V <sub>CC</sub> High Voltage Detection |                 |                                  | 2.7    |     | V     |            |       |

**Notes:**

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V<sub>CC</sub> falls below V<sub>BO</sub> limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V<sub>CC</sub> and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

**Table 12. EPROM/OTP Characteristics**

| Symbol | Parameter                  | Min. | Typ. | Max. | Unit    | Notes |
|--------|----------------------------|------|------|------|---------|-------|
|        | Erase Time                 | 15   |      |      | Minutes | 1,3   |
|        | Data Retention @ use years |      | 10   |      | Years   | 2     |
|        | Program/Erase Endurance    | 100  |      |      | Cycles  | 1     |

**Notes:**

1. For windowed cerdip package only.
2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

$$AF = \exp[(E_a/k) * (1/T_{use} - 1/T_{stress})]$$

Where:

E<sub>a</sub> is the intrinsic activation energy (eV; typ. 0.8)

k is Boltzman's constant (8.67 x 10<sup>-5</sup> eV/°K)

°K = -273.16°C

T<sub>use</sub> = Use Temperature in °K

T<sub>stress</sub> = Stress Temperature in °K

3. At a stable UV Lamp output of 20mW/CM<sup>2</sup>



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

- **Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).

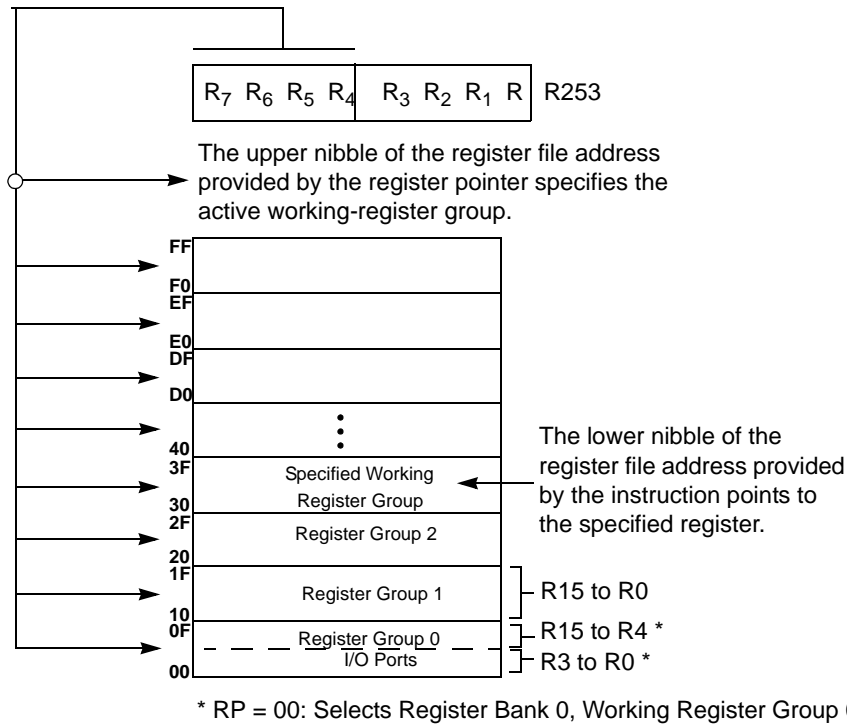


Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

### If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from `FFFFh`. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

### Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8\_OUT is set to this initial value (CTR1, D1). According to T8\_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16\_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

- **Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.



**Table 19. Interrupt Types, Sources, and Vectors**

| Name | Source               | Vector Location | Comments                                       |
|------|----------------------|-----------------|--|
| IRQ0 | P32                  | 0,1             | External (P32), Rising, Falling Edge Triggered |
| IRQ1 | P33                  | 2,3             | External (P33), Falling Edge Triggered         |
| IRQ2 | P31, T <sub>IN</sub> | 4,5             | External (P31), Rising, Falling Edge Triggered |
| IRQ3 | T16                  | 6,7             | Internal                                       |
| IRQ4 | T8                   | 8,9             | Internal                                       |
| IRQ5 | LVD                  | 10,11           | Internal                                       |

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All ZGP323H interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 20.

**Table 20. IRQ Register**

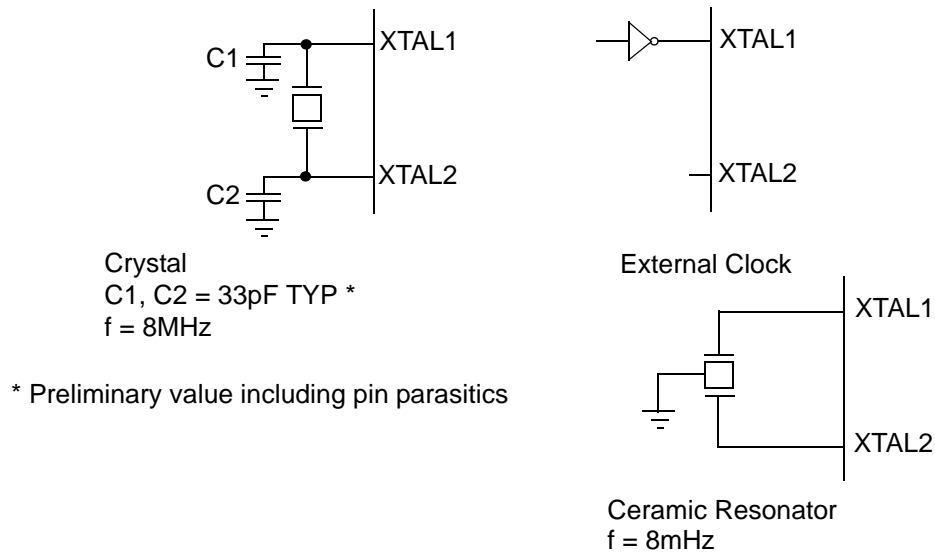
| IRQ |    | Interrupt Edge |            |
|-----|----|----------------|------------|
| D7  | D6 | IRQ2 (P31)     | IRQ0 (P32) |
| 0   | 0  | F              | F          |
| 0   | 1  | F              | R          |
| 1   | 0  | R              | F          |
| 1   | 1  | R/F            | R/F        |

**Note:** F = Falling Edge; R = Rising Edge

## Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal or ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100  $\Omega$ . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.



**Figure 31. Oscillator Configuration**

Table 22. Stop Mode Recovery Source

| SMR:432 |    |    | Operation                          |
|---------|----|----|------------------------------------|
| D4      | D3 | D2 | Description of Action              |
| 0       | 0  | 0  | POR and/or external reset recovery |
| 0       | 0  | 1  | Reserved                           |
| 0       | 1  | 0  | P31 transition                     |
| 0       | 1  | 1  | P32 transition                     |
| 1       | 0  | 0  | P33 transition                     |
| 1       | 0  | 1  | P27 transition                     |
| 1       | 1  | 0  | Logical NOR of P20 through P23     |
| 1       | 1  | 1  | Logical NOR of P20 through P27     |

- **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 61 for other recover sources.

#### Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the  $T_{POR}$  delay after Stop Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop Mode Recovery source must be kept active for at least 5  $T_{pC}$ .

- **Note:** This bit must be set to 1 if using a crystal or resonator clock source. The  $T_{POR}$  delay allows the clock source to stabilize before executing instructions.

#### Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

#### Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

### EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

**Table 24. EPROM Selectable Options**

|                                   |        |
|-----------------------------------|--------|
| Port 00–03 Pull-Ups               | On/Off |
| Port 04–07 Pull-Ups               | On/Off |
| Port 10–13 Pull-Ups               | On/Off |
| Port 14–17 Pull-Ups               | On/Off |
| Port 20–27 Pull-Ups               | On/Off |
| EPROM Protection                  | On/Off |
| Watch-Dog Timer at Power-On Reset | On/Off |

### Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the  $V_{DD}$  is at the required level for correct operation of the device. Reset is globally driven when  $V_{DD}$  falls below  $V_{BO}$ . A small drop in  $V_{DD}$  causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the  $V_{DD}$  is allowed to stay above  $V_{RAM}$ , the RAM content is preserved. When the power level is returned to above  $V_{BO}$ , the device performs a POR and functions normally.

**Low-Voltage Detection Register—LVD(D)0Ch**

- **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

| Field | Bit Position | Description           |         |                                |
|-------|--------------|-----------------------|---------|--------------------------------|
| LVD   | 76543---     | Reserved<br>No Effect |         |                                |
|       | ----2--      | R                     | 1<br>0* | HVD flag set<br>HVD flag reset |
|       | -----1-      | R                     | 1<br>0* | LVD flag set<br>LVD flag reset |
|       | -----0       | R/W                   | 1<br>0* | Enable VD<br>Disable VD        |

\*Default after POR

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

**Voltage Detection and Flags**

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the  $V_{CC}$  voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the  $V_{CC}$  level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if  $V_{CC}$  is higher than  $V_{HVD}$ . The LVD flag (bit 1 of the LVD register) is set only if  $V_{CC}$  is lower than the  $V_{LVD}$ . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.



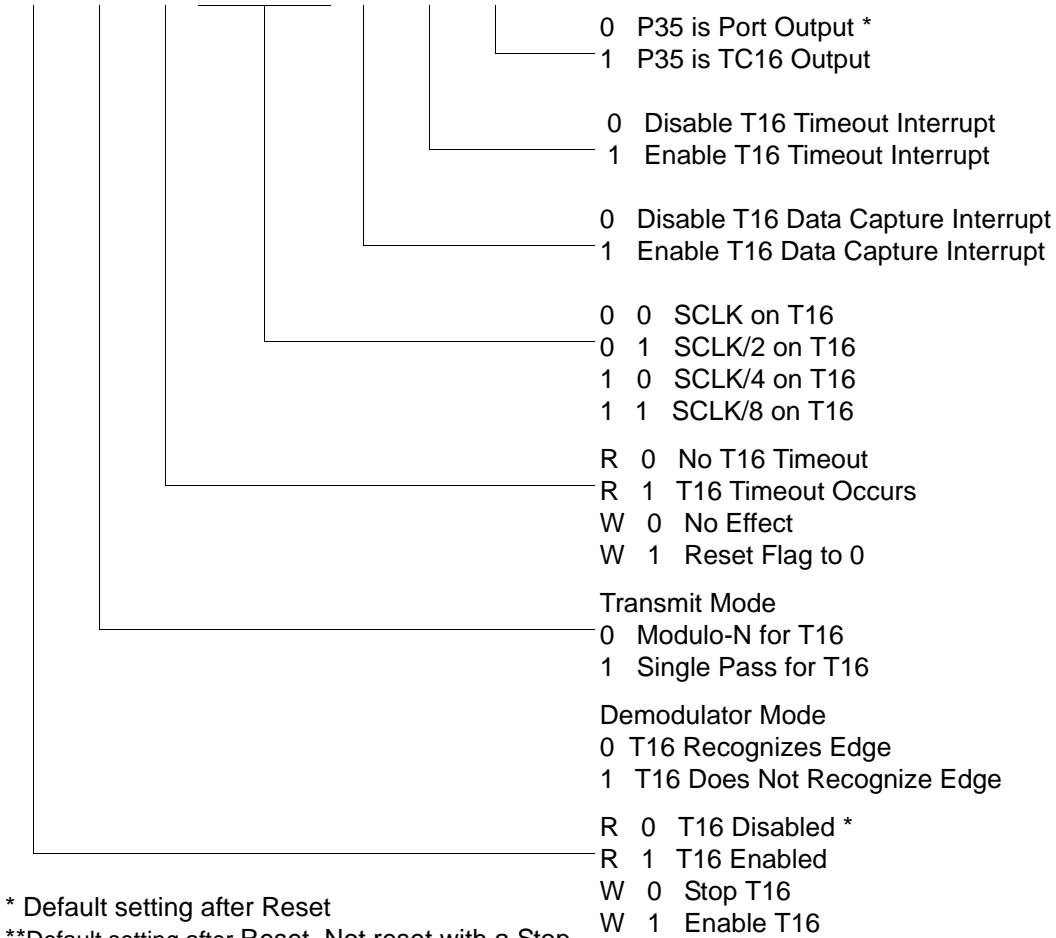
- **Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



CTR2(0D)02H

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|



\* Default setting after Reset  
\*\*Default setting after Reset. Not reset with a Stop-Mode recovery.

Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)

R250 IRQ(FAH)

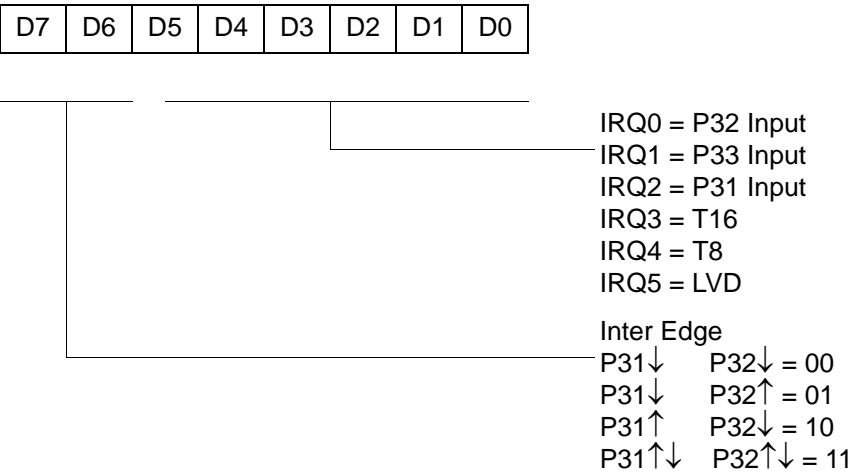


Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



\* Default setting after reset  
\* \* Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)



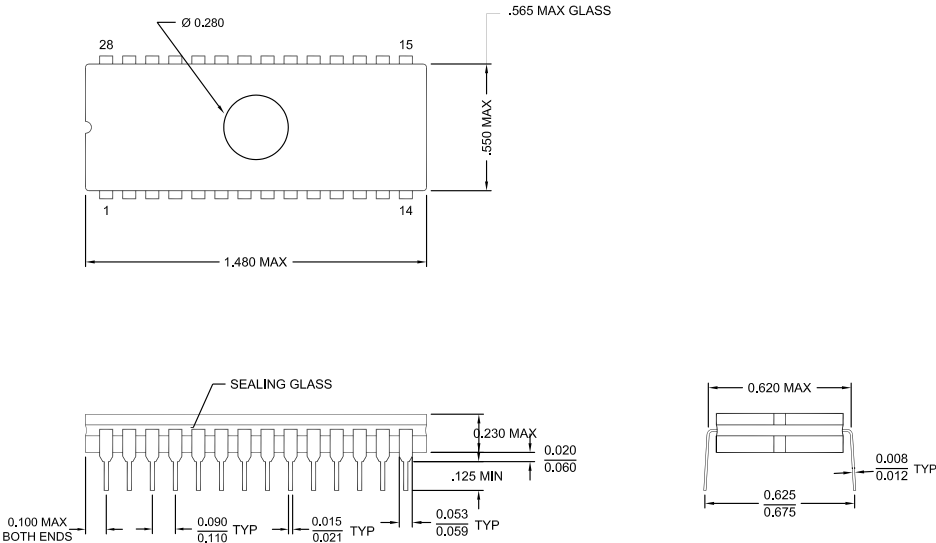
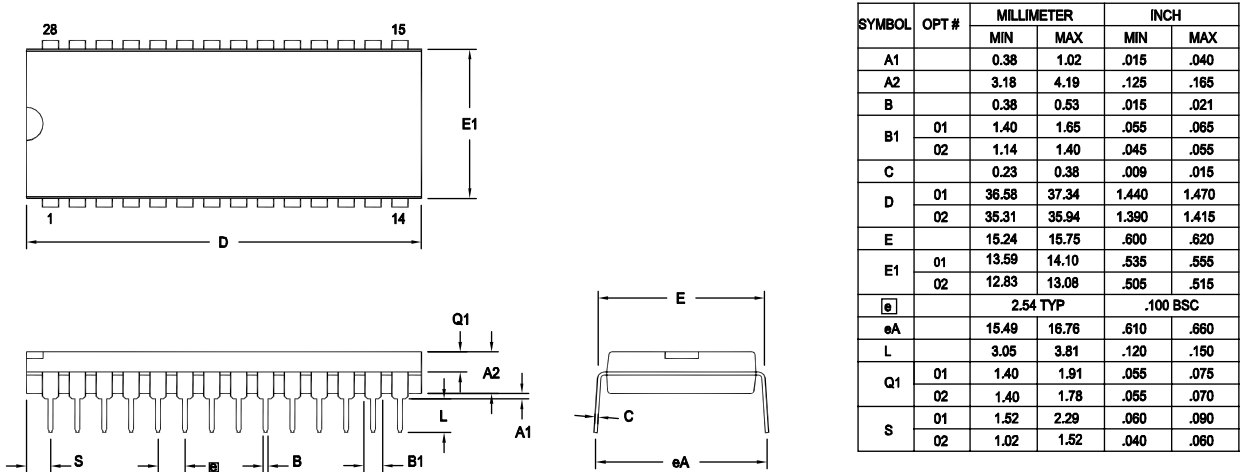


Figure 63. 28-Pin CDIP Package Diagram



CONTROLLING DIMENSIONS : INCH

| OPTION TABLE |          |
|--------------|----------|
| OPTION #     | PACKAGE  |
| 01           | STANDARD |
| 02           | IDF      |

Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 64. 28-Pin PDIP Package Diagram



## Ordering Information

### 32KB Standard Temperature: 0° to +70°C

| Part Number    | Description         | Part Number    | Description         |
|----------------|---------------------|----------------|---------------------|
| ZGP323HSH4832C | 48-pin SSOP 32K OTP | ZGP323HSS2832C | 28-pin SOIC 32K OTP |
| ZGP323HSP4032C | 40-pin PDIP 32K OTP | ZGP323HSH2032C | 20-pin SSOP 32K OTP |
| ZGP323HSK2832E | 28-pin CDIP 32K OTP | ZGP323HSK2032E | 20-pin CDIP 32K OTP |
| ZGP323HSK4032E | 40-pin CDIP 32K OTP | ZGP323HSP2032C | 20-pin PDIP 32K OTP |
| ZGP323HSH2832C | 28-pin SSOP 32K OTP | ZGP323HSS2032C | 20-pin SOIC 32K OTP |
| ZGP323HSP2832C | 28-pin PDIP 32K OTP |                |                     |

### 32KB Extended Temperature: -40° to +105°C

| Part Number    | Description         | Part Number    | Description         |
|----------------|---------------------|----------------|---------------------|
| ZGP323HEH4832C | 48-pin SSOP 32K OTP | ZGP323HES2832C | 28-pin SOIC 32K OTP |
| ZGP323HEP4032C | 40-pin PDIP 32K OTP | ZGP323HEH2032C | 20-pin SSOP 32K OTP |
| ZGP323HEH2832C | 28-pin SSOP 32K OTP | ZGP323HEP2032C | 20-pin PDIP 32K OTP |
| ZGP323HEP2832C | 28-pin PDIP 32K OTP | ZGP323HES2032C | 20-pin SOIC 32K OTP |

### 32KB Automotive Temperature: -40° to +125°C

| Part Number    | Description         | Part Number    | Description         |
|----------------|---------------------|----------------|---------------------|
| ZGP323HAH4832C | 48-pin SSOP 32K OTP | ZGP323HAS2832C | 28-pin SOIC 32K OTP |
| ZGP323HAP4032C | 40-pin PDIP 32K OTP | ZGP323HAH2032C | 20-pin SSOP 32K OTP |
| ZGP323HAH2832C | 28-pin SSOP 32K OTP | ZGP323HAP2032C | 20-pin PDIP 32K OTP |
| ZGP323HAP2832C | 28-pin PDIP 32K OTP | ZGP323HAS2032C | 20-pin SOIC 32K OTP |

Replace C with G for Lead-Free Packaging

- Numerics
  - 16-bit counter/timer circuits 46
  - 20-pin DIP package diagram 82
  - 20-pin SSOP package diagram 84
  - 28-pin DIP package diagram 86
  - 28-pin SOIC package diagram 85
  - 28-pin SSOP package diagram 87
  - 40-pin DIP package diagram 87
  - 48-pin SSOP package diagram 89
  - 8-bit counter/timer circuits 42
- A
  - absolute maximum ratings 10
- AC
  - characteristics 16
  - timing diagram 16
- address spaces, basic 2
- architecture 2
  - expanded register file 28
- B
  - basic address spaces 2
- block diagram, ZLP32300 functional 3
- C
  - capacitance 11
  - characteristics
    - AC 16
    - DC 11
  - clock 53
  - comparator inputs/outputs 25
  - configuration
    - port 0 19
    - port 1 20
    - port 2 21
    - port 3 22
    - port 3 counter/timer 24
  - counter/timer
    - 16-bit circuits 46
    - 8-bit circuits 42
    - brown-out voltage/standby 64
    - clock 53
    - demodulation mode count capture flow-  
chart 44
    - demodulation mode flowchart 45
    - EPROM selectable options 64
    - glitch filter circuitry 40
    - halt instruction 54
    - input circuit 40
    - interrupt block diagram 51
    - interrupt types, sources and vectors 52
    - oscillator configuration 53
    - output circuit 49
    - ping-pong mode 48
    - port configuration register 55
    - resets and WDT 63
    - SCLK circuit 58
    - stop instruction 54
    - stop mode recovery register 57
    - stop mode recovery register 2 61
    - stop mode recovery source 59
    - T16 demodulation mode 47
    - T16 transmit mode 46
    - T16\_OUT in modulo-N mode 47
    - T16\_OUT in single-pass mode 47
    - T8 demodulation mode 43
    - T8 transmit mode 40
    - T8\_OUT in modulo-N mode 43
    - T8\_OUT in single-pass mode 43
    - transmit mode flowchart 41
    - voltage detection and flags 65
    - watch-dog timer mode register 62
    - watch-dog timer time select 63
  - CTR(D)01h T8 and T16 Common Functions 35
- D
  - DC characteristics 11
- demodulation mode
  - count capture flowchart 44
  - flowchart 45
  - T16 47
  - T8 43
- description
  - functional 25
  - general 2

- pin 4
- E
- EPROM
  - selectable options 64
- expanded register file 26
- expanded register file architecture 28
- expanded register file control registers 71
  - flag 80
  - interrupt mask register 79
  - interrupt priority register 78
  - interrupt request register 79
  - port 0 and 1 mode register 77
  - port 2 configuration register 75
  - port 3 mode register 76
  - port configuration register 75
  - register pointer 80
  - stack pointer high register 81
  - stack pointer low register 81
  - stop-mode recovery register 73
  - stop-mode recovery register 2 74
  - T16 control register 69
  - T8 and T16 common control functions register 67
  - T8/T16 control register 70
  - TC8 control register 66
  - watch-dog timer register 75
- F
- features
  - standby modes 1
- functional description
  - counter/timer functional blocks 40
  - CTR(D)01h register 35
  - CTR0(D)00h register 33
  - CTR2(D)02h register 37
  - CTR3(D)03h register 39
  - expanded register file 26
  - expanded register file architecture 28
  - HI16(D)09h register 32
  - HI8(D)0Bh register 32
  - L08(D)0Ah register 32
  - L0I6(D)08h register 32
  - program memory map 26
  - RAM 25
  - register description 65
  - register file 30
  - register pointer 29
  - register pointer detail 31
  - SMR2(F)0D1h register 40
  - stack 31
  - TC16H(D)07h register 32
  - TC16L(D)06h register 33
  - TC8H(D)05h register 33
  - TC8L(D)04h register 33
- G
- glitch filter circuitry 40
- H
- halt instruction, counter/timer 54
- I
- input circuit 40
- interrupt block diagram, counter/timer 51
- interrupt types, sources and vectors 52
- L
- low-voltage detection register 65
- M
- memory, program 25
- modulo-N mode
  - T16\_OUT 47
  - T8\_OUT 43
- O
- oscillator configuration 53
- output circuit, counter/timer 49
- P
- package information
  - 20-pin DIP package diagram 82
  - 20-pin SSOP package diagram 84
  - 28-pin DIP package diagram 86
  - 28-pin SOIC package diagram 85
  - 28-pin SSOP package diagram 87
  - 40-pin DIP package diagram 87
  - 48-pin SSOP package diagram 89
- pin configuration
  - 20-pin DIP/SOIC/SSOP 5



- T8\_Capture\_LO 32
- register file 30
  - expanded 26
- register pointer 29
  - detail 31
- reset pin function 25
- resets and WDT 63
- S
- SCLK circuit 58
- single-pass mode
  - T16\_OUT 47
  - T8\_OUT 43
- stack 31
- standard test conditions 10
- standby modes 1
- stop instruction, counter/timer 54
- stop mode recovery
  - 2 register 61
  - source 59
- stop mode recovery 2 61
- stop mode recovery register 57
- T
- T16 transmit mode 46
- T16\_Capture\_HI 32
- T8 transmit mode 40
- T8\_Capture\_HI 32
- test conditions, standard 10
- test load diagram 10
- timing diagram, AC 16
- transmit mode flowchart 41
- V
- VCC 5
- voltage
  - brown-out/standby 64
  - detection and flags 65
- voltage detection register 71
- W
- watch-dog timer
  - mode registerwatch-dog timer mode regis-  
ter 62
  - time select 63
- X
- XTAL1 5
- XTAL1 pin function 18
- XTAL2 5
- XTAL2 pin function 18