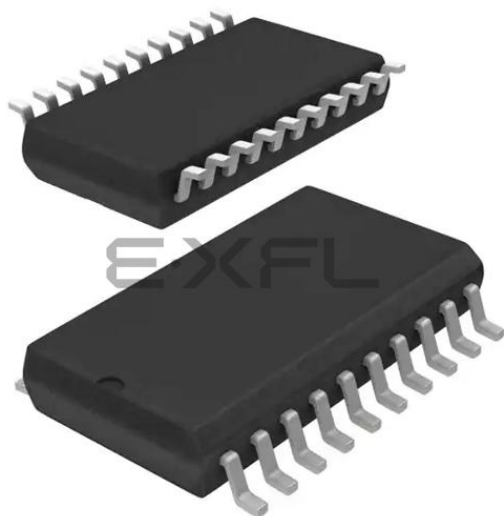




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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323has2032c00tr



Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Document

Date	Revision Level	Section	Description	Page #
December 2004	02		Changed low power consumption, STOP and HALT mode current values, deleted mask option note, clarified temperature ranges in Tables 6 and 8 and 10. Added new Tables 9 and 10. Also added Characterization data to Table 11 and changed Program/Erase Endurance value in Table 12.	1,2,10 11,12, 13,14, 15
			Removed Preliminary designation	All
March 2005	03		Minor change to Table 9 Electrical Characteristics. Added 20, 28 and 40-pin CDIP parts in the Ordering Section.	11,90



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Development Features

Table 2 lists the features of ZiLOG[®]'s ZGP323H members.

Table 2. Features

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323H OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–5.5V

- Low power consumption—18mW (typical)
- T = Temperature
S = Standard 0° to +70°C
E = Extended -40° to +105°C
A = Automotive -40° to +125°C
- Three standby modes:
 - STOP— (typical 1.8μA)
 - HALT— (typical 0.8mA)
 - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
 - One programmable 8-bit counter/timer with two capture registers and two load registers
 - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
 - Programmable input glitch filter for pulse reception
- Six priority interrupts
 - Three external
 - Two assigned to counter/timers
 - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
 - Port 0: 0–3 pull-up transistors
 - Port 0: 4–7 pull-up transistors

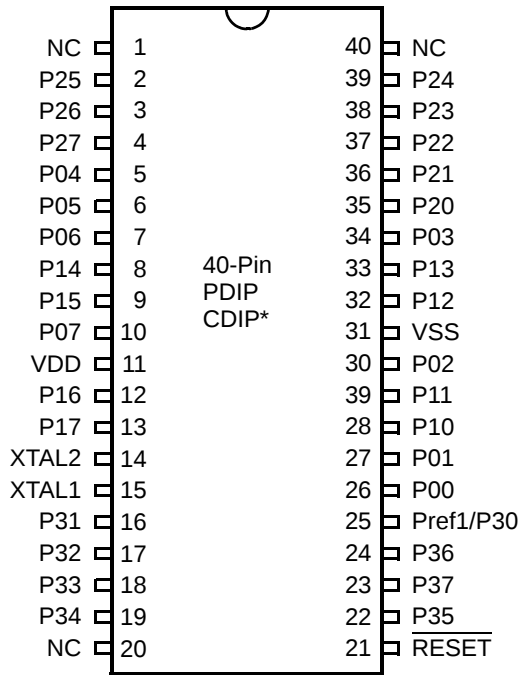


Figure 5. 40-Pin PDIP/CDIP* Pin Configuration

► **Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

Absolute Maximum Ratings

Stresses greater than those listed in Table 8 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	125	° C	1
Storage temperature	-65	+150	° C	
Voltage on any pin with respect to V_{SS}	-0.3	7.0	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	7.0	V	
Maximum current on input and/or inactive output pin	-5	+5	μ A	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	

Notes:

1. See Ordering Information.
2. This voltage applies to all pins except the following: V_{DD} , P32, P33 and RESET.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).

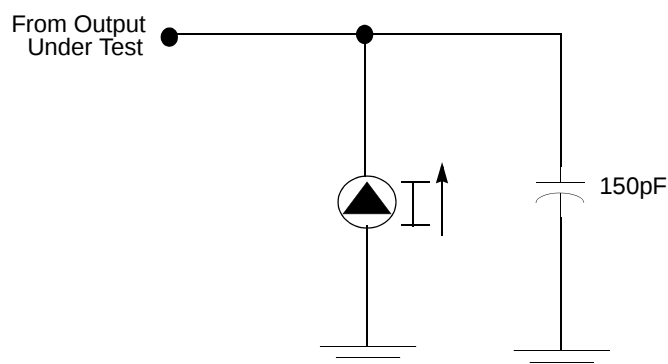


Figure 7. Test Load Diagram



Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position	Description
T16_Data_LO	[7:0]	R/W Data

Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position	Description
T8_Level_HI	[7:0]	R/W Data

Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position	Description
T8_Level_LO	[7:0]	R/W Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

Table 15. CTR0(D)00H Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-----	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5-----	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8_Clock	---43---	R/W	0 0**	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_Mask	----2--	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt



Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

Table 16. CTR1(0D)01H T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-----	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/ Demodulator_Input	-6-----	R/W	0*	Transmit Mode
			1	Port Output
				T8/T16 Output
			0*	Demodulation Mode
			1	P31
				P20
T8/T16_Logic/ Edge_Detect	--54----	R/W		Transmit Mode
			00**	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

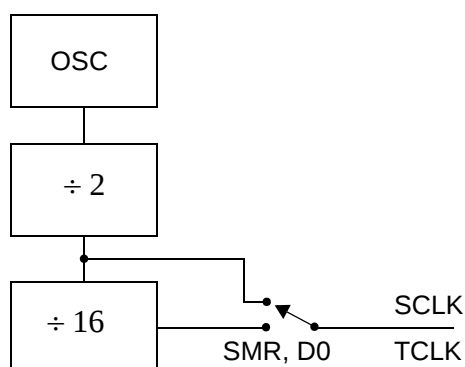


Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 22).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 21 lists and briefly describes the fields for this register.

Table 21. SMR2(F)0DH:Stop Mode Recovery Register 2*

Field	Bit Position	Value	Description
Reserved	7-----	0	Reserved (Must be 0)
Recovery Level	-6-----	W 0 [†] 1	Low High
Reserved	--5-----	0	Reserved (Must be 0)
Source	---432--	W 000 [†] 001 010 011 100 101 110 111	A. POR Only B. NAND of P23–P20 C. NAND of P27–P20 D. NOR of P33–P31 E. NAND of P33–P31 F. NOR of P33–P31, P00, P07 G. NAND of P33–P31, P00, P07 H. NAND of P33–P31, P22–P20
Reserved	-----10	00	Reserved (Must be 0)

Notes:

* Port pins configured as outputs are ignored as a SMR recovery source.

[†] Indicates the value upon Power-On Reset



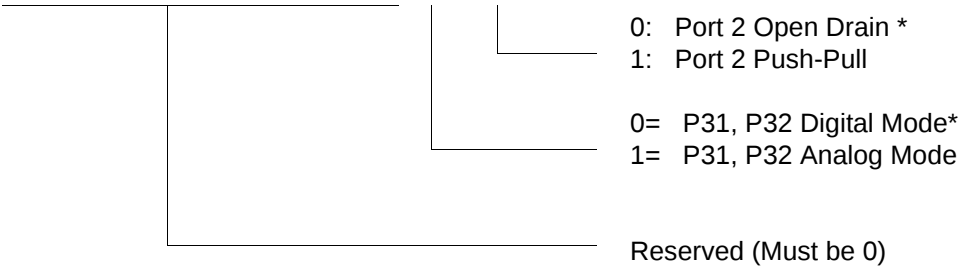
- **Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)

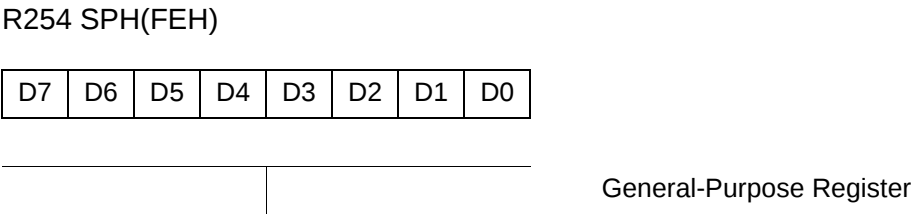


Figure 56. Stack Pointer High (FEH: Read/Write)

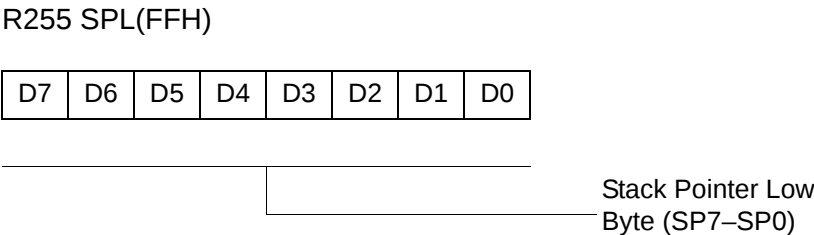


Figure 57. Stack Pointer Low (FFH: Read/Write)

Package Information

Package information for all versions of ZGP323H is depicted in Figures 59 through Figure 68.

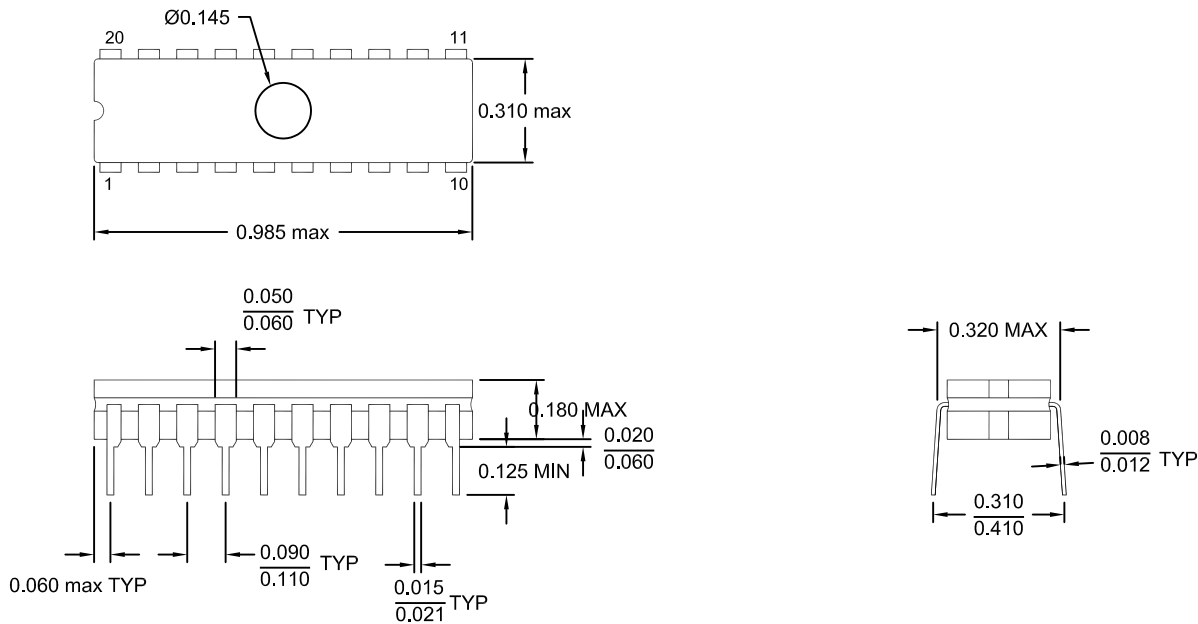


Figure 58. 20-Pin CDIP Package

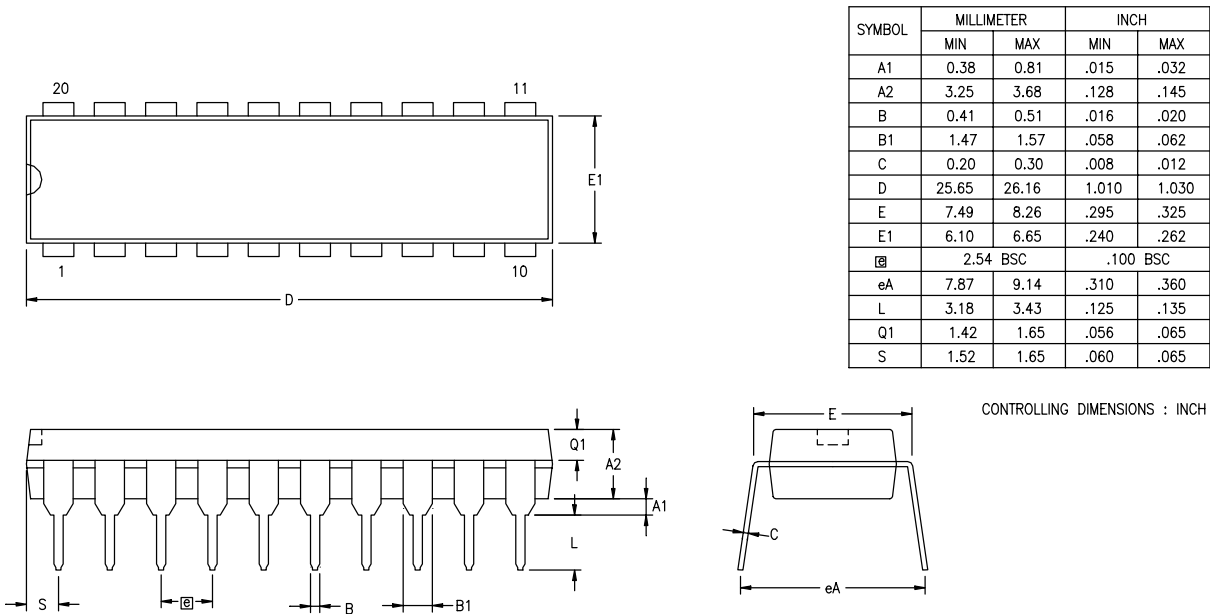
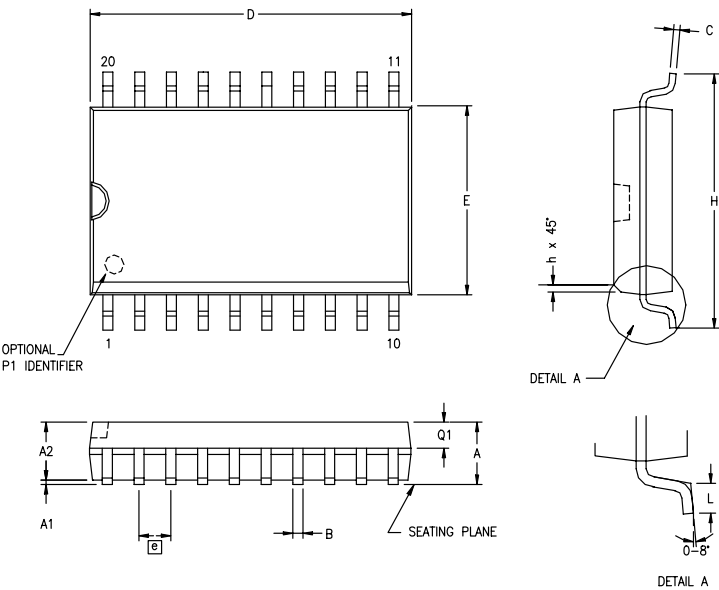


Figure 59. 20-Pin PDIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	12.60	12.95	.496	.510
E	7.40	7.60	.291	.299
⌀	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.40	.012	.016
L	0.60	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

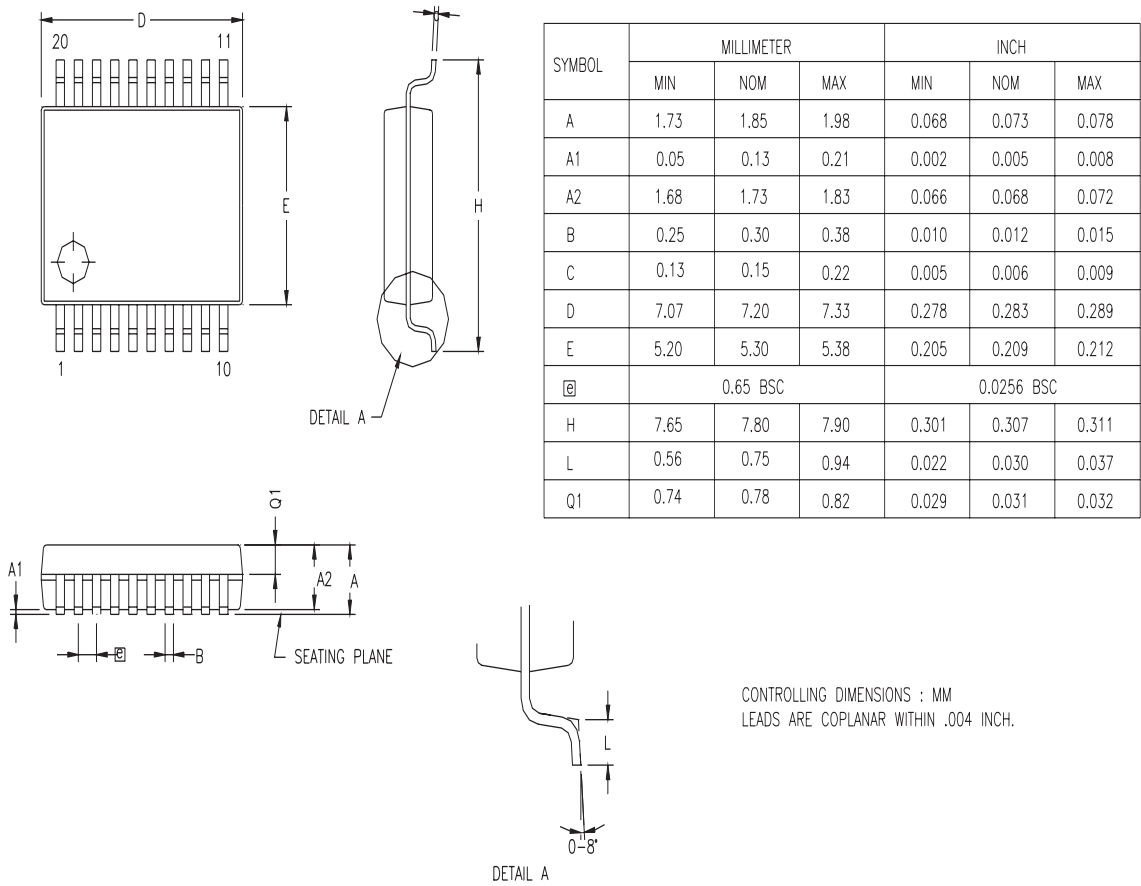


Figure 61. 20-Pin SSOP Package Diagram

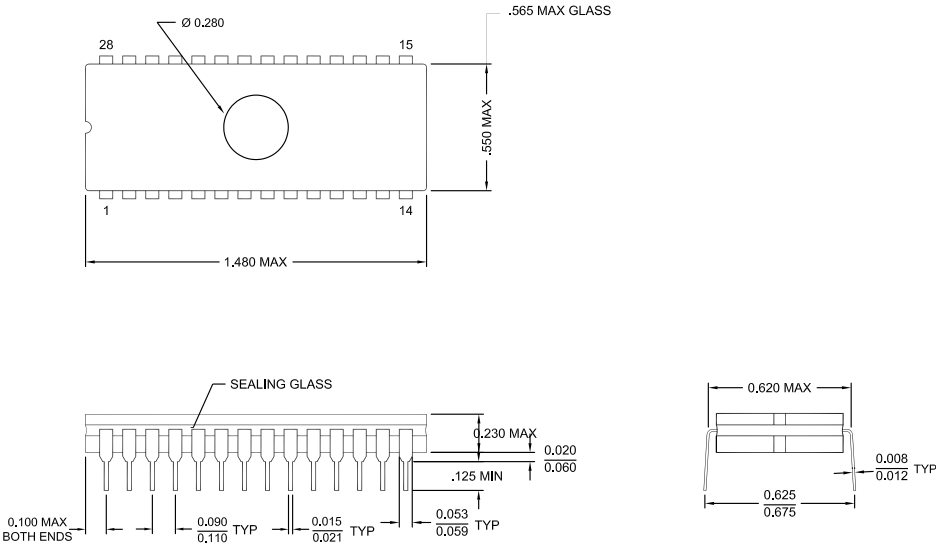
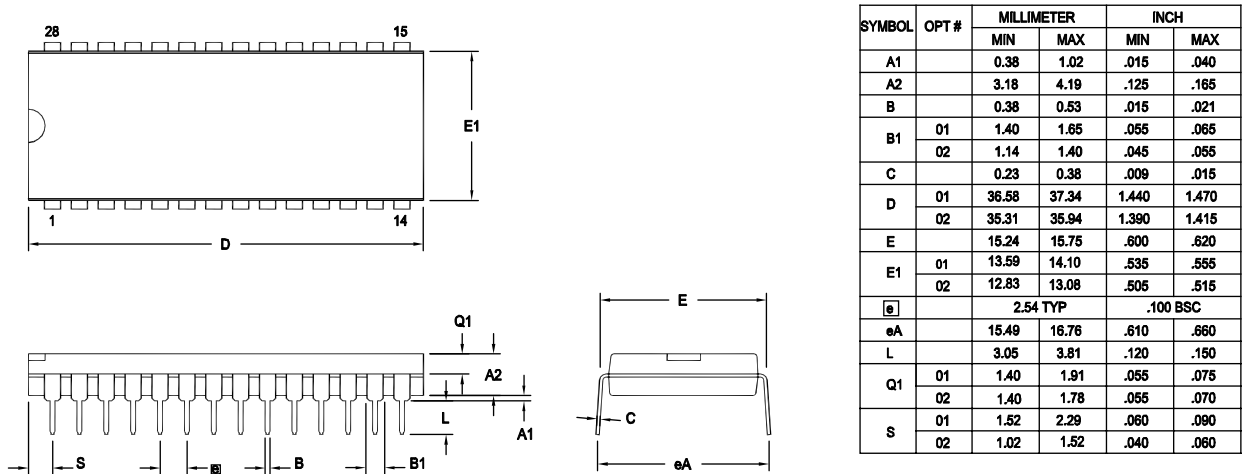


Figure 63. 28-Pin CDIP Package Diagram



CONTROLLING DIMENSIONS : INCH

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Note: ZILOG supplies both options for production. Component layout PCB design should cover bigger option 01.

Figure 64. 28-Pin PDIP Package Diagram

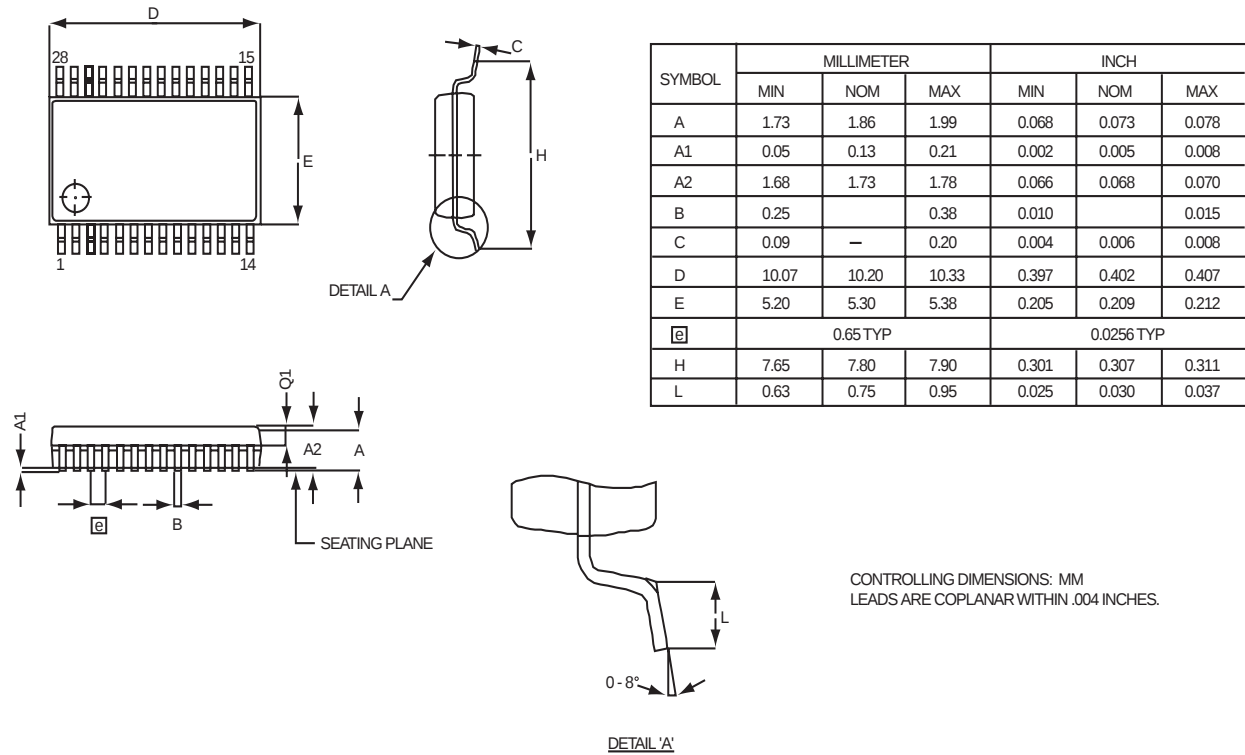


Figure 65. 28-Pin SSOP Package Diagram

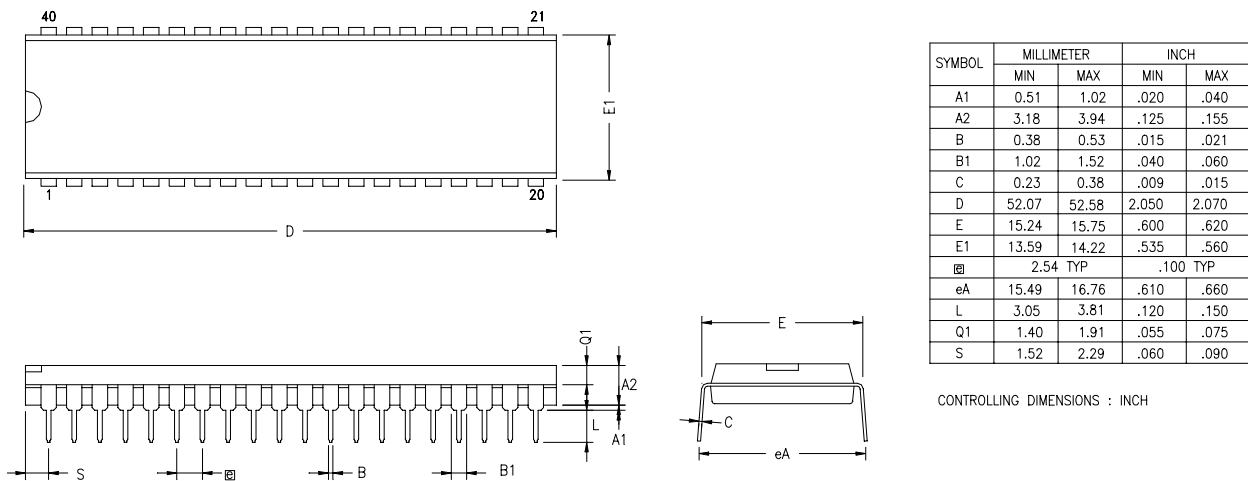


Figure 66. 40-Pin PDIP Package Diagram

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