## Zilog - ZGP323HAS2804G Datasheet





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#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323has2804g

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#### Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

Table 4.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V <sub>DD</sub>	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V <sub>SS</sub>	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output



	T <sub>Δ</sub> = -40°C to +105°C							
Symbol	Parameter	V <sub>CC</sub>	Min	Typ(7)	Max	Units	Conditions	Notes
V <sub>OH2</sub>	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V <sub>CC</sub> -0.8			V	I <sub>OH</sub> = -7mA	
V <sub>OL1</sub>	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$	
V <sub>OL2</sub>	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I <sub>OL</sub> = 10mA	
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V <sub>REF</sub>	Comparator Reference Voltage	2.0-5.5	0		V <sub>DD</sub> -1.75	V		
IIL	Input Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub> Pull-ups disabled	
R <sub>PU</sub>	Pull-up Resistance	2.0V	200.0		700.0	KΩ	V <sub>IN</sub> = 0V; Pullups selected by mask	
		3.6V	50.0		300.0	KΩ	option	
		5.0V	25.0		175.0	KΩ	_	
I <sub>OL</sub>	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0V, V_{CC}$	
I <sub>CC</sub>	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I <sub>CC1</sub>	Standby Current	2.0V		0.5	1.6	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
	(HALT Mode)	3.6V		0.8	2.0	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
I <sub>CC2</sub>	Standby Current (Stop	2.0V		1.6	12	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
	Mode)	3.6V		1.8	15	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
		5.5V		1.9	18	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		2.0V		5	30	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		3.6V		8	40	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		5.5V		15	60	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
I <sub>LV</sub>	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage Detection			2.4		V		
V <sub>HVD</sub>	Vcc High Voltage Detection			2.7		V		

#### Table 10. GP323HE DC Characteristics (Continued)

Notes:

1. All outputs unloaded, inputs at rail.

2. CL1 = CL2 = 100 pF.

3. Oscillator stopped.

4. Oscillator stops when  $V_{\mbox{\scriptsize CC}}$  falls below  $V_{\mbox{\scriptsize BO}}$  limit.

 It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VCC and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

6. Comparator and Timers are on. Interrupt disabled.

7. Typical values shown are at 25 degrees C.



## **AC Characteristics**





Figure 8. AC Timing Diagram



			T <sub>A</sub> =0°C to +70°C (S) −40°C to +105°C (E) −40°C to +125°C (A) 8.0MHz				Watch-Dog Timer Mode Register	
No	Symbol	Parameter	V <sub>CC</sub>	Minimum	Maximum	Units	Notes	(D1, D0)
1	ТрС	Input Clock Period	2.0–5.5	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–5.5		25	ns	1	
3	TwC	Input Clock Width	2.0–5.5	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 5.5	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–5.5	3ТрС			1	
6	TpTin	Timer Input Period	2.0–5.5	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–5.5		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 5.5	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–5.5	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width	2.0–5.5	12		ns	3	
		Spec		5TpC			4	
11	Tost	Oscillator Start-Up Time	2.0–5.5		5TpC		4	
12	Twdt	Watch-Dog Timer	2.0–5.5	5		ms		0, 0
		Delay Time	2.0–5.5	10		ms		0, 1
			2.0-5.5	20		ms		1,0
			2.0-0.0	ðU		ms		1, 1
13	T <sub>POR</sub>	Power-On Reset	2.0–5.5	2.5	10	ms		

#### **Table 13. AC Characteristics**

Notes:

1. Timing Reference uses 0.9  $V_{CC}$  for a logic 1 and 0.1  $V_{CC}$  for a logic 0. 2. Interrupt request through Port 3 (P33–P31).

3. SMR – D5 = 1.

4. SMR - D5 = 0.





Figure 11. Port 2 Configuration

## Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.



The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A OH in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.





#### Figure 16. Register Pointer

#### Example: Z8 GP: (See Figure 15 on page 28)

R253 RP = 00h R0 = Port 0 R1 = Port 1 R2 = Port 2 R3 = Port 3

But if:

R253 RP = 0Dh R0 = CTR0 R1 = CTR1 R2 = CTR2R3 = Reserved







Figure 17. Register Pointer—Detail

## Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



## Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field Bit Position			Description
T16_Data_LO	[7:0]	R/W	Data

## Counter/Timer8 High Hold Register—TC8H(D)05H

Field Bit Position			Description
T8_Level_HI	[7:0]	R/W	Data

## Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

## CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

Table 15. CTR0(D)00H Counter/Timera	<b>3 Control Register</b>
-------------------------------------	---------------------------

Field	<b>Bit Position</b>		Value	Description
T8_Enable	7	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W	0*	Modulo-N
-			1	Single Pass
Time_Out	5	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	43	R/W	0 0**	SCLK
			0 1	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt



#### Table 15.CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	0	R/W	0* 1	P34 as Port Output T8 Output on P34

#### Note:

\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

## **T8 Enable**

This field enables T8 when set (written) to 1.

## Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

### Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



**Caution:** Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

### **T8 Clock**

This bit defines the frequency of the input signal to T8.



When T8 is enabled, the output T8\_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8\_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8\_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8\_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8\_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8\_OUT level and repeats the cycle. See Figure 20.



Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



**Caution:** To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



FF	NOP	;	clear	the pipeline
6F	Stop	;	enter	Stop Mode
or				
FF	NOP	;	clear	the pipeline
7F	HALT	;	enter	HALT Mode

## **Port Configuration Register**

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

## PCON(FH)00H



\* Default setting after reset

#### Figure 32. Port Configuration Register (PCON) (Write Only)

#### Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

#### Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.



## Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

## Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XORgate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/ TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address OBH.





## Low-Voltage Detection Register—LVD(D)0Ch

**Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position			Description
LVD	76543			Reserved No Effect
	2	R	1 0*	HVD flag set HVD flag reset
	1-	R	1 0*	LVD flag set LVD flag reset
	0	R/W	1 0*	Enable VD Disable VD
*Default after POR				

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

#### **Voltage Detection and Flags**

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the V<sub>CC</sub> voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the V<sub>CC</sub> level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V<sub>CC</sub> is higher than V<sub>HVD</sub>. The LVD flag (bit 1 of the LVD register) is set only if V<sub>CC</sub> is lower than the V<sub>LVD</sub>. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

**Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.



## LVD(0D)0CH



\* Default setting after reset.

#### Figure 43. Voltage Detection Register

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

## **Expanded Register File Control Registers (0F)**

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.



## R248 P01M(F8H)



\* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

### Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)











Figure 63. 28-Pin CDIP Package Diagram



SYMBOL	OPT #	MILLIMETER		INCH	
		MíN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
В		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
С		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
s	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH



01

02

STANDARD

Figure 64. 28-Pin PDIP Package Diagram





Figure 67. 40-Pin CDIP Package Diagram

ZGP323H Product Specification



# **Ordering Information**

#### 32KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4832C	48-pin SSOP 32K OTP	ZGP323HSS2832C	28-pin SOIC 32K OTP
ZGP323HSP4032C	40-pin PDIP 32K OTP	ZGP323HSH2032C	20-pin SSOP 32K OTP
ZGP323HSK2832E	28-pin CDIP 32K OTP	ZGP323HSK2032E	20-pin CDIP 32K OTP
ZGP323HSK4032E	40-pin CDIP 32K OTP	ZGP323HSP2032C	20-pin PDIP 32K OTP
ZGP323HSH2832C	28-pin SSOP 32K OTP	ZGP323HSS2032C	20-pin SOIC 32K OTP
ZGP323HSP2832C	28-pin PDIP 32K OTP		

#### 32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4832C	48-pin SSOP 32K OTP	ZGP323HES2832C	28-pin SOIC 32K OTP
ZGP323HEP4032C	40-pin PDIP 32K OTP	ZGP323HEH2032C	20-pin SSOP 32K OTP
ZGP323HEH2832C	28-pin SSOP 32K OTP	ZGP323HEP2032C	20-pin PDIP 32K OTP
ZGP323HEP2832C	28-pin PDIP 32K OTP	ZGP323HES2032C	20-pin SOIC 32K OTP

32KB Automotive Temperature: -40° to +125°C				
Part Number	Description	Part Number	Description	
ZGP323HAH4832C	48-pin SSOP 32K OTP	ZGP323HAS2832C	28-pin SOIC 32K OTP	
ZGP323HAP4032C	40-pin PDIP 32K OTP	ZGP323HAH2032C	20-pin SSOP 32K OTP	
ZGP323HAH2832C	28-pin SSOP 32K OTP	ZGP323HAP2032C	20-pin PDIP 32K OTP	
ZGP323HAP2832C	28-pin PDIP 32K OTP	ZGP323HAS2032C	20-pin SOIC 32K OTP	
Replace C with G fo	r Lead-Free Packaging			



## Example



#### ZGP323H Z8<sup>®</sup> OTP Microcontroller with IR Timers



pin 4 Ε **EPROM** selectable options 64 expanded register file 26 expanded register file architecture 28 expanded register file control registers 71 flag 80 interrupt mask register 79 interrupt priority register 78 interrupt request register 79 port 0 and 1 mode register 77 port 2 configuration register 75 port 3 mode register 76 port configuration register 75 register pointer 80 stack pointer high register 81 stack pointer low register 81 stop-mode recovery register 73 stop-mode recovery register 2 74 T16 control register 69 T8 and T16 common control functions register 67 T8/T16 control register 70 TC8 control register 66 watch-dog timer register 75 F features standby modes 1 functional description counter/timer functional blocks 40 CTR(D)01h register 35 CTR0(D)00h register 33 CTR2(D)02h register 37 CTR3(D)03h register 39 expanded register file 26 expanded register file architecture 28 HI16(D)09h register 32 HI8(D)0Bh register 32 L08(D)0Ah register 32 L0I6(D)08h register 32

program memory map 26 **RAM 25** register description 65 register file 30 register pointer 29 register pointer detail 31 SMR2(F)0D1h register 40 stack 31 TC16H(D)07h register 32 TC16L(D)06h register 33 TC8H(D)05h register 33 TC8L(D)04h register 33 G glitch filter circuitry 40 Η halt instruction, counter/timer 54 input circuit 40 interrupt block diagram, counter/timer 51 interrupt types, sources and vectors 52 L low-voltage detection register 65 Μ memory, program 25 modulo-N mode T16 OUT 47 T8 OUT 43 0 oscillator configuration 53 output circuit, counter/timer 49 Ρ package information 20-pin DIP package diagram 82 20-pin SSOP package diagram 84 28-pin DIP package diagram 86 28-pin SOIC package diagram 85 28-pin SSOP package diagram 87 40-pin DIP package diagram 87 48-pin SSOP package diagram 89 pin configuration 20-pin DIP/SOIC/SSOP 5