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"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323has2808g

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–   Port 1: 0–3 pull-up transistors
–   Port 1: 4–7 pull-up transistors
–   Port 2: 0–7 pull-up transistors
–   EPROM Protection
–   WDT enabled at POR

General Description

The ZGP323H is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The ZGP323H architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

▶   **Note:**   All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 3.
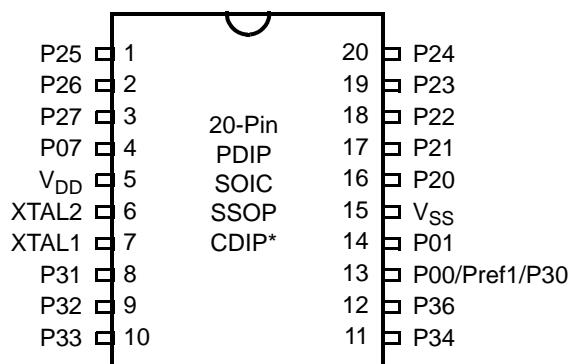
Figure 3.   20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 4.   20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V_{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V_{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output
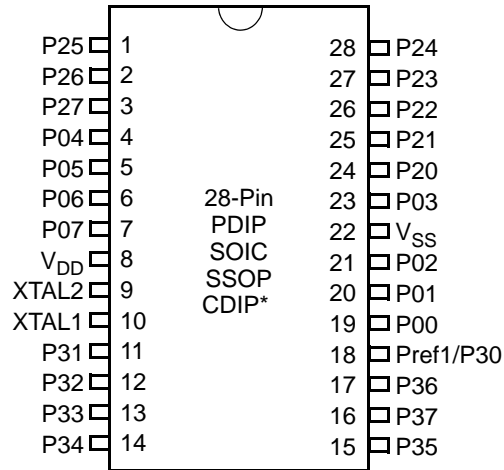
Figure 4.   28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 5.   28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V_{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V_{CC} if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V_{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

Table 6. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	$\overline{\text{RESET}}$
15	18	XTAL1
14	17	XTAL2
11	12, 13	V_{DD}
31	24, 37, 38	V_{SS}
25	29	Pref1/P30
	48	NC
	6	NC
	14	NC
	30	NC
	36	NC

Pin Functions

XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

> **Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.
>
> The Port 0 direction is reset to its default state following an SMR.

Location of
first Byte of
instruction
executed
after RESET

32768

	Not Accessible
	On-Chip ROM
12	Reset Start Address
11	IRQ5
10	IRQ5
9	IRQ4
8	IRQ4
7	IRQ3
6	IRQ3
5	IRQ2
4	IRQ2
3	IRQ1
2	IRQ1
1	IRQ0
0	IRQ0

Interrupt Vector
(Lower Byte)

Interrupt Vector
(Upper Byte)

Figure 14. Program Memory Map (32K OTP)

Expanded Register File

The register file has been expanded to allow for additional system control regis-
ters and for mapping of additional peripheral devices into the register address
area. The Z8® register address space (R0 through R15) has been implemented
as 16 banks, with 16 registers per bank. These register groups are known as the

Z8® Standard Control Registers

Register Pointer

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Working Register Group Pointer

Expanded Register Bank Pointer

Register File (Bank 0)**

FF
F0

7F

0F
00

Reset Condition

Expanded Reg. Bank 0/Group 15**

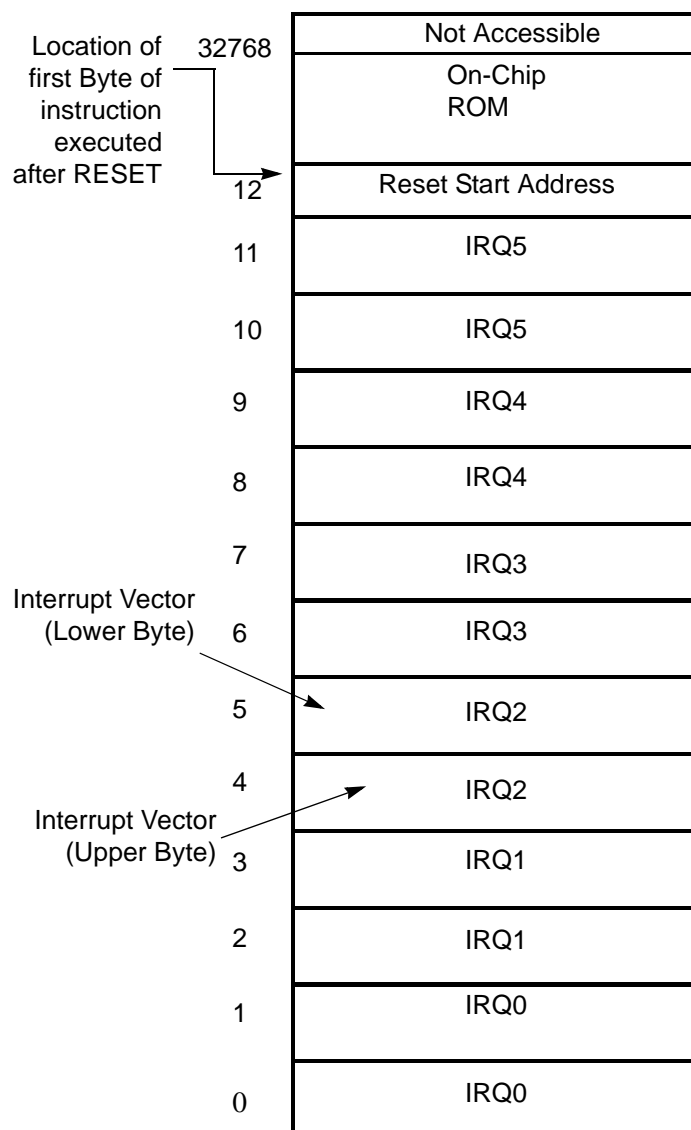|			D7	D6	D5	D4	D3	D2	D1	D0
	FF	SPL	U	U	U	U	U	U	U	U
	FE	SPH	U	U	U	U	U	U	U	U
	FD	RP	0	0	0	0	0	0	0	0
	FC	FLAGS	U	U	U	U	U	U	U	U
	FB	IMR	U	U	U	U	U	U	U	U
	FA	IRQ	0	0	0	0	0	0	0	0
	F9	IPR	U	U	U	U	U	U	U	U
	F8	P01M	1	1	0	0	1	1	1	1
*	F7	P3M	0	0	0	0	0	0	0	0
*	F6	P2M	1	1	1	1	1	1	1	1
	F5	Reserved	U	U	U	U	U	U	U	U
	F4	Reserved	U	U	U	U	U	U	U	U
	F3	Reserved	U	U	U	U	U	U	U	U
	F2	Reserved	U	U	U	U	U	U	U	U
	F1	Reserved	U	U	U	U	U	U	U	U
	F0	Reserved	U	U	U	U	U	U	U	U

Expanded Reg. Bank F/Group 0**

			D7	D6	D5	D4	D3	D2	D1	D0
*	(F) 0F	WDTMR	U	U	0	0	1	1	0	1
	(F) 0E	Reserved								
*	(F) 0D	SMR2	0	0	0	0	0	0	0	0
	(F) 0C	Reserved								
↑	(F) 0B	SMR	U	0	1	0	0	0	U	0
	(F) 0A	Reserved								
	(F) 09	Reserved								
	(F) 08	Reserved								
	(F) 07	Reserved								
	(F) 06	Reserved								
	(F) 05	Reserved								
	(F) 04	Reserved								
	(F) 03	Reserved								
	(F) 02	Reserved								
	(F) 01	Reserved								
*	(F) 00	PCON	1	1	1	1	1	1	1	0

Expanded Reg. Bank 0/Group (0)

	(0) 03	P3	0	U
	(0) 02	P2	U	
*	(0) 01	P1	U	
	(0) 00	P0	U	

Expanded Reg. Bank D/Group 0

			D7	D6	D5	D4	D3	D2	D1	D0
	(D) 0C	LVD	U	U	U	U	U	U	U	0
*	(D) 0B	HI8	0	0	0	0	0	0	0	0
*	(D) 0A	LO8	0	0	0	0	0	0	0	0
*	(D) 09	HI16	0	0	0	0	0	0	0	0
*	(D) 08	LO16	0	0	0	0	0	0	0	0
*	(D) 07	TC16H	0	0	0	0	0	0	0	0
*	(D) 06	TC16L	0	0	0	0	0	0	0	0
*	(D) 05	TC8H	0	0	0	0	0	0	0	0
*	(D) 04	TC8L	0	0	0	0	0	0	0	0
↑↑	(D) 03	CTR3	0	0	0	1	1	1	1	1
↑↑↑	(D) 02	CTR2	0	0	0	0	0	0	0	0
↑↑↑↑	(D) 01	CTR1	0	0	0	0	0	0	0	0
↑↑↑↑↑	(D) 00	CTR0	0	0	0	0	0	0	0	0

U = Unknown

* Is not reset with a Stop-Mode Recovery

** All addresses are in hexadecimal

↑ Is not reset with a Stop-Mode Recovery, except Bit 0

↑↑ Bit 5 Is not reset with a Stop-Mode Recovery

↑↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery

↑↑↑↑ Bits 5 and 4 not reset with a Stop-Mode Recovery
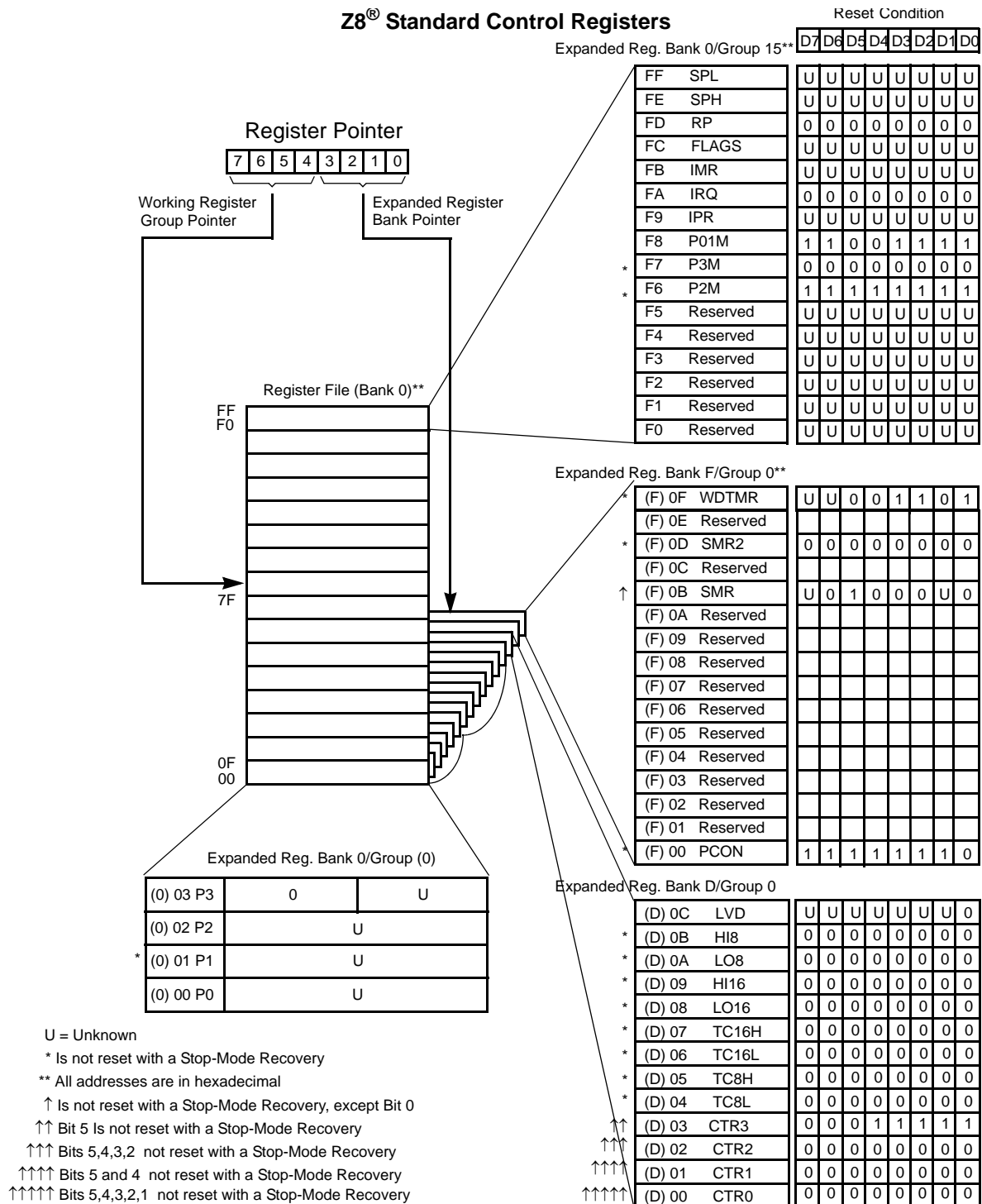
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery

Figure 15. Expanded Register File Architecture

Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

Table 15. CTR0(D)00H Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-------	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5------	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0**	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_Mask	-----2--	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with `FFh` and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from `FFH` (see Figure 23 and Figure 24).
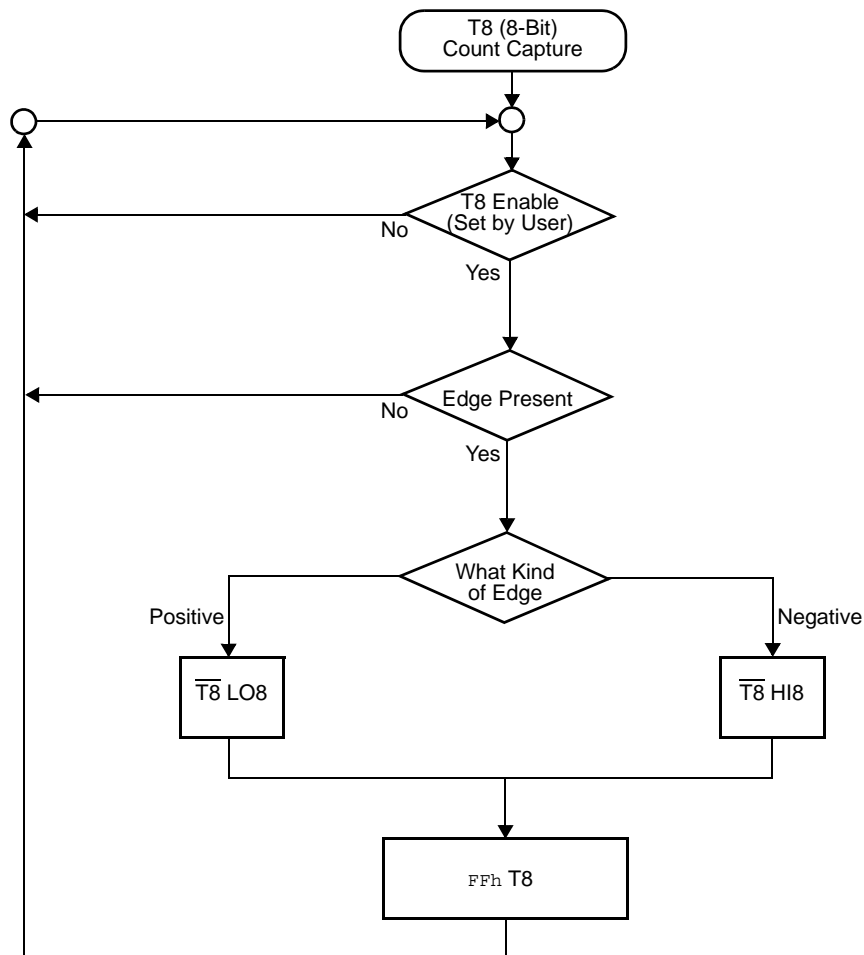

Figure 23. Demodulation Mode Count Capture Flowchart

Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/ TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

Table 24. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.

Low-Voltage Detection Register—LVD(D)0Ch

▶ **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position			Description
LVD	76543---			Reserved No Effect
	-----2--	R	1 0*	HVD flag set HVD flag reset
	------1-	R	1 0*	LVD flag set LVD flag reset
	-------0	R/W	1 0*	Enable VD Disable VD

*Default after POR

▶ **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.
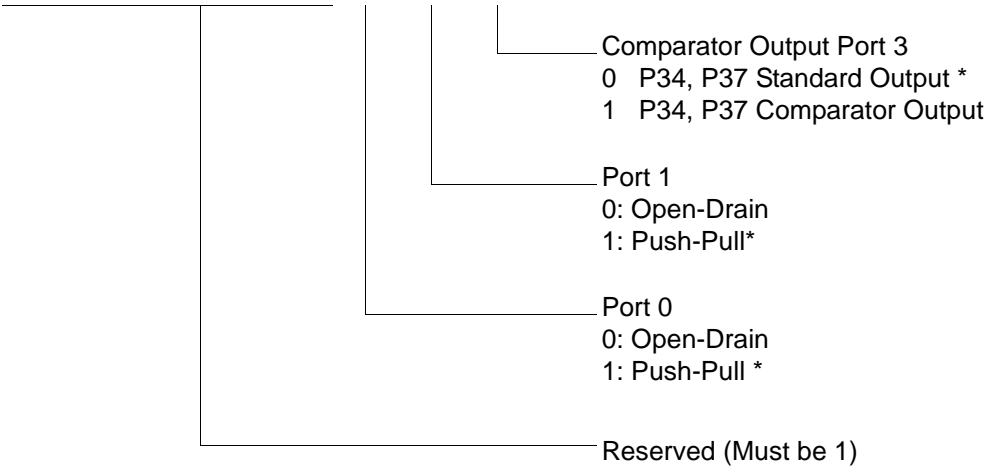
Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the V_{CC} level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V_{CC} is higher than $V_{HVD.}$ The LVD flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

▶ **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

PCON(0F)00H

D7	D6	D5	D4	D3	D2	D1	D0

Comparator Output Port 3
0   P34, P37 Standard Output *
1   P34, P37 Comparator Output

Port 1
0: Open-Drain
1: Push-Pull*

Port 0
0: Open-Drain
1: Push-Pull *

Reserved (Must be 1)

 * Default setting after reset

Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)

SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0

SCLK/TCLK Divide-by-16
0   OFF *
1   ON

Reserved (Must be 0)

Stop-Mode Recovery Source
000   POR Only *
001   Reserved
010   P31
011   P32
100   P33
101   P27
110   P2 NOR 0–3
111   P2 NOR 0–7

Stop Delay
0   OFF
1   ON * * * *

Stop Recovery Level * * *
0   Low *
1   High

Stop Flag
0   POR * * * * *
1   Stop Recovery * *
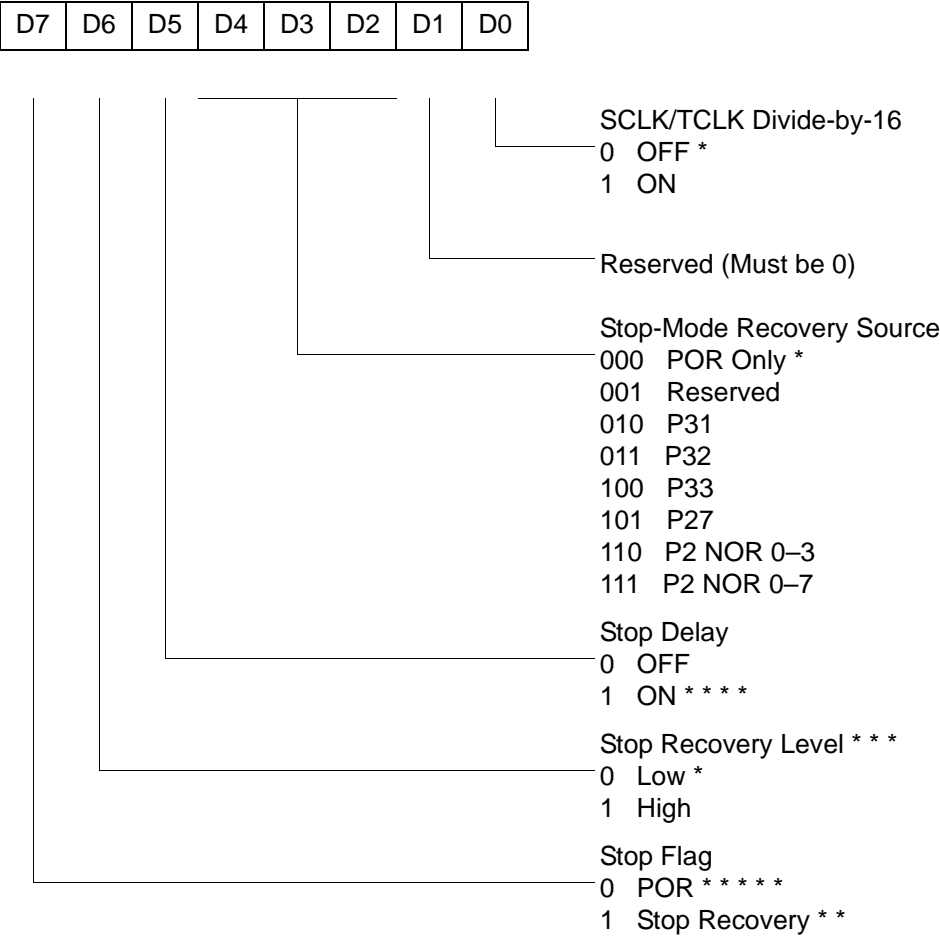
* Default setting after reset
* * Set after Stop Mode Recovery
* * * At the XOR gate input
* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.
* * * * * Default setting after Power On Reset. Not reset with a Stop Mode recovery.

Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)
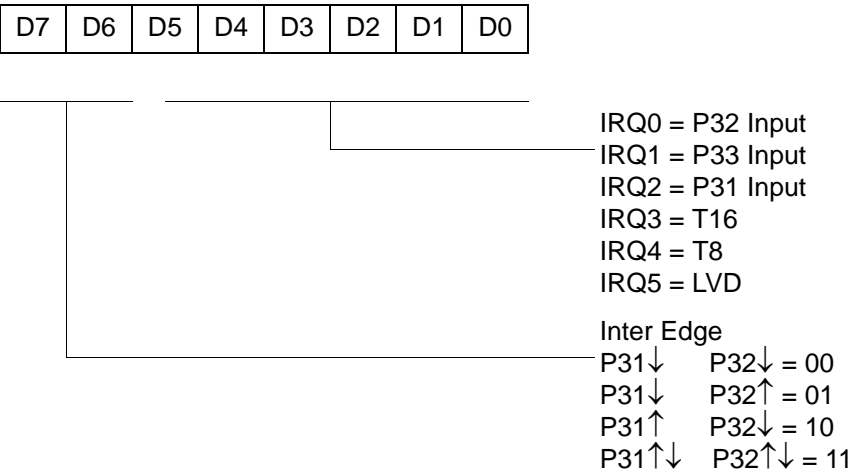
R250 IRQ(FAH)

D7	D6	D5	D4	D3	D2	D1	D0

IRQ0 = P32 Input
IRQ1 = P33 Input
IRQ2 = P31 Input
IRQ3 = T16
IRQ4 = T8
IRQ5 = LVD

Inter Edge
P31↓   P32↓ = 00
P31↓   P32↑ = 01
P31↑   P32↓ = 10
P31↑↓   P32↑↓ = 11

Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)

D7	D6	D5	D4	D3	D2	D1	D0

1 Enables IRQ5–IRQ0
   (D0 = IRQ0)

Reserved (Must be 0)

0   Master Interrupt Disable *
1   Master Interrupt Enable * *

 * Default setting after reset
 * * Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)

16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4816C	48-pin SSOP 16K OTP	ZGP323HSS2816C	28-pin SOIC 16K OTP
ZGP323HSP4016C	40-pin PDIP 16K OTP	ZGP323HSH2016C	20-pin SSOP 16K OTP
ZGP323HSH2816C	28-pin SSOP 16K OTP	ZGP323HSP2016C	20-pin PDIP 16K OTP
ZGP323HSP2816C	28-pin PDIP 16K OTP	ZGP323HSS2016C	20-pin SOIC 16K OTP

16KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4816C	48-pin SSOP 16K OTP	ZGP323HES2816C	28-pin SOIC 16K OTP
ZGP323HEP4016C	40-pin PDIP 16K OTP	ZGP323HEH2016C	20-pin SSOP 16K OTP
ZGP323HEH2816C	28-pin SSOP 16K OTP	ZGP323HEP2016C	20-pin PDIP 16K OTP
ZGP323HEP2816C	28-pin PDIP 16K OTP	ZGP323HES2016C	20-pin SOIC 16K OTP

16KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323HAH4816C	48-pin SSOP 16K OTP	ZGP323HAS2816C	28-pin SOIC 16K OTP
ZGP323HAP4016C	40-pin PDIP 16K OTP	ZGP323HAH2016C	20-pin SSOP 16K OTP
ZGP323HAH2816C	28-pin SSOP 16K OTP	ZGP323HAP2016C	20-pin PDIP 16K OTP
ZGP323HAP2816C	28-pin PDIP 16K OTP	ZGP323HAS2016C	20-pin SOIC 16K OTP
Replace C with G for Lead-Free Packaging			

8KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4808C	48-pin SSOP 8K OTP	ZGP323HSS2808C	28-pin SOIC 8K OTP
ZGP323HSP4008C	40-pin PDIP 8K OTP	ZGP323HSH2008C	20-pin SSOP 8K OTP
ZGP323HSH2808C	28-pin SSOP 8K OTP	ZGP323HSP2008C	20-pin PDIP 8K OTP
ZGP323HSP2808C	28-pin PDIP 8K OTP	ZGP323HSS2008C	20-pin SOIC 8K OTP

8KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4808C	48-pin SSOP 8K OTP	ZGP323HES2808C	28-pin SOIC 8K OTP
ZGP323HEP4008C	40-pin PDIP 8K OTP	ZGP323HEH2008C	20-pin SSOP 8K OTP
ZGP323HEH2808C	28-pin SSOP 8K OTP	ZGP323HEP2008C	20-pin PDIP 8K OTP
ZGP323HEP2808C	28-pin PDIP 8K OTP	ZGP323HES2008C	20-pin SOIC 8K OTP

8KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323HAH4808C	48-pin SSOP 8K OTP	ZGP323HAS2808C	28-pin SOIC 8K OTP
ZGP323HAP4008C	40-pin PDIP 8K OTP	ZGP323HAH2008C	20-pin SSOP 8K OTP
ZGP323HAH2808C	28-pin SSOP 8K OTP	ZGP323HAP2008C	20-pin PDIP 8K OTP
ZGP323HAP2808C	28-pin PDIP 8K OTP	ZGP323HAS2008C	20-pin SOIC 8K OTP
Replace C with G for Lead-Free Packaging			

Example

```
ZG    P    323    H    T    P    48    32    C
```

- Molding Compound
- Memory Size
- Number of Pins
- Package Type:
  E = CDIP
  P = PDIP
  H = SSOP
  S = SOIC
- Temperature:
  S = Standard
  E = Extended
  A = Automotive
- Voltage:
  H = High
- Family Designation
- OTP
- ZiLOG General-Purpose Family