# Zilog - ZGP323HAS2816C00TR Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | HLVD, POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zgp323has2816c00tr |

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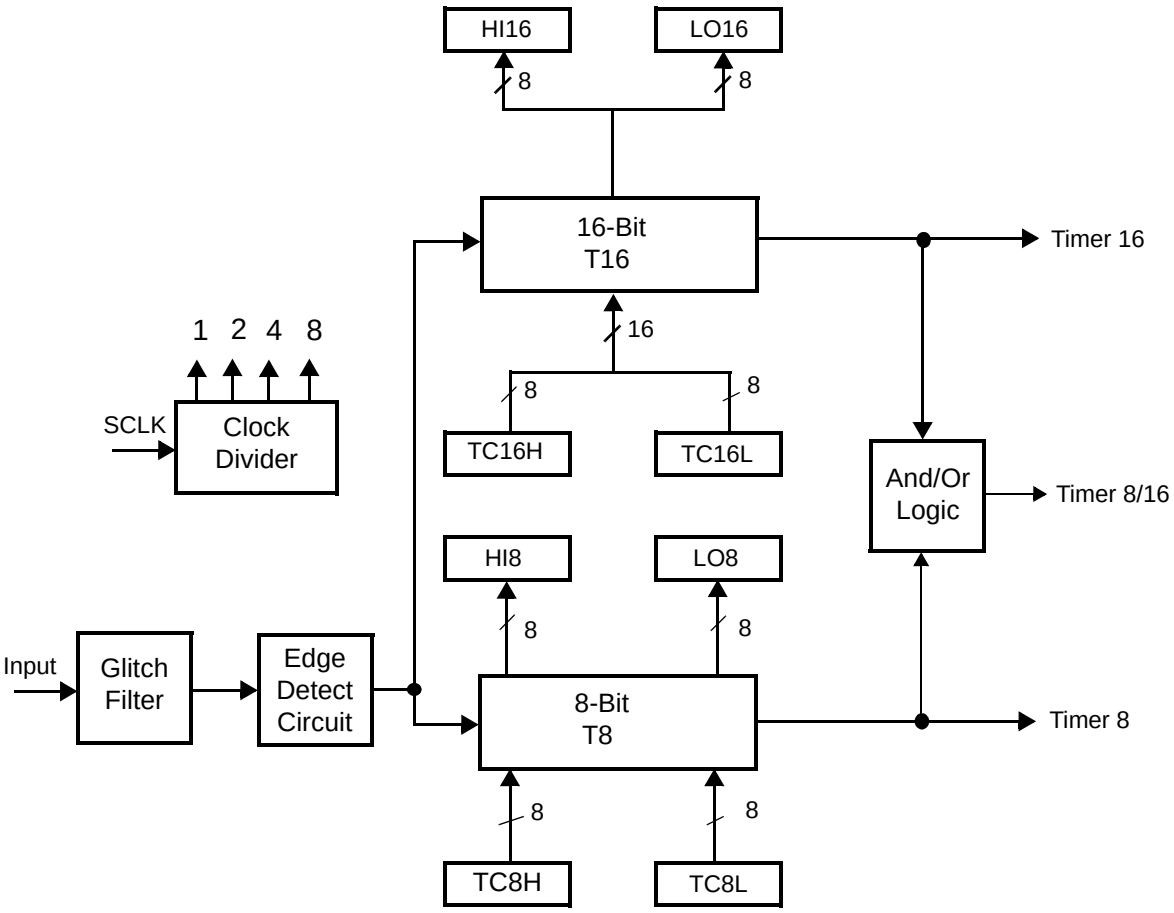



**Figure 2. Counter/Timers Diagram**

## Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.

# AC Characteristics

Figure 8 and Table 13 describe the Alternating Current (AC) characteristics.

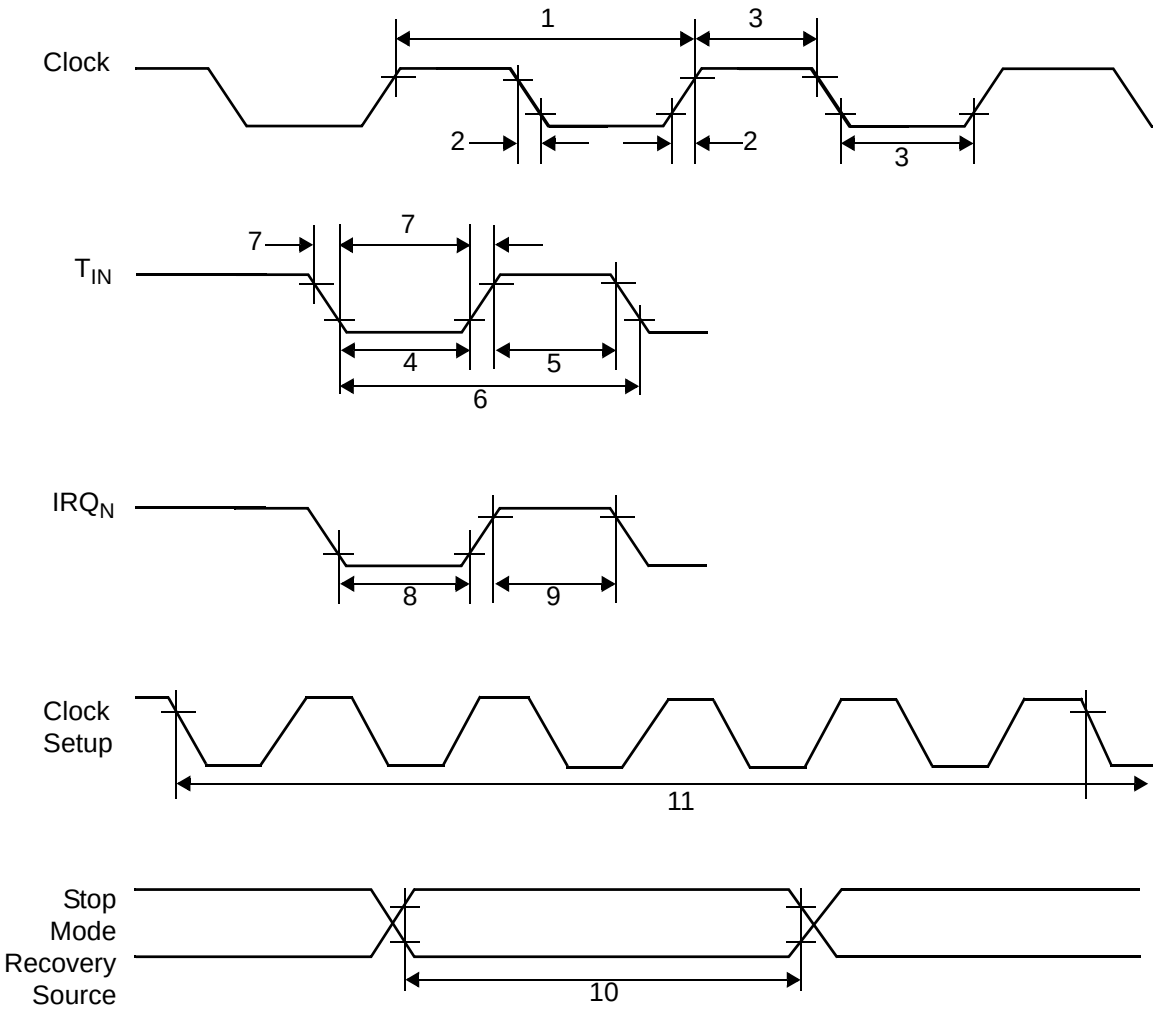



**Figure 8. AC Timing Diagram**

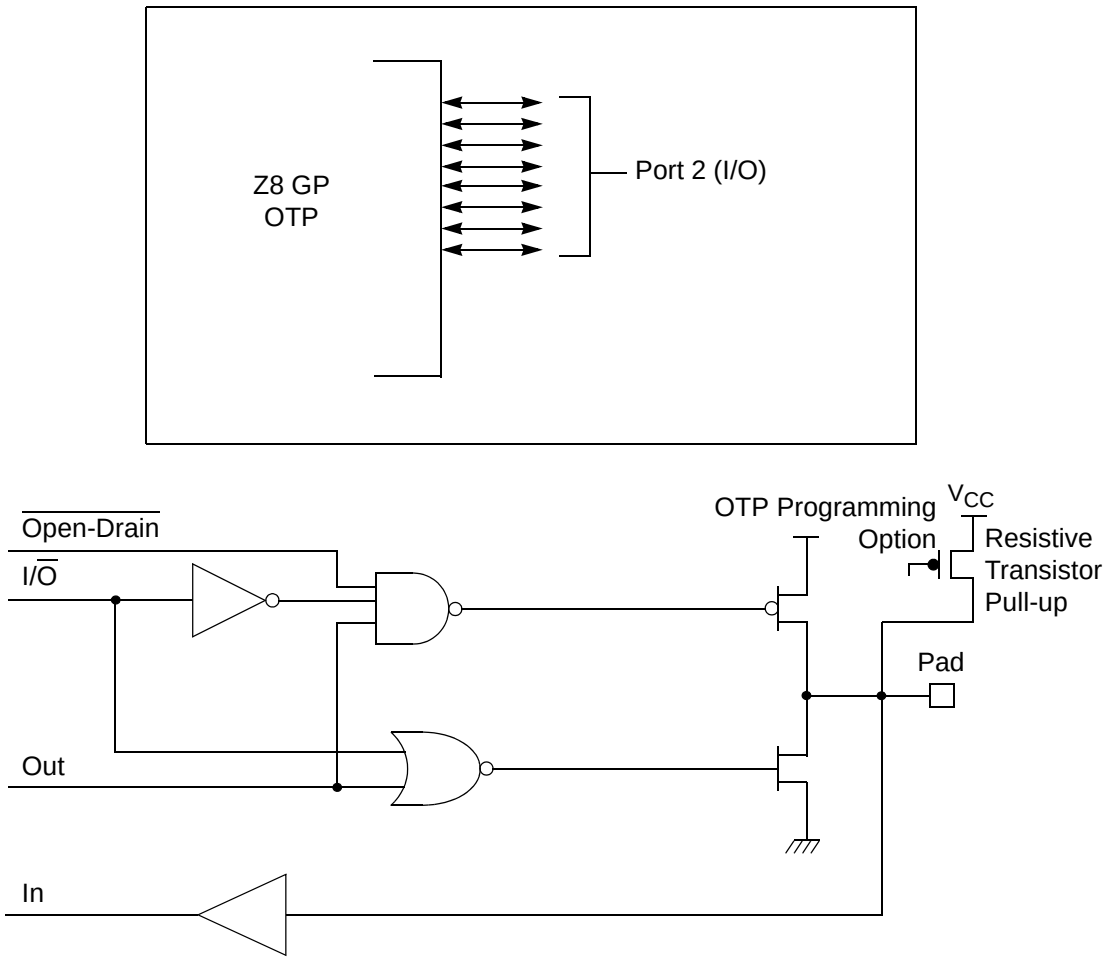



**Figure 11. Port 2 Configuration**

## Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

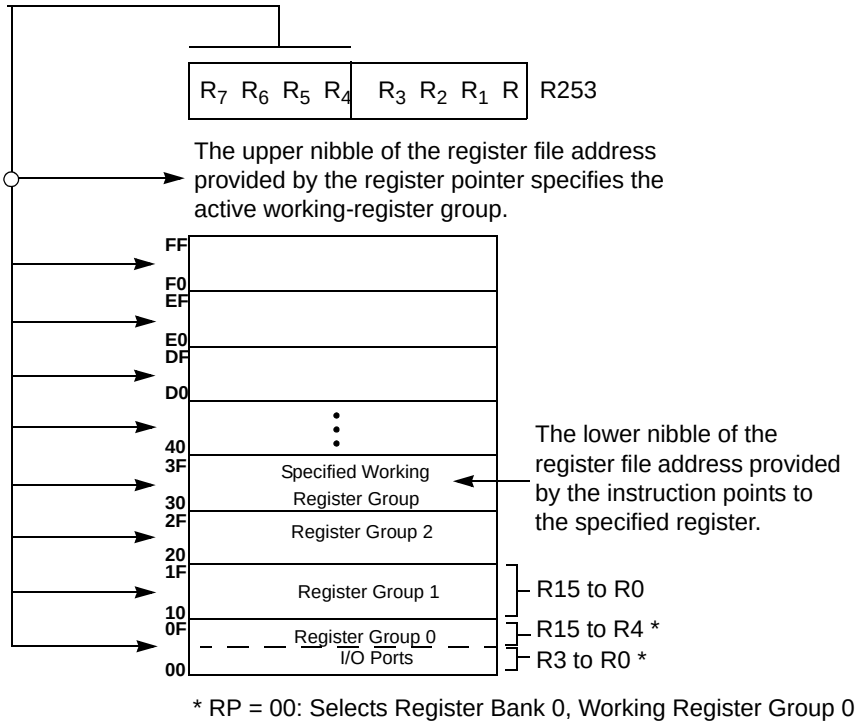



**Figure 17. Register Pointer—Detail**

## Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

### Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

### Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

### P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

### T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

**Table 16. CTR1(0D)01H T8 and T16 Common Functions**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Mode | 7------- | R/W | 0* | Transmit Mode |
| | | | | Demodulation Mode |
| P36_Out/ | -6------ | R/W | | Transmit Mode |
| Demodulator_Input | | | 0* | Port Output |
| | | | 1 | T8/T16 Output |
| | | | | Demodulation Mode |
| | | | 0* | P31 |
| | | | 1 | P20 |
| T8/T16_Logic/ | --54---- | R/W | | Transmit Mode |
| Edge _Detect | | | 00** | AND |
| | | | 01 | OR |
| | | | 10 | NOR |
| | | | 11 | NAND |
| | | | | Demodulation Mode |
| | | | 00** | Falling Edge |
| | | | 01 | Rising Edge |
| | | | 10 | Both Edges |
| | | | 11 | Reserved |

**Table 18. CTR3 (D)03H: T8/T16 Control Register (Continued)**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Reserved | ---43210 | R<br>W | 1<br>x | Always reads 11111<br>No Effect |

*Indicates the value upon Power-On Reset.
**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

## Counter/Timer Functional Blocks

### Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).

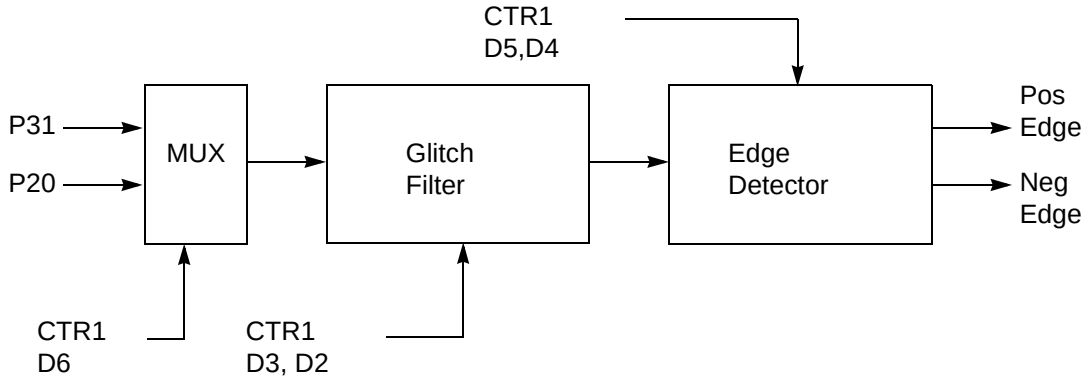



**Figure 18. Glitch Filter Circuitry**

### T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.

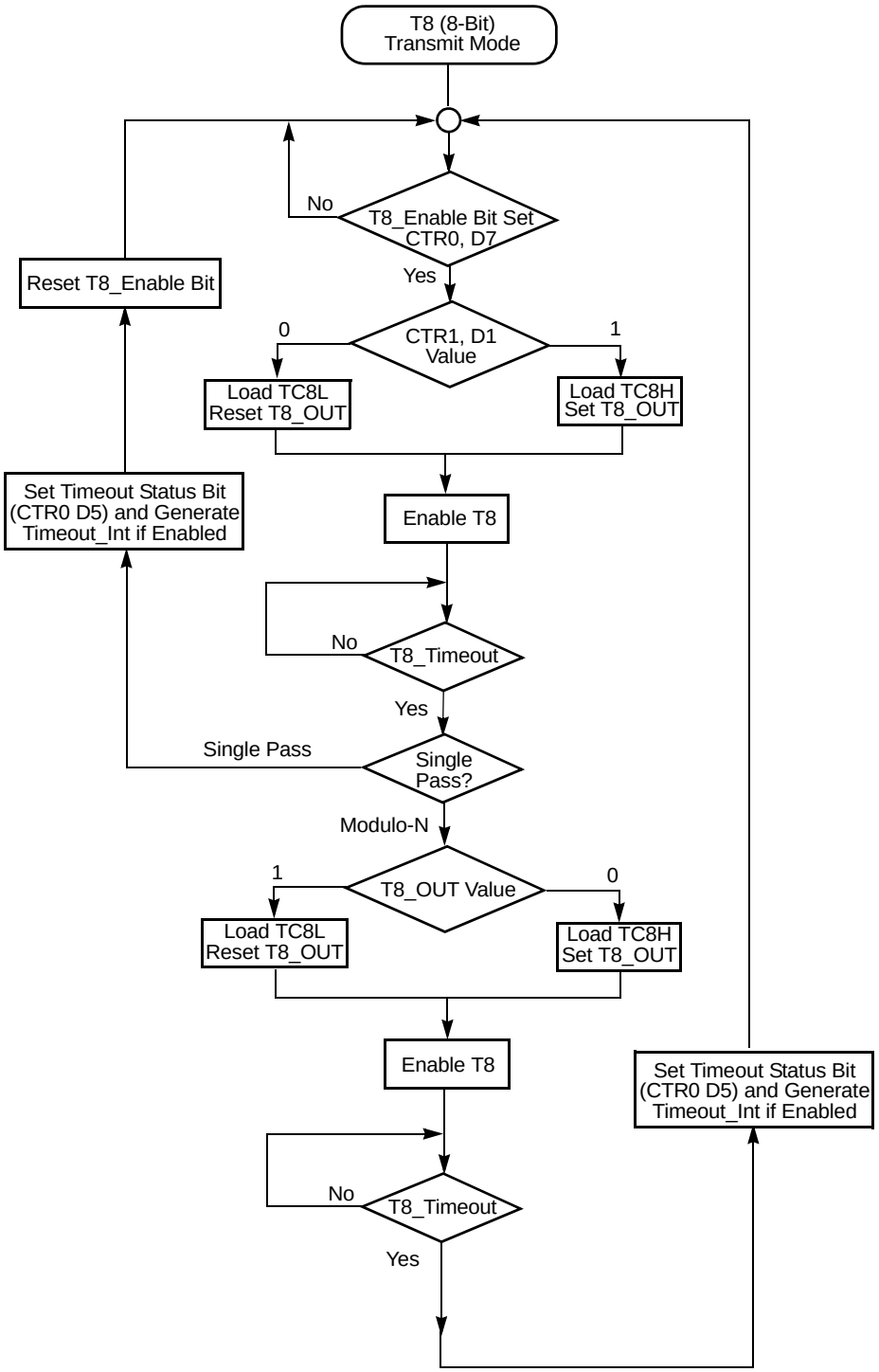



**Figure 19. Transmit Mode Flowchart**

**Caution:** Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFEH. Transition from 0 to FFFFH is not a timeout condition.

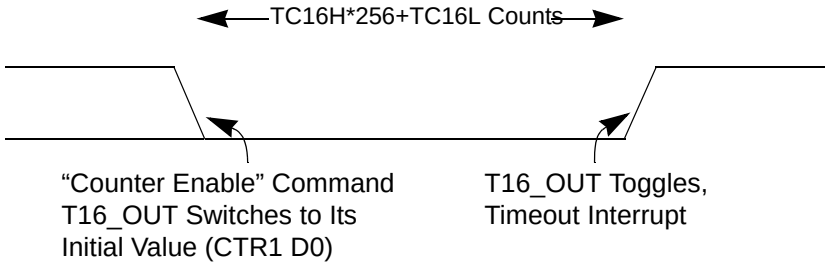



**Figure 26. T16_OUT in Single-Pass Mode**

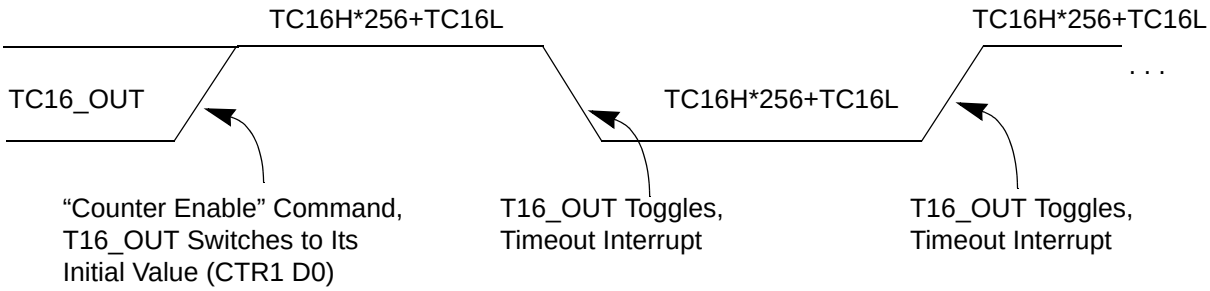



**Figure 27. T16_OUT in Modulo-N Mode**

### T16 DEMODULATION Mode

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

### If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

### Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows $V_{DD}$ and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from $V_{BO}$ Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

### HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

### STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10 μA or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:

### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

### EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

**Table 24. EPROM Selectable Options**

| | |
|---|---|
| Port 00–03 Pull-Ups | On/Off |
| Port 04–07 Pull-Ups | On/Off |
| Port 10–13 Pull-Ups | On/Off |
| Port 14–17 Pull-Ups | On/Off |
| Port 20–27 Pull-Ups | On/Off |
| EPROM Protection | On/Off |
| Watch-Dog Timer at Power-On Reset | On/Off |

### Voltage Brown-Out/Standby

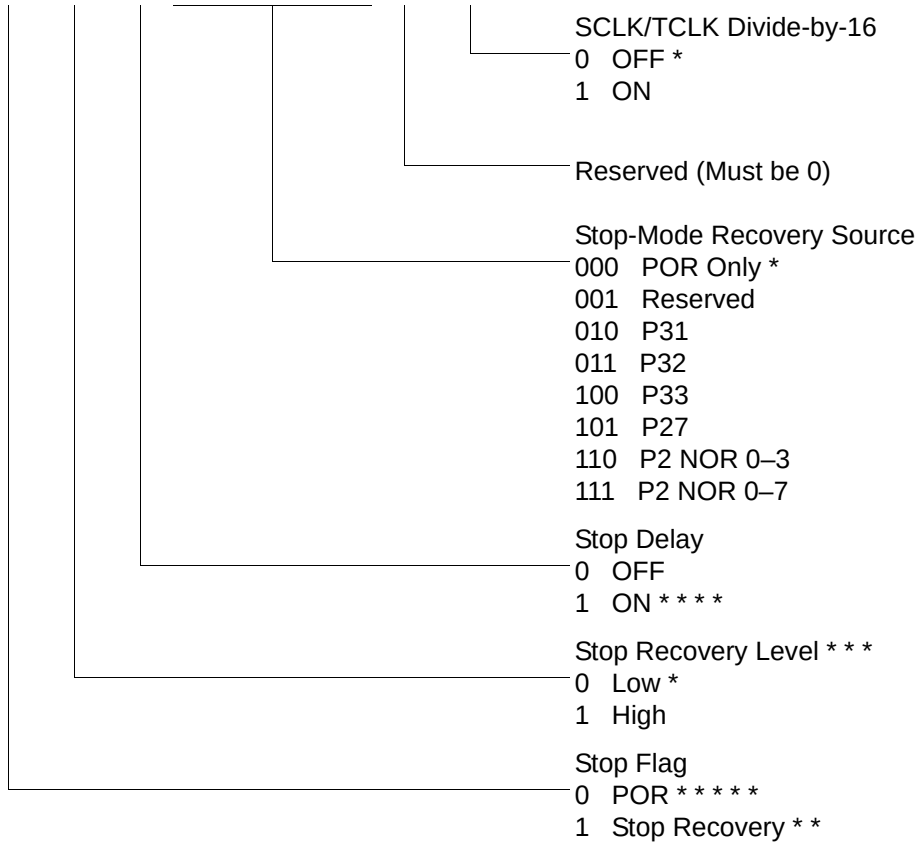
An on-chip Voltage Comparator checks that the $V_{DD}$ is at the required level for correct operation of the device. Reset is globally driven when $V_{DD}$ falls below $V_{BO}$. A small drop in $V_{DD}$ causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the $V_{DD}$ is allowed to stay above $V_{RAM}$, the RAM content is preserved. When the power level is returned to above $V_{BO}$, the device performs a POR and functions normally.

**Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.

SMR(0F)0BH

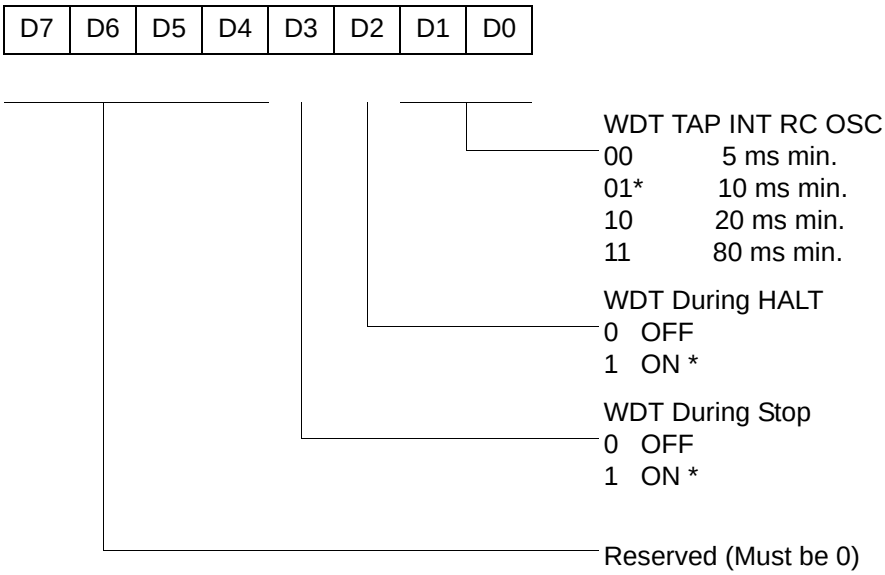
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|




* Default setting after reset
* * Set after Stop Mode Recovery
* * * At the XOR gate input
* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.
* * * * * Default setting after Power On Reset. Not reset with a Stop Mode recovery.

**Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)**

WDTMR(0F)0FH

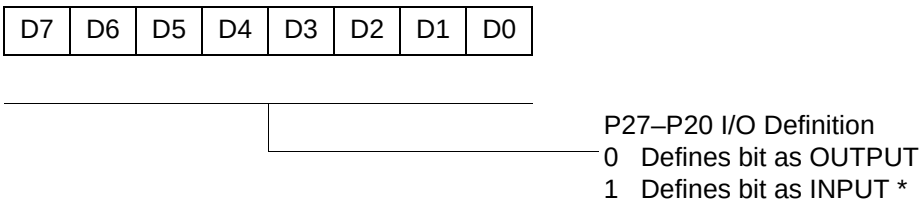



* Default setting after reset. Not reset with a Stop Mode recovery.

**Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)**

## Standard Control Registers

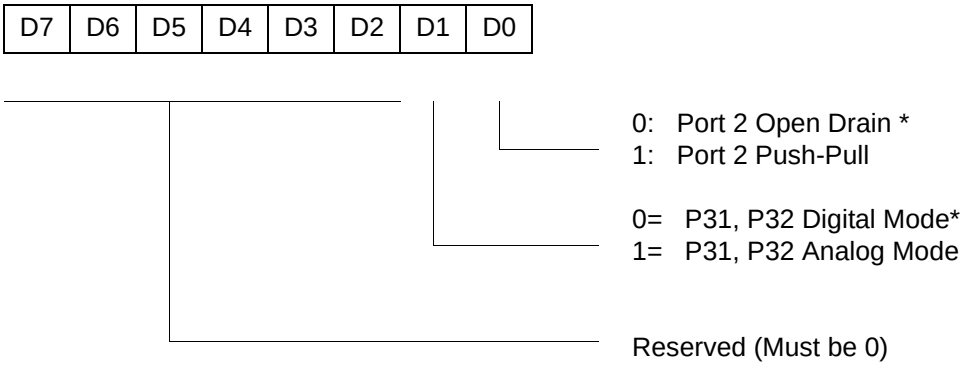
R246 P2M(F6H)




* Default setting after reset. Not reset with a Stop Mode recovery.

**Figure 48. Port 2 Mode Register (F6H: Write Only)**

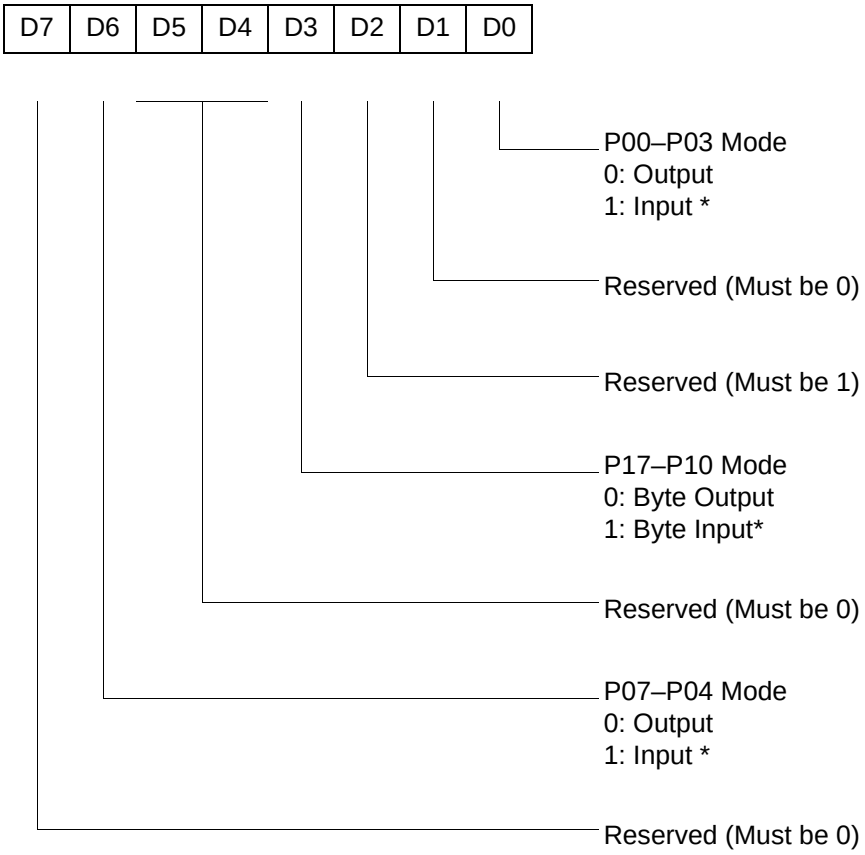
R247 P3M(F7H)




* Default setting after reset. Not reset with a Stop Mode recovery.

**Figure 49. Port 3 Mode Register (F7H: Write Only)**

R248 P01M(F8H)




* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

**Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)**

R252 Flags(FCH)

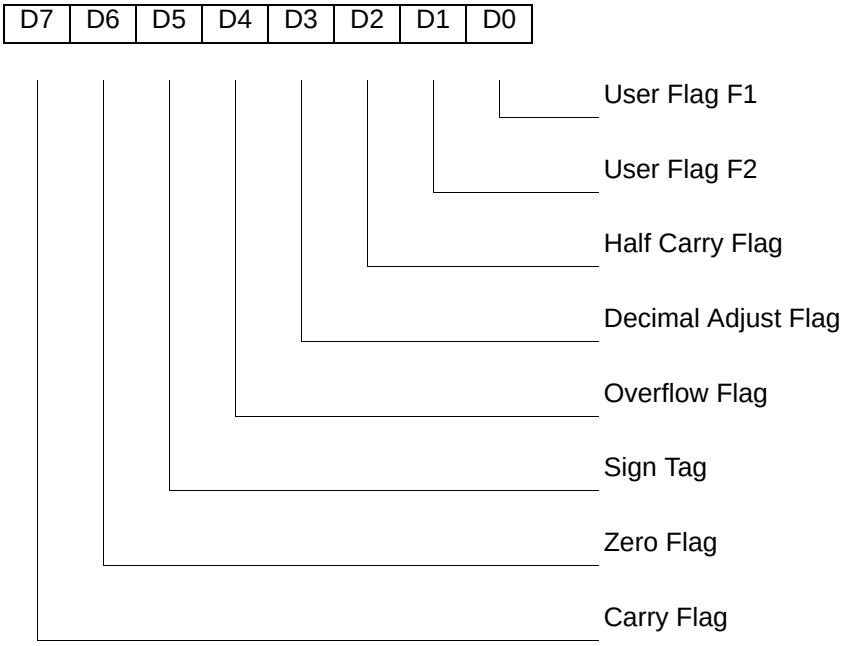
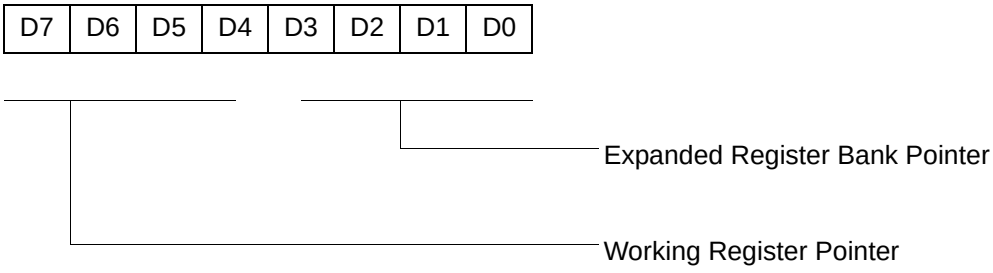



**Figure 54. Flag Register (FCH: Read/Write)**

R253 RP(FDH)




Default setting after reset = 0000 0000

**Figure 55. Register Pointer (FDH: Read/Write)**

| 4KB Standard Temperature: 0° to +70°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HSH4804C | 48-pin SSOP 4K OTP | ZGP323HSS2804C | 28-pin SOIC 4K OTP |
| ZGP323HSP4004C | 40-pin PDIP 4K OTP | ZGP323HSH2004C | 20-pin SSOP 4K OTP |
| ZGP323HSH2804C | 28-pin SSOP 4K OTP | ZGP323HSP2004C | 20-pin PDIP 4K OTP |
| ZGP323HSP2804C | 28-pin PDIP 4K OTP | ZGP323HSS2004C | 20-pin SOIC 4K OTP |

| 4KB Extended Temperature: -40° to +105°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HEH4804C | 48-pin SSOP 4K OTP | ZGP323HES2804C | 28-pin SOIC 4K OTP |
| ZGP323HEP4004C | 40-pin PDIP 4K OTP | ZGP323HEH2004C | 20-pin SSOP 4K OTP |
| ZGP323HEH2804C | 28-pin SSOP 4K OTP | ZGP323HEP2004C | 20-pin PDIP 4K OTP |
| ZGP323HEP2804C | 28-pin PDIP 4K OTP | ZGP323HES2004C | 20-pin SOIC 4K OTP |

| 4KB Automotive Temperature: -40° to +125°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HAH4804C | 48-pin SSOP 4K OTP | ZGP323HAS2804C | 28-pin SOIC 4K OTP |
| ZGP323HAP4004C | 40-pin PDIP 4K OTP | ZGP323HAH2004C | 20-pin SSOP 4K OTP |
| ZGP323HAH2804C | 28-pin SSOP 4K OTP | ZGP323HAP2004C | 20-pin PDIP 4K OTP |
| ZGP323HAP2804C | 28-pin PDIP 4K OTP | ZGP323HAS2004C | 20-pin SOIC 4K OTP |
| Replace C with G for Lead-Free Packaging | | | |

| Additional Components | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323ICE01ZEM (For 3.6V Emulation only) | Emulator/programmer | ZGP32300100ZPR (Ethernet) | Programming system |
| | | ZGP32300200ZPR (USB) | Programming system |

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