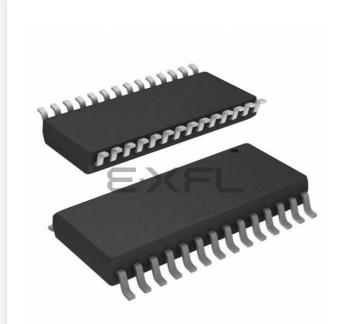
#### Zilog - ZGP323HAS2832G Datasheet





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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323has2832g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

ZGP323H | Product Specification |



## **Table of Contents**

Revision History iii
Development Features 1
General Description 2
Pin Description
Absolute Maximum Ratings 10
Standard Test Conditions 10
DC Characteristics 11
AC Characteristics
Pin Functions 18   XTAL1 Crystal 1 (Time-Based Input) 18   XTAL2 Crystal 2 (Time-Based Output) 18   Port 0 (P07–P00) 18   Port 1 (P17–P10) 19   Port 2 (P27–P20) 20   Port 3 (P37–P30) 21   RESET (Input, Active Low) 25
Functional Description25Program Memory25RAM25Expanded Register File26Register File30Stack31Timers32Counter/Timer Functional Blocks40
Expanded Register File Control Registers (0D)
Expanded Register File Control Registers (0F) 71
Standard Control Registers
Package Information
Ordering Information





- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0-7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

## **General Description**

The ZGP323H is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG<sup>®</sup>'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The ZGP323H architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8<sup>®</sup> offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

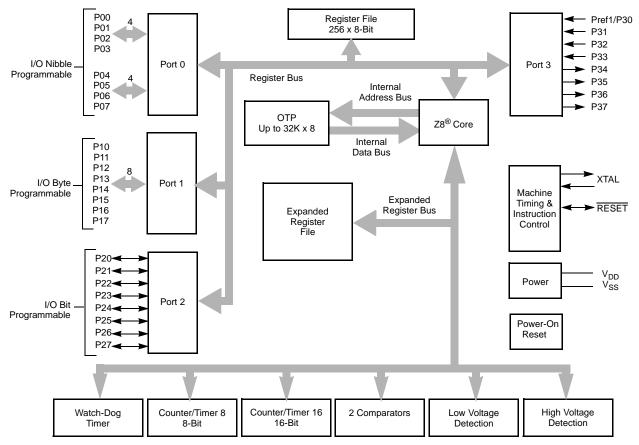
**Note:** All signals with an overline, "", are active Low. For example, B/W, in which WORD is active Low, and B/W, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 3.



#### Table 3. Power Connections

Connection	Circuit	Device	
Power	V <sub>CC</sub>	V <sub>DD</sub>	
Ground	GND	V <sub>SS</sub>	



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram





Figure 2. Counter/Timers Diagram

## **Pin Description**

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.

## ZGP323H Product Specification



	I					
NC		1	$\bigcirc$	48	-	NC
P25		2		47	-	NC
P26		3		46	-	P24
P27		4		45	-	P23
P04		5			-	P22
N/C		6				P21
P05		7				P20
P06		8		42		P03
P14		9		40	-	P13
P15		10		39	-	P12
P07		11		38	-	VSS
VDD		12	48-Pin	37	7	VSS
VDD		13	SSOP		-	N/C
N/C		14		35		P02
P16		15		34	7	P11
P17		16				P10
XTAL2		17		32		P01
XTAL1	Π	18		31	7	P00
P31		19		30	7	N/C
P32		20		29	-	PREF1/P30
P33		21		28		P36
		22		27	-	P37
		22		26	_	P35
VSS		23		25	_	RESET
		27		25	_	

Figure 6. 48-Pin SSOP Pin Configuration

Table 6. 40- and 48-Pin Configuration

40-Pin PDIP #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12



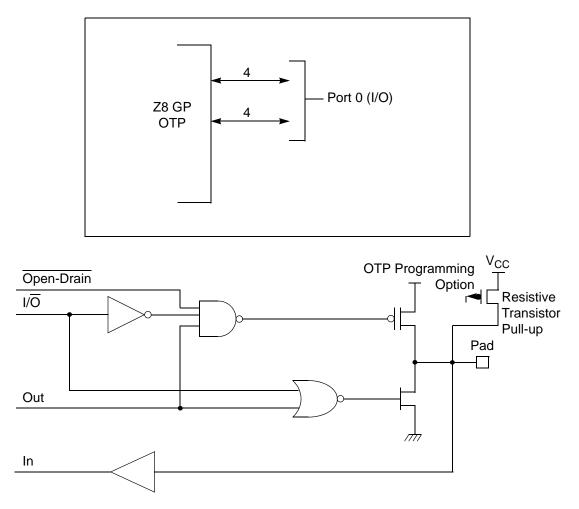


Figure 9. Port 0 Configuration

### Port 1 (P17–P10)

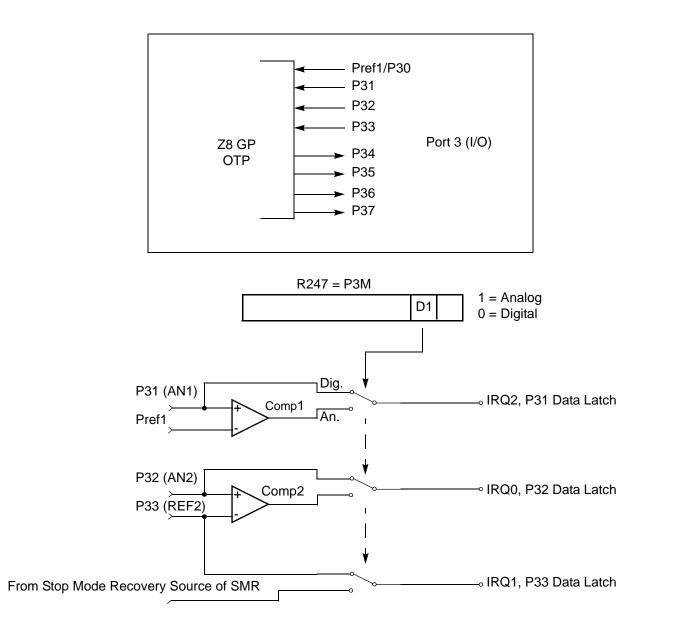
Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.



**Note:** The Port 1 direction is reset to its default state following an SMR.







#### Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—

## ZGP323H Product Specification



Location of C	0700	Not Accessible	
Location of 3	2768 1	On-Chip	
instruction		ROM	
executed after RESET			
aller RESET	12	Reset Start Address	
	11	IRQ5	
	10	IRQ5	
	9	IRQ4	
	8	IRQ4	
Interrupt \/e eter	7	IRQ3	
Interrupt Vector (Lower Byte)	6	IRQ3	
	5	IRQ2	
Interrupt Vecto	4 r	✓ IRQ2	
(Upper Byte		IRQ1	
	2	IRQ1	
	1	IRQ0	
	0	IRQ0	



### **Expanded Register File**

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8<sup>®</sup> register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

**Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).





Z8 <sup>®</sup> Standard (	Control Registers	Reset Condition
	Expanded Reg. Bank 0/Group 15	** D7 D6 D5 D4 D3 D2 D1 D0
	FF SPL	
	FE SPH	
Register Pointer	FD RP	0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	FC FLAGS	
	FB IMR	
Working Register Expanded Regist	er FA IRQ	0 0 0 0 0 0 0 0
Group Pointer Bank Pointer	F9 IPR	
	F8 P01M	1 1 0 0 1 1 1 1
	* F7 P3M	0 0 0 0 0 0 0 0
	* F6 P2M	
	F5 Reserved	
	F4 Reserved	
X	F3 Reserved F2 Reserved	
Register File (Bank 0)**		
FF F0		
	F0 Reserved	
	Expanded Reg. Bank F/Group 0**	×
	(F) OF WDTMR	
	(F) 0E Reserved	
	* (F) 0D_SMR2	0 0 0 0 0 0 0 0
	(F) 0C Reserved	
	(F) 0B_SMR	
7F	(F) 0A Reserved	
	(F) 09 Reserved	┫┣╌┽┽┽┽┽┽┽┥╴
	(F) 08 Reserved	┫┝┼┼┼┼┼┼┼┥
	(F) 07 Reserved	╢┝┼┼┼┼┼┼┼┤
	(F) 06 Reserved	┫┝┼┼┼┼┼┼┼┥
	(F) 05 Reserved	
₀₅┝────₽₽∕	(F) 04 Reserved	
	(F) 03 Reserved	
	(F) 02 Reserved	
	(F) 01 Reserved	┨┠┼┼┼┼┼┼┼┥
Expanded Reg. Bank 0/Group (0)	(F) 00 PCON	
	Expanded Reg. Bank D/Group 0	, <u>, , , , , , , , , , , , , , , , , , </u>
(0) 03 P3 0 U	(D) OC LVD	
(0) 02 P2 U	* (D) 0B HI8	00000000
* (0) 01 P1 U	* (D) 0A LO8	00000000
	* (D) 09 HI16	000000000
(0) 00 P0 U	* (D) 08 LO16	000000000
U = Unknown	* (D) 07 TC16H	0 0 0 0 0 0 0 0
* Is not reset with a Stop-Mode Recovery	* (D) 06 TC16L	00000000
** All addresses are in hexadecimal	* (D) 05 TC8H	00000000
↑ Is not reset with a Stop-Mode Recovery, except Bit 0	* (D) 04 TC8L	000000000
↑↑ Bit 5 Is not reset with a Stop-Mode Recovery	1↑ (D) 03 CTR3	0 0 0 1 1 1 1 1
↑↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery	↑↑↓ (D) 02 CTR2	000000000
↑↑↑↑ Bits 5 and 4 not reset with a Stop-Mode Recovery	↑↑↑↑ (D) 01 CTR1	0 0 0 0 0 0 0 0
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	000000000

#### Figure 15. Expanded Register File Architecture



#### T8/T16\_Logic/Edge \_Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

#### Transmit\_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to "NORMAL OPERATION Mode" terminates the "PING-PONG Mode" operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

#### Initial\_T8\_Out/Rising\_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

#### Initial\_T16 Out/Falling \_Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

**Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16\_OUT.

#### CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 17 lists and briefly describes the fields for this register.





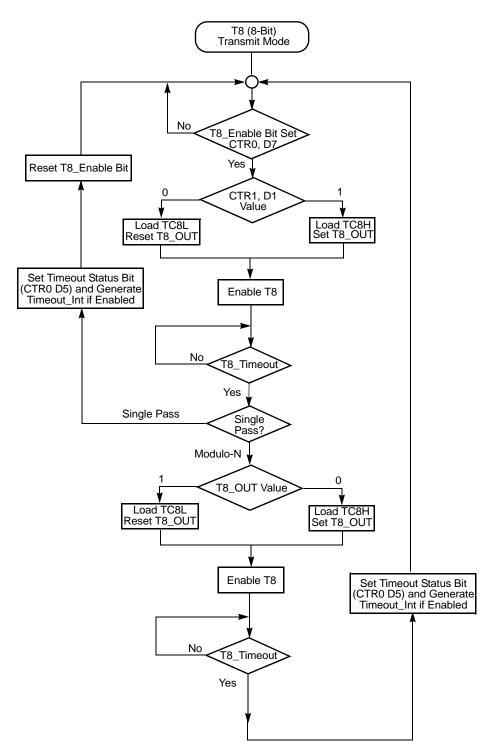


Figure 19. Transmit Mode Flowchart



into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFH (see Figure 23 and Figure 24).



Figure 23. Demodulation Mode Count Capture Flowchart



57

#### SMR(0F)0BH



\* Default after Power On Reset or Watch-Dog Reset

\* \* Default setting after Reset and Stop Mode Recovery

\* \* \* At the XOR gate input

\* \* \* \* Default setting after reset. Must be 1 if using a crystal or resonator clock source.

#### Figure 33. STOP Mode Recovery Register

#### SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.



69

#### CTR2(0D)02H

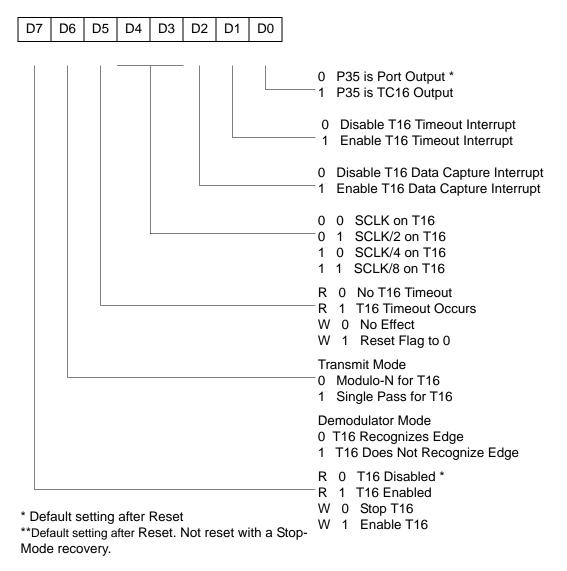
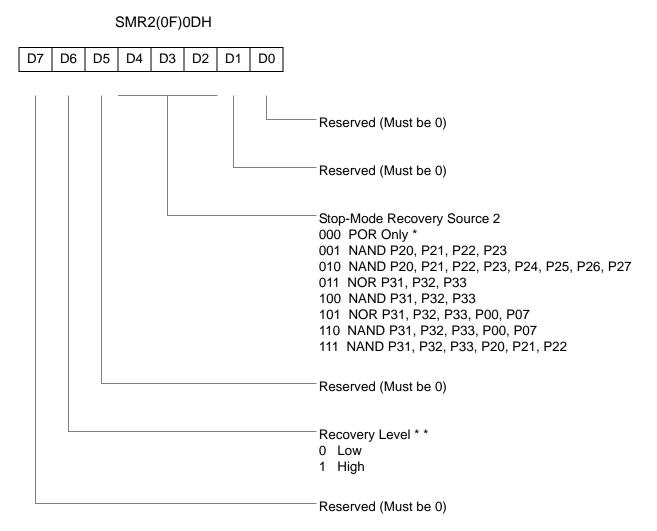


Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)





Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

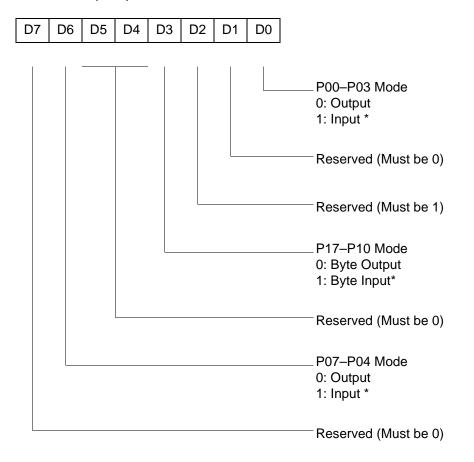
\* Default setting after reset. Not reset with a Stop Mode recovery.

\* \* At the XOR gate input

#### Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)



#### R248 P01M(F8H)



\* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

#### Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)





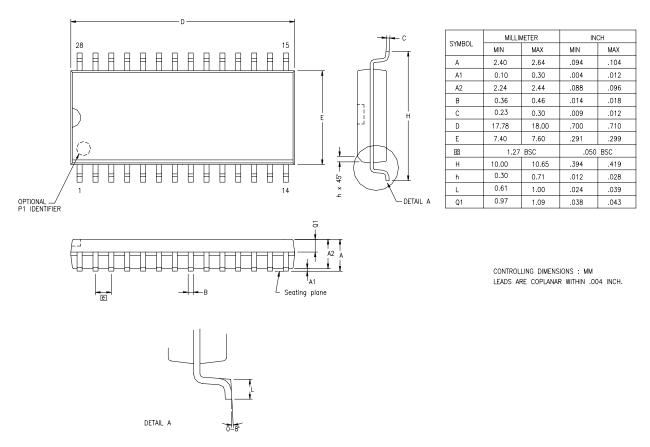


Figure 62. 28-Pin SOIC Package Diagram

ZGP323H Product Specification



## **Ordering Information**

#### 32KB Standard Temperature: 0° to +70°C

	•		
Part Number	Description	Part Number	Description
ZGP323HSH4832C	48-pin SSOP 32K OTP	ZGP323HSS2832C	28-pin SOIC 32K OTP
ZGP323HSP4032C	40-pin PDIP 32K OTP	ZGP323HSH2032C	20-pin SSOP 32K OTP
ZGP323HSK2832E	28-pin CDIP 32K OTP	ZGP323HSK2032E	20-pin CDIP 32K OTP
ZGP323HSK4032E	40-pin CDIP 32K OTP	ZGP323HSP2032C	20-pin PDIP 32K OTP
ZGP323HSH2832C	28-pin SSOP 32K OTP	ZGP323HSS2032C	20-pin SOIC 32K OTP
ZGP323HSP2832C	28-pin PDIP 32K OTP		

#### 32KB Extended Temperature: -40° to +105°C

	•		
Part Number	Description	Part Number	Description
ZGP323HEH4832C	48-pin SSOP 32K OTP	ZGP323HES2832C	28-pin SOIC 32K OTP
ZGP323HEP4032C	40-pin PDIP 32K OTP	ZGP323HEH2032C	20-pin SSOP 32K OTP
ZGP323HEH2832C	28-pin SSOP 32K OTP	ZGP323HEP2032C	20-pin PDIP 32K OTP
ZGP323HEP2832C	28-pin PDIP 32K OTP	ZGP323HES2032C	20-pin SOIC 32K OTP

32KB Automotive Temperature: -40° to +125°C				
Part Number	Description	Part Number	Description	
ZGP323HAH4832C	48-pin SSOP 32K OTP	ZGP323HAS2832C	28-pin SOIC 32K OTP	
ZGP323HAP4032C	40-pin PDIP 32K OTP	ZGP323HAH2032C	20-pin SSOP 32K OTP	
ZGP323HAH2832C	28-pin SSOP 32K OTP	ZGP323HAP2032C	20-pin PDIP 32K OTP	
ZGP323HAP2832C	28-pin PDIP 32K OTP	ZGP323HAS2032C	20-pin SOIC 32K OTP	
Replace C with G for Lead-Free Packaging				

# ZGP323H Z8<sup>®</sup> OTP Microcontroller with IR Timers



T8\_Capture\_LO 32 register file 30 expanded 26 register pointer 29 detail 31 reset pin function 25 resets and WDT 63 S SCLK circuit 58 single-pass mode T16\_OUT 47 T8\_OUT 43 stack 31 standard test conditions 10 standby modes 1 stop instruction, counter/timer 54 stop mode recovery 2 register 61 source 59 stop mode recovery 2 61 stop mode recovery register 57 Т T16 transmit mode 46 T16\_Capture\_HI 32 T8 transmit mode 40 T8\_Capture\_HI 32 test conditions, standard 10 test load diagram 10 timing diagram, AC 16 transmit mode flowchart 41 V VCC 5 voltage brown-out/standby 64 detection and flags 65 voltage detection register 71 W watch-dog timer mode registerwatch-dog timer mode register 62 time select 63

X XTAL1 5 XTAL1 pin function 18 XTAL2 5 XTAL2 pin function 18