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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323heh2004g

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Table 3. Power Connections

Connection	Circuit	Device	
Power	V _{CC}	V _{DD}	
Ground	GND	V _{SS}	



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram





Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.







Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 4.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V _{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V _{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output



	T _A = -40°C to +105°C								
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions	Notes	
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA		
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$		
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA		
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV			
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V			
IIL	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled		
R _{PU}	Pull-up Resistance	2.0V	200.0		700.0	KΩ	V _{IN} = 0V; Pullups selected by mask		
		3.6V	50.0		300.0	KΩ	option		
		5.0V	25.0		175.0	KΩ	_		
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0V, V_{CC}$		
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2	
		3.6V		5	10	mA	at 8.0 MHz	1, 2	
		5.5V		10	15	mA	at 8.0 MHz	1, 2	
I _{CC1}	Standby Current	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6	
	(HALT Mode)	3.6V		0.8	2.0	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6	
		5.5V		1.3	3.2	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6	
I _{CC2}	Standby Current (Stop	2.0V		1.6	12	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3	
	Mode)	3.6V		1.8	15	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3	
		5.5V		1.9	18	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3	
		2.0V		5	30	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3	
		3.6V		8	40	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3	
		5.5V		15	60	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3	
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4	
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.		
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V			
V _{HVD}	Vcc High Voltage Detection			2.7		V			

Table 10. GP323HE DC Characteristics (Continued)

Notes:

1. All outputs unloaded, inputs at rail.

2. CL1 = CL2 = 100 pF.

3. Oscillator stopped.

4. Oscillator stops when $V_{\mbox{\scriptsize CC}}$ falls below $V_{\mbox{\scriptsize BO}}$ limit.

 It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VCC and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

6. Comparator and Timers are on. Interrupt disabled.

7. Typical values shown are at 25 degrees C.





Figure 10. Port 1 Configuration

Port 2 (P27-P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.







Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—



Field	Bit Position		Value	Description
T16_Enable	7	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W		Transmit Mode
			0*	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize
				Edge
Time_Out	5	R	0*	No Counter Timeout
			1	Counter Timeout
				Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	43	R/W	00**	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	1-	R/W	0*	Disable Timeout Int.
				Enable Timeout Int.
P35_Out	0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Table 17. CTR2(D)02H: Counter/Timer16 Control Register

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.



In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 47.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03H

Table 18 lists and briefly describes the fields for this register. This register allows the T_8 and T_{16} counters to be synchronized.

Field	Bit Position		Value	Description
T ₁₆ Enable	7	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T ₈ Enable	-6	R	0*	Counter Disabled
-		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	5	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode

Table 18. CTR3 (D)03H: T8/T16 Control Register



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When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.



Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.

ZGP323H Product Specification



Caution: Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFFH. Transition from 0 to FFFFH is not a timeout condition.







Figure 27. T16_OUT in Modulo-N Mode

T16 DEMODULATION Mode

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).





Figure 28. Ping-Pong Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.





The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.



Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XORgate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/ TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address OBH.

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Table 22. Stop Mode Recovery Source

SMR:432			Operation		
D4	D3	D2	Description of Action		
0	0	0	POR and/or external reset recovery		
0	0	1	Reserved		
0	1	0	P31 transition		
0	1	1	P32 transition		
1	0	0	P33 transition		
1	0	1	P27 transition		
1	1	0	Logical NOR of P20 through P23		
1	1	1	Logical NOR of P20 through P27		

Note: Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 61 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 TpC.

Note: This bit must be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).



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Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8[®] CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



* Default setting after reset

Figure 37. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 23.



R248 P01M(F8H)



* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)







A1	 ¥↓ ↓ δ
↓	A2 A

		MILLIMETER	2	INCH		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
А	1.73	1.86	1.99	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.78	0.066	0.068	0.070
В	0.25		0.38	0.010		0.015
С	0.09	-	0.20	0.004	0.006	0.008
D	10.07	10.20	10.33	0.397	0.397 0.402	
E	5.20	5.30	5.38	0.205	0.209	0.212
е	0.65 TYP				0.0256 TYF)
н	7.65	7.80	7.90	0.301	0.307	0.311
L	0.63	0.75	0.95	0.025	0.030	0.037

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<u>DETAIL 'A'</u>

0-8

Figure 65. 28-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
В	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
С	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100_TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
2	1.52	2.20	060	000

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Figure 66. 40-Pin PDIP Package Diagram



Example



ZGP323H Z8[®] OTP Microcontroller with IR Timers



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