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Zilog - ZGP323HEH2008C00TR Datasheet



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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323heh2008c00tr

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Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Docume	ent
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Date	Revision Level	Section	Description	Page #
December 2004	02	Changed low power of deleted mask option and 10. Added new T Table 11 and change	consumption, STOP and HALT mode current values, note, clarified temperature ranges in Tables 6 and 8 ables 9 and 10. Also added Characterization data to d Program/Erase Endurance value in Table 12.	1,2,10 11,12, 13,14, 15
		Removed Preliminar	/ designation	All
March 2005	03	Minor change to Tabl pin CDIP parts in the	e 9 Electrical Characteristics. Added 20, 28 and 40- Ordering Section.	11,90



	T _Δ = -40°C to +105°C							
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V		
IIL	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled	
R _{PU}	Pull-up Resistance	2.0V	200.0		700.0	KΩ	V _{IN} = 0V; Pullups selected by mask	
		3.6V	50.0		300.0	KΩ	option	
		5.0V	25.0		175.0	KΩ	_	
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0V, V_{CC}$	
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I _{CC1}	Standby Current	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
	(HALT Mode)	3.6V		0.8	2.0	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I _{CC2}	Standby Current (Stop	2.0V		1.6	12	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
	Mode)	3.6V		1.8	15	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
		5.5V		1.9	18	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		2.0V		5	30	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		3.6V		8	40	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		5.5V		15	60	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V		
V _{HVD}	Vcc High Voltage Detection			2.7		V		

Table 10. GP323HE DC Characteristics (Continued)

Notes:

1. All outputs unloaded, inputs at rail.

2. CL1 = CL2 = 100 pF.

3. Oscillator stopped.

4. Oscillator stops when V_{CC} falls below V_{BO} limit.

 It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VCC and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

6. Comparator and Timers are on. Interrupt disabled.

7. Typical values shown are at 25 degrees C.





Expanded Reg. Bank 0/Group 15" Register Pointer [7] [5] [4] [3] [2] [10] Working Register Group Pointer Bank Pointer FF FP Bank Pointer FF FP Bank Pointer FF FF FF FF Bank Pointer FF FF		Z8 [®] Standard Control Registers						۱
Register Pointer FF SPL FE U <thu< th=""> <thu< th=""> U U</thu<></thu<>			Expanded Reg. Bank 0/Group 15	** D7 D6 D	5 D4	D3	D2[D1 D0
Register Pointer Image: Construction of the second of					1	ii		
Register Pointer T D								
Register Pointer U <			FD RP		0	0	0	
7 6 5 4 3 2 1 0		Register Pointer	FC FLAGS					
Working Register Group Pointer Expanded Register Bank Pointer FA IRQ 0 <td< td=""><td>7</td><td>7 6 5 4 3 2 1 0</td><td>FB IMB</td><td></td><td></td><td></td><td></td><td></td></td<>	7	7 6 5 4 3 2 1 0	FB IMB					
Working Register Expanded Register F3 F3 <td></td> <td></td> <td>FA IBO</td> <td></td> <td>0</td> <td>0</td> <td>0</td> <td></td>			FA IBO		0	0	0	
Ordop Pollies Dirth Antes PB PD1M 1 0 <t< td=""><td>Working Regist</td><td>ter Expanded Regist</td><td>er F9 IPR</td><td></td><td></td><td></td><td></td><td></td></t<>	Working Regist	ter Expanded Regist	er F9 IPR					
F7 P3M 0	Group Pointer	Dank Fonter	F8 P01M	1 1 0	0	1	1	1 1
F6 P2M 1			F7 P3M		0	0	0	0 0
F5 Reserved I			F6 P2M	1 1 1	1	1	1	1 1
F4 Reserved F3 Reserved F3 Reserved F4 Reserved F5 Reserved F6 F6 F6 F7 F7 F8 F8 F8 F7 F8 F8 F8 F9 F8 <td></td> <td></td> <td>F5 Reserved</td> <td></td> <td></td> <td>$\frac{1}{1}$</td> <td>ii l</td> <td></td>			F5 Reserved			$\frac{1}{1}$	ii l	
Fig Reserved U			F4 Reserved			11	U	
File (Bank 0)** File (Bank 0)** File (Bank 0)** File Reserved U			F3 Reserved		U U	U	U	
Findersterning (bank 0)** Findersterning (bank 0)**			F2 Reserved		U U	U	Ŭ	
F0 Reserved U	FF	Register File (Bank 0)	F1 Reserved		U U	Ŭ	U	υυ
Image: Second State Sta	Fo		F0 Reserved		U U	Ŭ	U	
Figure 1 Expanded Reg. Bank F/Group 0** (F) 0F WD 1MR (F) 0F WD 1MR (F) 0F Reserved (F) 0F Reserved (F) 0R Reserved						1-1	~	
Image: constraint of the second state stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the			Expanded Reg. Bank F/Group 0*	*				
(F) 0E Reserved 0			(F) 0F WDTMR	U U O	0	1	1	0 1
F) OD SMR2 0			(F) 0E Reserved			Π		
7F F			* (F) 0D SMR2	0 0 0	0	0	0	0 0
7F (F) 0B SMR U 0 1 0 0 0 U 0 (F) 0B Reserved (F) 0B Reserved (F) 0B Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved </td <td>_</td> <td></td> <td>(F) 0C Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	_		(F) 0C Reserved					
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0F (F) 07 Reserved (F) 06 Reserved (F) 06 Reserved (F) 05 Reserved (F) 07 Reserved (F) 04 Reserved (F) 07 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 04 Reserved (F) 04 Reserved			(F) 08 Reserved					
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0F 0F <td< td=""><td></td><td></td><td>(F) 06 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 06 Reserved					
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00 Image: constraint of the set with a Stop-Mode Recovery 1 <td>0F</td> <td><u> </u>₩/</td> <td>(F) 04 Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	0F	<u> </u> ₩/	(F) 04 Reserved					
Expanded Reg. Bank 0/Group (0) (F) 02 Reserved 1	00		(F) 03 Reserved					
Expanded Reg. Bank 0/Group (0) (0) 03 P3 0 (0) 02 P2 U (0) 01 P1 U (0) 01 P1 U (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** Di 03 CTR3 0 ** (D) 04 TC8L 0 0 0 ** (D) 03 CTR3 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 01 CTR1 0 ** (D) 00 CTR0 0		\backslash	(F) 02 Reserved					
Expanded Reg. Bank 0/Group (0) (0) 03 P3 0 U (0) 02 P2 U * (0) 01 P1 U (0) 00 P0 U (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** His 5 Is not reset with a Stop-Mode Recovery ** (D) 04 TC8L 0 <			(F) 01 Reserved					
(0) 03 P3 0 U (0) 02 P2 U * (0) 01 P1 U (0) 00 P0 U * (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ^* (D) 05 TC8H 0	Expa	anded Reg. Bank 0/Group (0)	(F) 00 PCON	1 1 1	1	1	1	1 0
(0) 03 P3 0			Expanded Reg. Bank D/Group 0					
(b) 02 P2 U * (0) 01 P1 U (0) 00 P0 U U = Unknown * * All addresses are in hexadecimal * ↑ Bit 5 Is not reset with a Stop-Mode Recovery ** (D) 04 ** (D) 05 ** (D) 06 ** (D) 07 ** (D) 08 ** (D) 08 ** (D) 07 ** (D) 08 ** (D) 07 ** (D) 06 ** (D) 06 ** (D) 07 ** (D) 06 ** (D) 07 ** (D) 08 ** (D) 08 ** (D) 04 ** (D) 05 ** (D) 04 ** (D) 03 ** (D) 02 ** (D) 01 ** (D) 01 ** (D) 01 ** (D) 01 ** (D) 02 ** (D) 01 (D) 0	(0) 03 P3	U U		UUI	υ	U	U	υn
* (0) 01 P1 U (0) 01 P1 U (0) 00 P0 U * (D) 00 A LO8 0<	(0) 02 P2	U	* (D) 0B HI8	0 0 0	0	0	0	0 0
(b) 01 1 1 0	* (0) 01 P1	U	* (D) 0A 08	0 0 0	0	0	0	0 0
(0) 00 P0 U U = Unknown (D) 08 LO16 0	(0) 011 1	<u> </u>	* (D) 09 HI16	0 0 0	0	0	0	0 0
U = Unknown * (D) 07 TC16H 0 <td>(0) 00 P0</td> <td>U</td> <td>* (D) 08 LO16</td> <td>0 0 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td>	(0) 00 P0	U	* (D) 08 LO16	0 0 0	0	0	0	0 0
* Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ^* All addresses are in hexadecimal ^* Is not reset with a Stop-Mode Recovery, except Bit 0 ^* Bit 5 Is not reset with a Stop-Mode Recovery ^* Bit 5 Is not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Diss 5,4,3,2 not reset with a Stop-Mode Recovery ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery ^* CD 00 CTR1 0 0 ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery ^* CD 00 CTR0 ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery			* (D) 07 TC16H	0 0 0	0	0	0	0 0
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⁺ Is not reset with a Stop-Mode Recovery, except Bit 0 ⁺ 1bit 5 Is not reset with a Stop-Mode Recovery ⁺ (D) 04 TC8L ⁻ 0 0 0 0 0 0 0 0 0 0 0 ⁺ (D) 03 CTR3 ⁻ 0 0 0 0 1 1 1 1 1 ⁺ 1 ⁺ (D) 02 CTR2 ⁻ 0 0 0 0 0 0 0 0 0 ⁻ 1 1 1 1 ⁺	** All addresses are in beyade	ecimal	* (D) 05 TC8H	0 0 0	0	0	0	0 0
	↑ Is not reset with a Stop-Mo	de Recovery, except Bit 0	* (D) 04 TC8L	0 0 0	0	0	0	0 0
[↑] ↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery [↑] ↑↑↑ [↑] ↑↑↑ [↑] ↑↑↑ [↑] ↑↑↑↑ [↑] ↑↑↑ [↑] ↑↑ [↑] ↑ [↑]	↑↑ Bit 5 Is not reset with a Sto	p-Mode Recovery	1↑ (D) 03 CTR3	0 0 0	1	1	1	1 1
^{↑↑↑↑} Bits 5 and 4 not reset with a Stop-Mode Recovery ^{↑↑↑↑↑} (D) 01 CTR1 (D) 01 CTR1 (D) 0 0 0 0 0 0 0 0 (D) 01 CTR1 (D) 00 CTR0 (D)	↑↑↑ Bits 5,4,3.2 not reset with	a Stop-Mode Recoverv	↑↑↑ (D) 02 CTR2	0 0 0	0	0	0	0 0
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery ↑↑↑↑↑↓ (D) 00 CTR0 0 0 0 0 0 0 0 0 0 0	↑↑↑↑ Bits 5 and 4 not reset with	a Stop-Mode Recovery	↑↑↑↑ (D) 01 CTR1	0 0 0	0	0	0	0 0
	↑↑↑↑↑ Bits 5,4,3,2,1 not reset wit	th a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	0 0 0	0	0	0	0 0

Figure 15. Expanded Register File Architecture







Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



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Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position		Description	
T16_Data_LO	[7:0]	R/W	Data	

Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position		Description	
T8_Level_HI	[7:0]	R/W	Data	

Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

Table 15. CTR0(D)00H Counter/Timera	3 Control Register
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Field	Bit Position		Value	Description
T8_Enable	7	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W	0*	Modulo-N
-			1	Single Pass
Time_Out	5	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	43	R/W	0 0**	SCLK
			0 1	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt



Field	Bit Position		Value	Description
T16_Enable	7	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W		Transmit Mode
			0*	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize
				Edge
Time_Out	5	R	0*	No Counter Timeout
			1	Counter Timeout
				Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	43	R/W	00**	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	1-	R/W	0*	Disable Timeout Int.
				Enable Timeout Int.
P35_Out	0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Table 17. CTR2(D)02H: Counter/Timer16 Control Register

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.



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During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Interrupts

The ZGP323H features six different interrupts (Table 19). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 19) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 59.



Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T _{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	Т8	8,9	Internal
IRQ5	LVD	10,11	Internal

Table 19. Interrupt Types, Sources, and Vectors

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All ZGP323H interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 20.

IRQ		Interrupt Edge			
D7	D6	IRQ2 (P31)	IRQ0 (P32)		
0	0	F	F		
0	1	F	R		
1	0	R	F		
1 1 R/F R/F					
Note: F = Falling Edge; R = Rising Edge					

Table 20. IRQ Register







Figure 35. Stop Mode Recovery Source

ZGP323H Product Specification



Table 22. Stop Mode Recovery Source

SMR:432			Operation	
D4 D3 D2		D2	Description of Action	
0	0	0	POR and/or external reset recovery	
0	0	1	Reserved	
0	1	0	P31 transition	
0	1	1	P32 transition	
1	0	0	P33 transition	
1	0	1	P27 transition	
1	1	0	Logical NOR of P20 through P23	
1	1	1	Logical NOR of P20 through P27	

Note: Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 61 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 TpC.

Note: This bit must be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).



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Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8[®] CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



* Default setting after reset

Figure 37. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 23.



Table 23. Watch-Dog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.



* CLR1 and CLR2 enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-

Figure 38. Resets and WDT



LVD(0D)0CH



* Default setting after reset.

Figure 43. Voltage Detection Register

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.



R250 IRQ(FAH)





Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



* Default setting after reset

* * Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)



R252 Flags(FCH)



Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)



R254 SPH(FEH)



Figure 56. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)



Stack Pointer Low Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFH: Read/Write)

Package Information

Package information for all versions of ZGP323H is depicted in Figures 59 through Figure 68.





Figure 67. 40-Pin CDIP Package Diagram

ZGP323H Product Specification



Ordering Information

32KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4832C	48-pin SSOP 32K OTP	ZGP323HSS2832C	28-pin SOIC 32K OTP
ZGP323HSP4032C	40-pin PDIP 32K OTP	ZGP323HSH2032C	20-pin SSOP 32K OTP
ZGP323HSK2832E	28-pin CDIP 32K OTP	ZGP323HSK2032E	20-pin CDIP 32K OTP
ZGP323HSK4032E	40-pin CDIP 32K OTP	ZGP323HSP2032C	20-pin PDIP 32K OTP
ZGP323HSH2832C	28-pin SSOP 32K OTP	ZGP323HSS2032C	20-pin SOIC 32K OTP
ZGP323HSP2832C	28-pin PDIP 32K OTP		

32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4832C	48-pin SSOP 32K OTP	ZGP323HES2832C	28-pin SOIC 32K OTP
ZGP323HEP4032C	40-pin PDIP 32K OTP	ZGP323HEH2032C	20-pin SSOP 32K OTP
ZGP323HEH2832C	28-pin SSOP 32K OTP	ZGP323HEP2032C	20-pin PDIP 32K OTP
ZGP323HEP2832C	28-pin PDIP 32K OTP	ZGP323HES2032C	20-pin SOIC 32K OTP

32KB Automotive Temperature: -40° to +125°C			
Part Number	Description	Part Number	Description
ZGP323HAH4832C	48-pin SSOP 32K OTP	ZGP323HAS2832C	28-pin SOIC 32K OTP
ZGP323HAP4032C	40-pin PDIP 32K OTP	ZGP323HAH2032C	20-pin SSOP 32K OTP
ZGP323HAH2832C	28-pin SSOP 32K OTP	ZGP323HAP2032C	20-pin PDIP 32K OTP
ZGP323HAP2832C	28-pin PDIP 32K OTP	ZGP323HAS2032C	20-pin SOIC 32K OTP
Replace C with G for Lead-Free Packaging			





4KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4804C	48-pin SSOP 4K OTP	ZGP323HSS2804C	28-pin SOIC 4K OTP
ZGP323HSP4004C	40-pin PDIP 4K OTP	ZGP323HSH2004C	20-pin SSOP 4K OTP
ZGP323HSH2804C	28-pin SSOP 4K OTP	ZGP323HSP2004C	20-pin PDIP 4K OTP
ZGP323HSP2804C	28-pin PDIP 4K OTP	ZGP323HSS2004C	20-pin SOIC 4K OTP

4KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4804C	48-pin SSOP 4K OTP	ZGP323HES2804C	28-pin SOIC 4K OTP
ZGP323HEP4004C	40-pin PDIP 4K OTP	ZGP323HEH2004C	20-pin SSOP 4K OTP
ZGP323HEH2804C	28-pin SSOP 4K OTP	ZGP323HEP2004C	20-pin PDIP 4K OTP
ZGP323HEP2804C	28-pin PDIP 4K OTP	ZGP323HES2004C	20-pin SOIC 4K OTP

4KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description	
ZGP323HAH4804C	48-pin SSOP 4K OTP	ZGP323HAS2804C	28-pin SOIC 4K OTP	
ZGP323HAP4004C	40-pin PDIP 4K OTP	ZGP323HAH2004C	20-pin SSOP 4K OTP	
ZGP323HAH2804C	28-pin SSOP 4K OTP	ZGP323HAP2004C	20-pin PDIP 4K OTP	
ZGP323HAP2804C	28-pin PDIP 4K OTP	ZGP323HAS2004C	20-pin SOIC 4K OTP	
Replace C with G for Lead-Free Packaging				

Additional Components				
Part Number	Description	Part Number	Description	
ZGP323ICE01ZEM (For 3.6V Emulation only)	Emulator/programmer	ZGP32300100ZPR (Ethernet)	Programming system	
		ZGP32300200ZPR (USB)	Programming system	



Example

