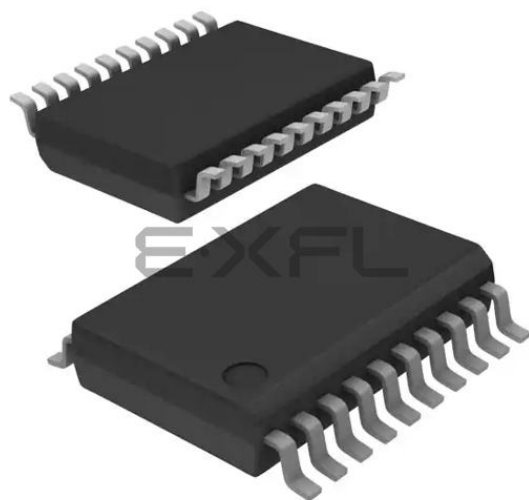




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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323heh2032c



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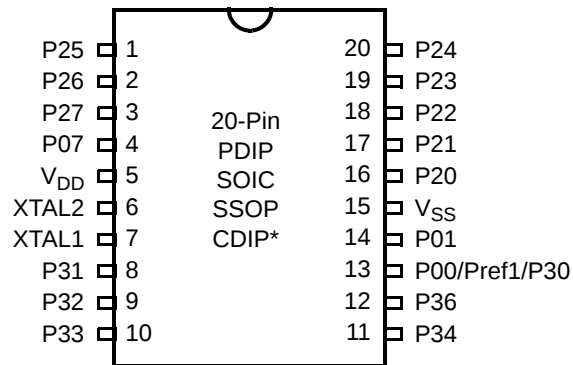


Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 4. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V _{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V _{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output

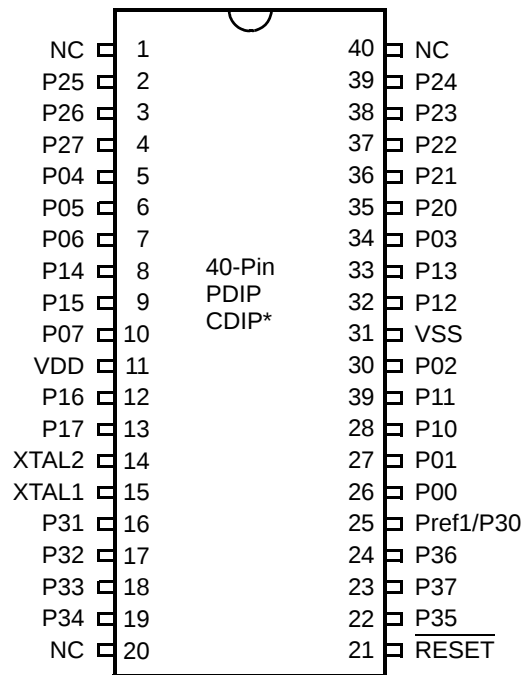


Figure 5. 40-Pin PDIP/CDIP* Pin Configuration

► **Note:** *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

Table 11. GP323HA DC Characteristics

$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$								
Symbol	Parameter	V_{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V_{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-5.5	$0.8 V_{CC}$		$V_{CC}+0.3$	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-5.5	$V_{SS}-0.3$		0.4	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-5.5	$0.7 V_{CC}$		$V_{CC}+0.3$	V		
V_{IL}	Input Low Voltage	2.0-5.5	$V_{SS}-0.3$		$0.2 V_{CC}$	V		
V_{OH1}	Output High Voltage	2.0-5.5	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{mA}$	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	$V_{CC}-0.8$			V	$I_{OH} = -7\text{mA}$	
V_{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0\text{mA}$	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	$I_{OL} = 10\text{mA}$	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-5.5	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC} Pull-ups disabled	
R_{PU}	Pull-up Resistance	2.0V	200		700	$\text{K}\Omega$	$V_{IN} = 0\text{V}$; Pullups selected by mask option	
		3.6V	50		300	$\text{K}\Omega$		
		5.0V	25		175	$\text{K}\Omega$		
I_{OL}	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC}	
I_{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I_{CC1}	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	$V_{IN} = 0\text{V}$, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	$V_{IN} = 0\text{V}$, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	$V_{IN} = 0\text{V}$, Clock at 8.0MHz	1, 2, 6
I_{CC2}	Standby Current (Stop Mode)	2.0V		1.6	15	μA	$V_{IN} = 0\text{V}$, V_{CC} WDT not Running	3
		3.6V		1.8	20	μA	$V_{IN} = 0\text{V}$, V_{CC} WDT not Running	3
		5.5V		1.9	25	μA	$V_{IN} = 0\text{V}$, V_{CC} WDT not Running	3
		2.0V		5	30	μA	$V_{IN} = 0\text{V}$, V_{CC} WDT is Running	3
		3.6V		8	40	μA	$V_{IN} = 0\text{V}$, V_{CC} WDT is Running	3
		5.5V		15	60	μA	$V_{IN} = 0\text{V}$, V_{CC} WDT is Running	3
I_{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V_{BO}	V_{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V_{LVD}	V_{CC} Low Voltage Detection			2.4		V		

AC Characteristics

Figure 8 and Table 13 describe the Alternating Current (AC) characteristics.

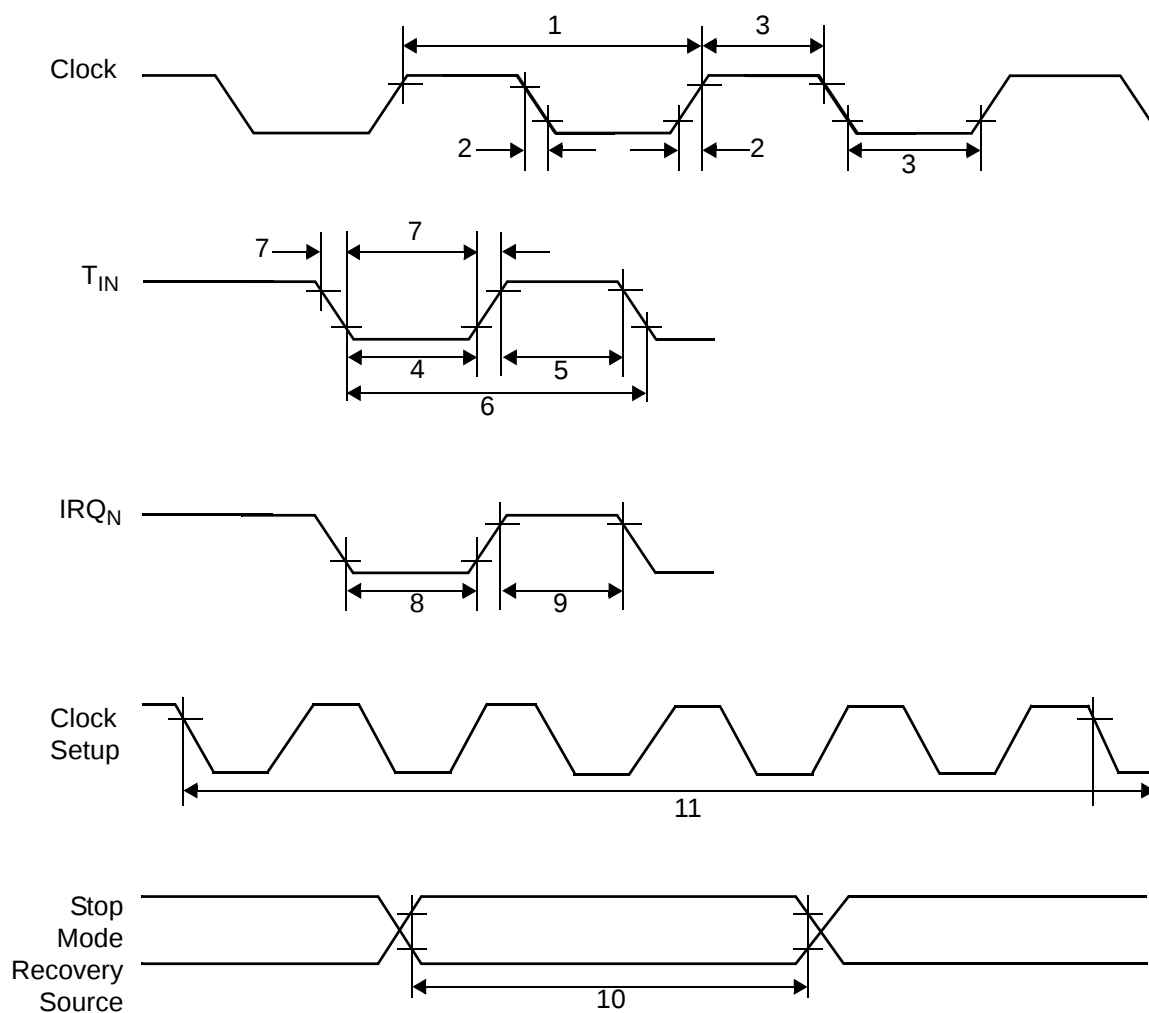


Figure 8. AC Timing Diagram

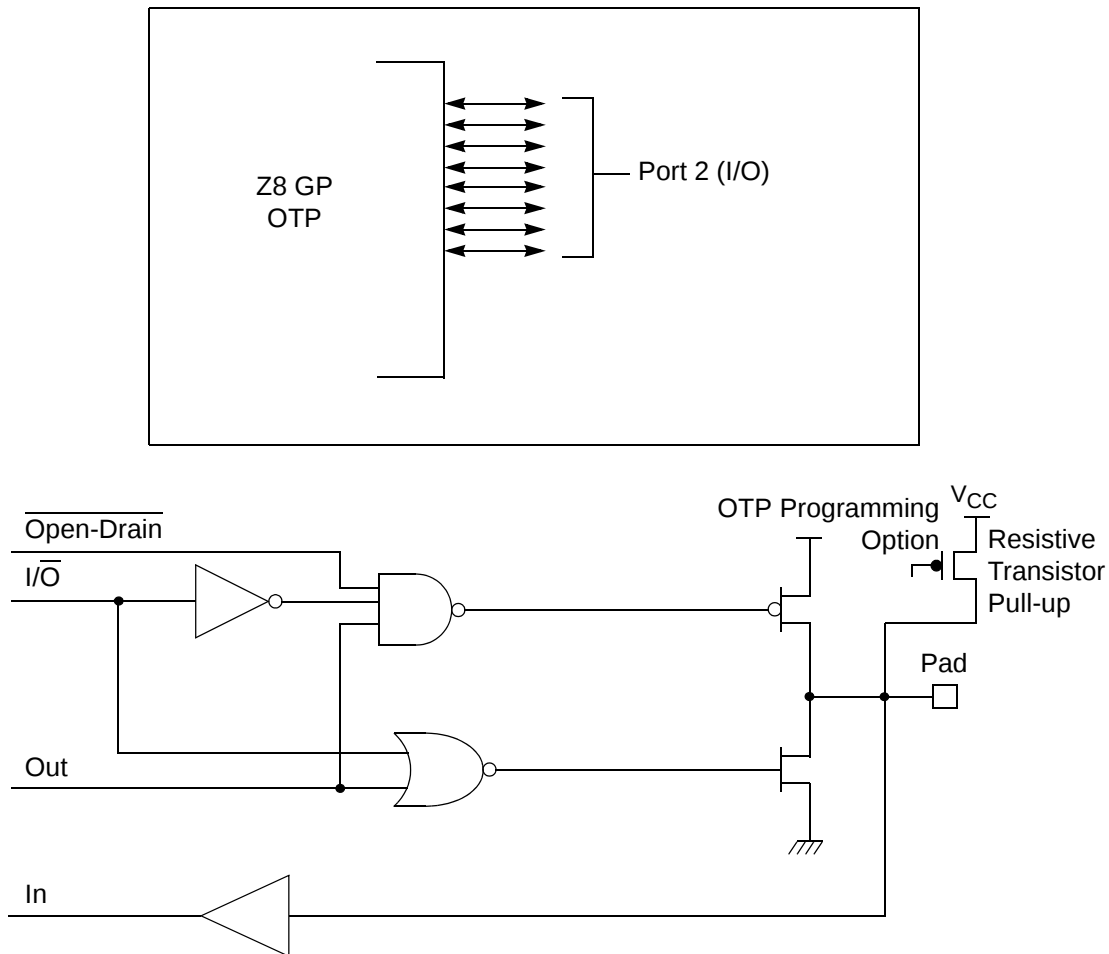


Figure 11. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

Table 16. CTR1(0D)01H T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-----	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/ Demodulator_Input	-6-----	R/W	0*	Transmit Mode
			1	Port Output
				T8/T16 Output
			0*	Demodulation Mode
			1	P31
				P20
T8/T16_Logic/ Edge_Detect	--54----	R/W		Transmit Mode
			00**	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 47.

Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

CTR3 T8/T16 Control Register—CTR3(D)03H

Table 18 lists and briefly describes the fields for this register. This register allows the T₈ and T₁₆ counters to be synchronized.

Table 18. CTR3 (D)03H: T8/T16 Control Register

Field	Bit Position		Value	Description
T ₁₆ Enable	7-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
T ₈ Enable	-6-----	R	0*	Counter Disabled
		R	1	Counter Enabled
		W	0	Stop Counter
		W	1	Enable Counter
Sync Mode	--5-----	R/W	0**	Disable Sync Mode
			1	Enable Sync Mode

Table 18. CTR3 (D)03H: T8/T16 Control Register (Continued)

Field	Bit Position		Value	Description
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).

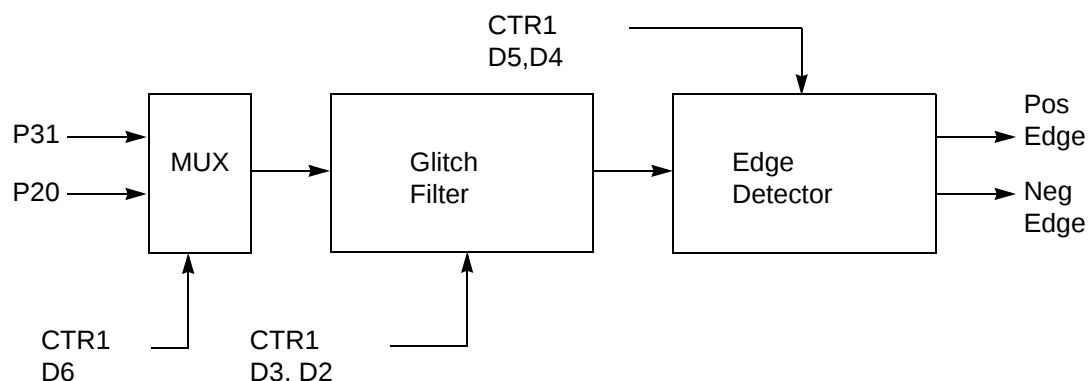


Figure 18. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.

► **Note:** The letter *h* denotes hexadecimal values.

Transition from 0 to FF_h is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.

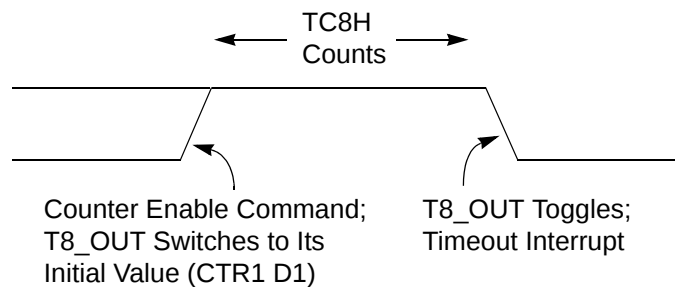


Figure 21. T8_OUT in Single-Pass Mode

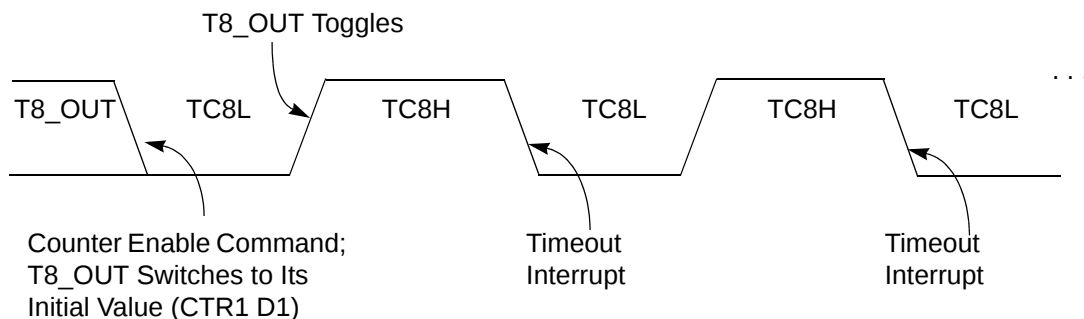


Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FF_h. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.

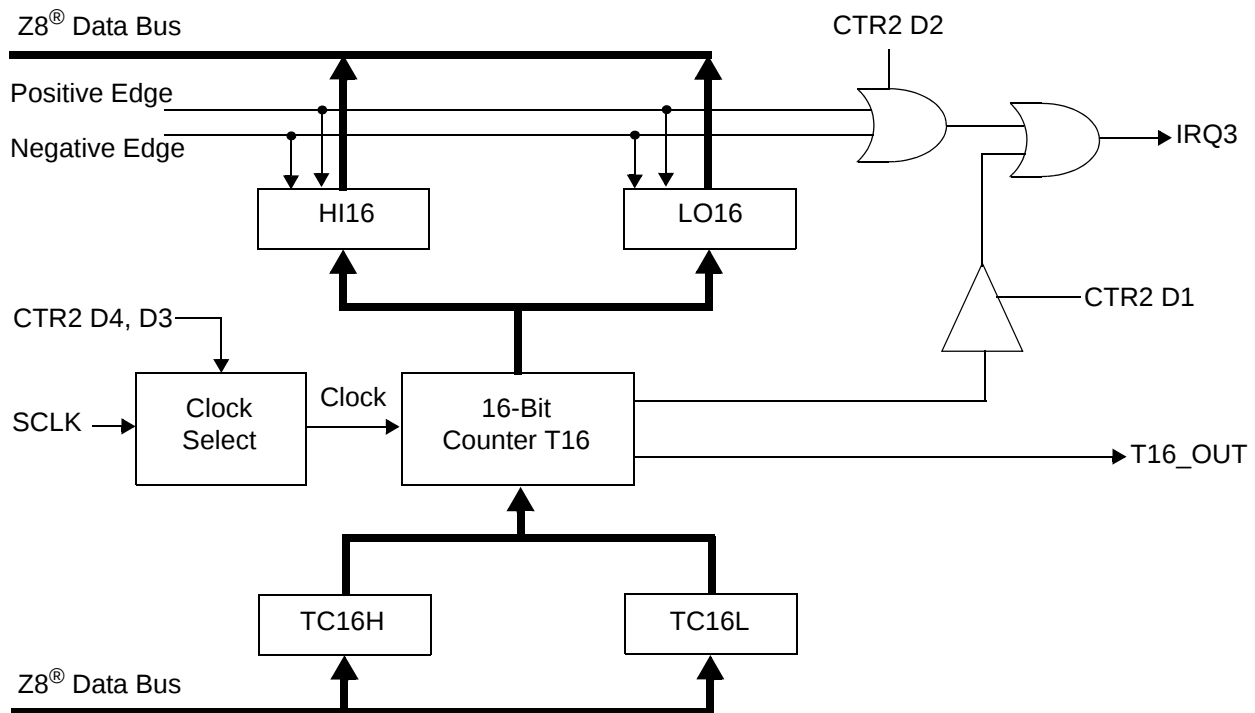


Figure 25. 16-Bit Counter/Timer Circuits

► **Note:** Global interrupts override this function as described in “Interrupts” on page 50.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.

Table 19. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T _{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LVD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All ZGP323H interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

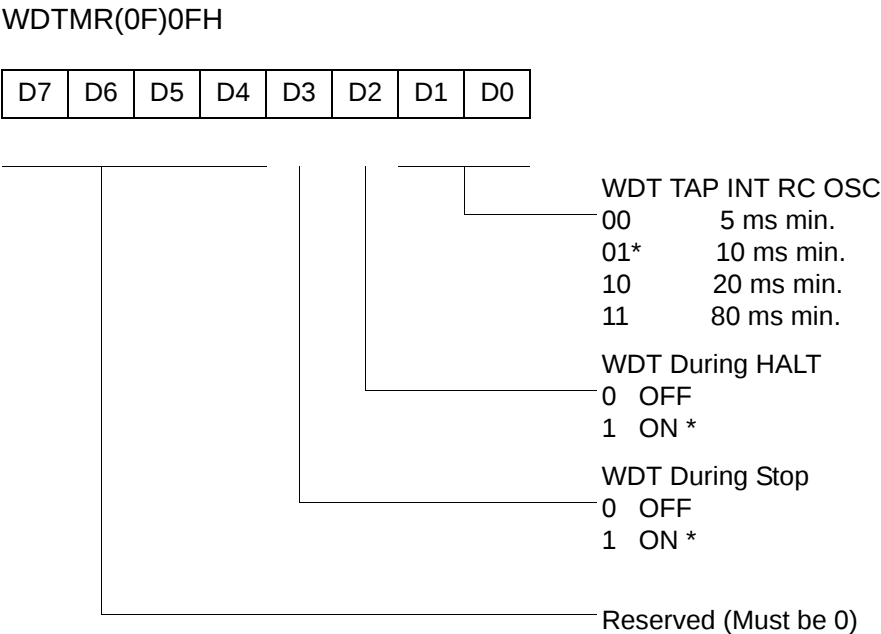
An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 20.

Table 20. IRQ Register

IRQ		Interrupt Edge	
D7	D6	IRQ2 (P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

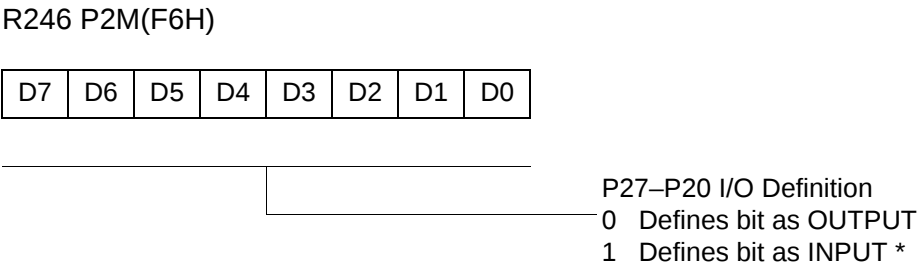
Note: F = Falling Edge; R = Rising Edge



* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

Standard Control Registers



* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 48. Port 2 Mode Register (F6H: Write Only)



R249 IPR(F9H)

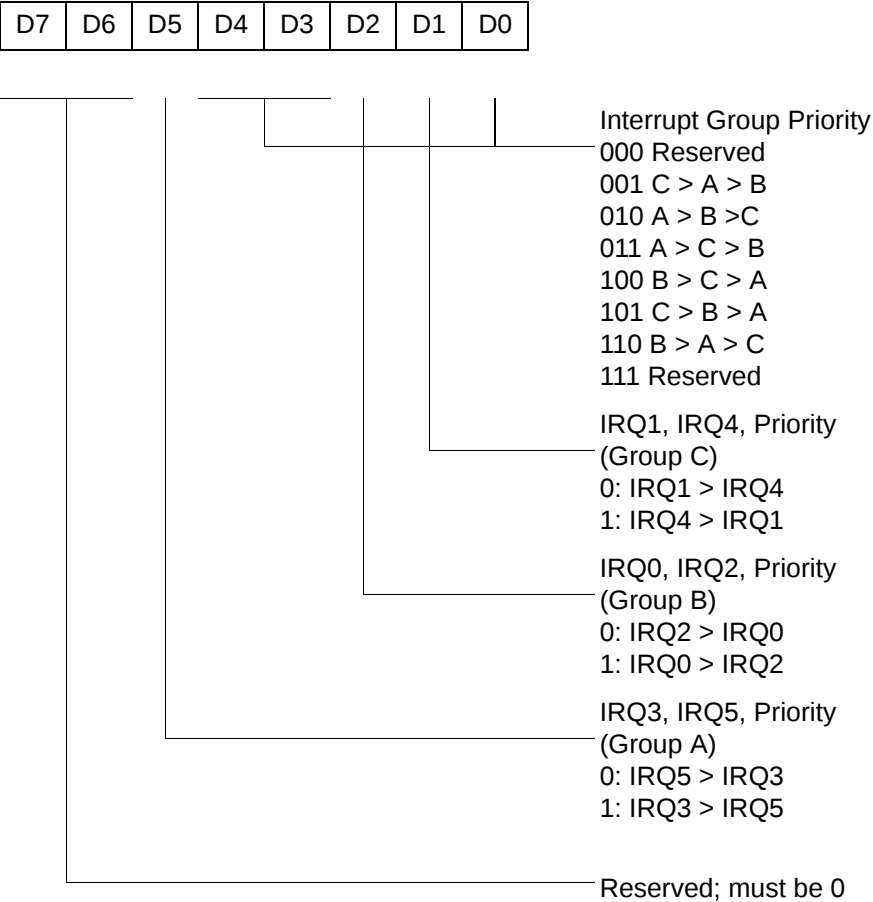


Figure 51. Interrupt Priority Register (F9H: Write Only)

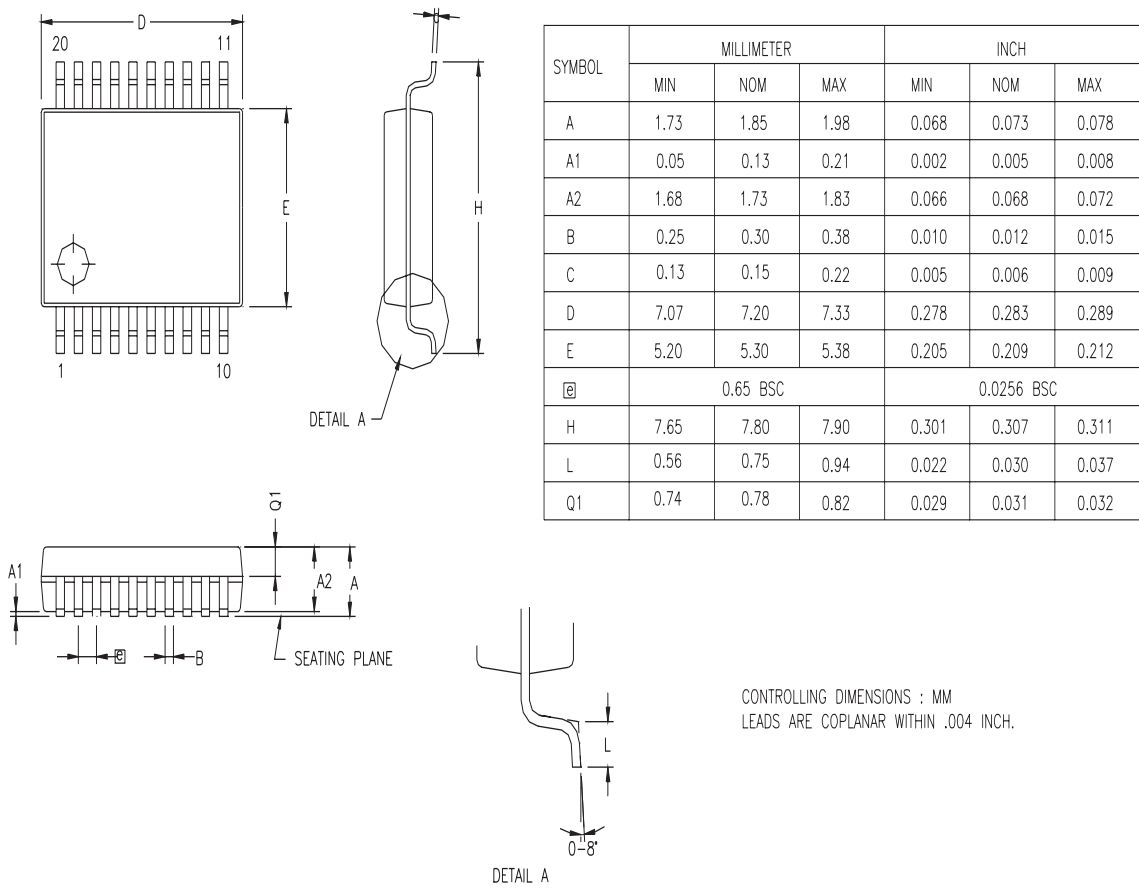
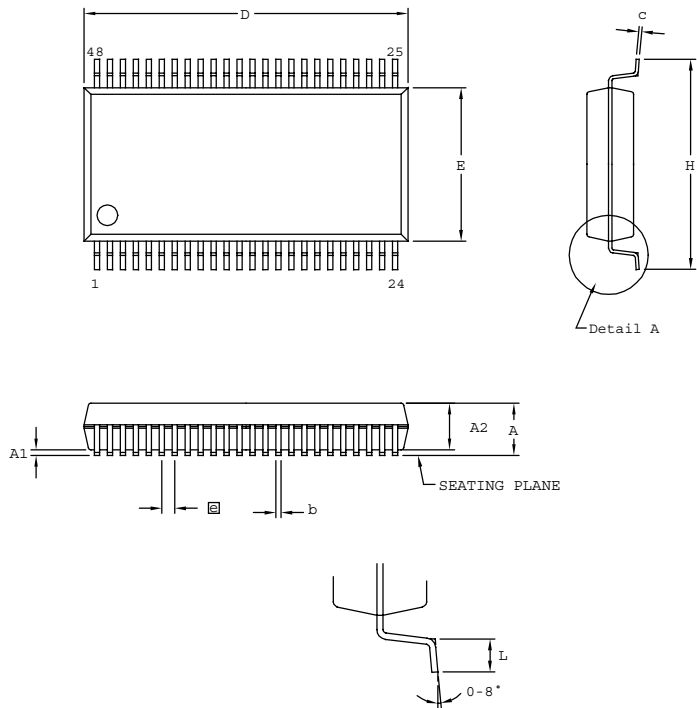


Figure 61. 20-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
ⓐ	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

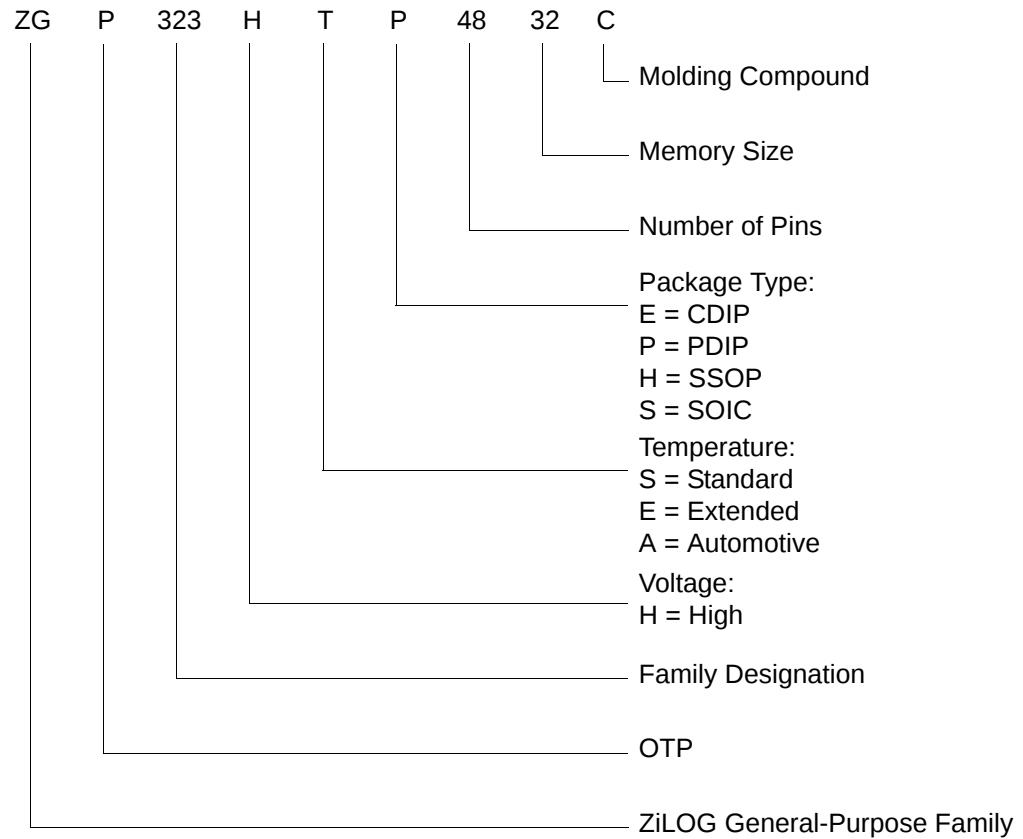
CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 68. 48-Pin SSOP Package Design

► **Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.



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