#### Zilog - ZGP323HEH2816G Datasheet





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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323heh2816g

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<b>-</b> : 00		04	~
Figure 68.	48-Pin SSOP Package Design		J



#### Table 3. Power Connections

Connection	Circuit	Device	
Power	V <sub>CC</sub>	V <sub>DD</sub>	
Ground	GND	V <sub>SS</sub>	



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram





	ſ		$\overline{\mathbf{\nabla}}$				
NC		1	-		40	þ	NC
P25		2			39	Þ	P24
P26		3			38		P23
P27		4			37	Þ	P22
P04		5			36	Þ	P21
P05	q	6			35		P20
P06	Ц	7			34	Þ	P03
P14	С	8	40-Pir	۱	33	Þ	P13
P15		9			32		P12
P07	Ц	10	CDIP		31	Þ	VSS
VDD		11			30		P02
P16		12			39		P11
P17	С	13			28		P10
XTAL2		14			27		P01
XTAL1	С	15			26		P00
P31		16			25		Pref1/P30
P32	С	17			24		P36
P33	q	18			23		P37
P34	С	19			22	þ	P35
NC	Ц	20			21	Þ	RESET
	_						

## Figure 5. 40-Pin PDIP/CDIP\* Pin Configuration

**Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

# ZGP323H Product Specification



	1	-	<del>\</del>	-		
NC		1	$\bigcirc$	48	_	NC
DOF		2		17	_	NC
F 20		2		47		NC DO4
P20		3		40		P24
P2/		4		45		P23
P04		5		44		P22
N/C		6		43		P21
P05	q	7		42		P20
P06		8		41		P03
P14		9		40		P13
P15		10		39		P12
P07		11	40 Dia	38		VSS
VDD		12	48-PIN	37		VSS
VDD		13	330P	36		N/C
N/C		14		35		P02
P16	Е	15		34		P11
P17		16		33		P10
XTAL2		17		32		P01
XTAL1		18		31		P00
P31		19		30		N/C
P32		20		29		PREF1/P30
P33		21		28		P36
P34		22		27		P37
NC		22		26		P35
VSS	Д	20		20	_	RESET
100	-	24		ZD		NEOL I

Figure 6. 48-Pin SSOP Pin Configuration

Table 6. 40- and 48-Pin Configuration

40-Pin PDIP #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12



# **Absolute Maximum Ratings**

Stresses greater than those listed in Table 8 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

#### Table 7. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	125	° C	1
Storage temperature	-65	+150	° C	
Voltage on any pin with respect to V <sub>SS</sub>	-0.3	7.0	V	2
Voltage on $V_{DD}$ pin with respect to $V_{SS}$	-0.3	7.0	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into $V_{DD}$ or out of $V_{SS}$		75	mA	

Notes:

1. See Ordering Information.

2. This voltage applies to all pins except the following: V<sub>DD</sub>, P32, P33 and RESET.

# **Standard Test Conditions**

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).



Figure 7. Test Load Diagram



# Capacitance

Table 8 lists the capacitances.

### Table 8. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^{\circ} \text{ C}$ , $V_{CC} = \text{GND} = 0 \text{ V}$ , f = 1.0 MH	Iz, unmeasured pins returned to GND

# **DC Characteristics**

#### Table 9. GP323HS DC Characteristics

			T <sub>A</sub> =0°C to	o +70°C				
Symbol	Parameter	V <sub>CC</sub>	Min	Typ(7)	Max	Units	Conditions N	lotes
V <sub>CC</sub>	Supply Voltage		2.0		5.5	V	See Note 5 5	5
V <sub>CH</sub>	Clock Input High Voltage	2.0-5.5	0.8 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.4	V	Driven by External Clock Generator	
VIH	Input High Voltage	2.0-5.5	0.7 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V		
V <sub>IL</sub>	Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.2 V <sub>CC</sub>	V		
V <sub>OH1</sub>	Output High Voltage	2.0-5.5	V <sub>CC</sub> -0.4			V	$I_{OH} = -0.5 \text{mA}$	
V <sub>OH2</sub>	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V <sub>CC</sub> -0.8			V	I <sub>OH</sub> = -7mA	
V <sub>OL1</sub>	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$	
V <sub>OL2</sub>	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I <sub>OL</sub> = 10mA	
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V <sub>REF</sub>	Comparator Reference Voltage	2.0-5.5	0		V <sub>CC</sub> 1.75	V		
IIL	Input Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub> Pull-ups disabled	
R <sub>PU</sub>	Pull-up Resistance	2.0V	225		675	KΩ	V <sub>IN</sub> = 0V; Pullups selected by mask	
-		3.6V	75		275	KΩ	option	
		5.0V	40		160	KΩ		





Figure 9. Port 0 Configuration

# Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.



**Note:** The Port 1 direction is reset to its default state following an SMR.





Figure 11. Port 2 Configuration

# Port 3 (P37–P30)

Port 3 is a 8-bit, CMOS-compatible fixed I/O port (see Figure 12). Port 3 consists of four fixed input (P33–P30) and four fixed output (P37–P34), which can be configured under software control for interrupt and as output from the counter/timers. P30, P31, P32, and P33 are standard CMOS inputs; P34, P35, P36, and P37 are push-pull outputs.

# ZGP323H Product Specification



Location of 3	2768	Not Accessible
first Byte of	_100	On-Chip
executed		KOM
after RESET	12	Reset Start Address
	11	IRQ5
	10	IRQ5
	9	IRQ4
	8	IRQ4
	7	IRQ3
(Lower Byte)	6	IRQ3
	5	IRQ2
Interrupt Vector	4	IRQ2
(Upper Byte)	3	IRQ1
	2	IRQ1
	1	IRQ0
	0	IRQ0



# **Expanded Register File**

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8<sup>®</sup> register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the



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### Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

#### Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position	Description	
T8_Level_HI	[7:0]	R/W	Data

#### Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

#### CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

Table 15. CTR0(D)00H Counter/Timera	<b>3 Control Register</b>
-------------------------------------	---------------------------

Field	<b>Bit Position</b>		Value	Description
T8_Enable	7	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W	0*	Modulo-N
-			1	Single Pass
Time_Out	5	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	43	R/W	0 0**	SCLK
			0 1	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt



Field	Bit Position		Value	Description
Transmit_Submode/	32	R/W		Transmit Mode
Glitch_Filter			00*	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	1-			Transmit Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/	0			Transmit Mode
Falling_Edge		R/W	0*	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

#### Table 16.CTR1(0D)01H T8 and T16 Common Functions (Continued)

#### Note:

\*Default at Power-On Reset

\*Default at Power-On Reset. Not reset with Stop Mode recovery.

#### Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

#### P36\_Out/Demodulator\_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

ZGP323H Product Specification



**Caution:** Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFFH. Transition from 0 to FFFFH is not a timeout condition.







Figure 27. T16\_OUT in Modulo-N Mode

#### **T16 DEMODULATION Mode**

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

#### If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).



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#### SMR(0F)0BH



\* Default after Power On Reset or Watch-Dog Reset

\* \* Default setting after Reset and Stop Mode Recovery

\* \* \* At the XOR gate input

\* \* \* \* Default setting after reset. Must be 1 if using a crystal or resonator clock source.

#### Figure 33. STOP Mode Recovery Register

#### SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.



#### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

#### **EPROM Selectable Options**

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

#### Table 24. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

#### Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V<sub>DD</sub> is at the required level for correct operation of the device. Reset is globally driven when V<sub>DD</sub> falls below V<sub>BO</sub>. A small drop in V<sub>DD</sub> causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V<sub>DD</sub> is allowed to stay above V<sub>RAM</sub>, the RAM content is preserved. When the power level is returned to above V<sub>BO</sub>, the device performs a POR and functions normally.







**Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



MILLIMETER

MAX

2.65

0.30

2.44

0.46

0.30

12.95

7.60

10.65

0.40

1.00

1.07

1.27 BSC



INCH

мах

.104

.012

.096

.018

.012

.510

.299

.419

.016

.039

.042

.050 BSC

MIN

.094

.004

.088

.014

.009

.496

.291

.394

.012

.024

.038



Figure 60. 20-Pin SOIC Package Diagram

PS023803-0305



#### 16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4816C	48-pin SSOP 16K OTP	ZGP323HSS2816C	28-pin SOIC 16K OTP
ZGP323HSP4016C	40-pin PDIP 16K OTP	ZGP323HSH2016C	20-pin SSOP 16K OTP
ZGP323HSH2816C	28-pin SSOP 16K OTP	ZGP323HSP2016C	20-pin PDIP 16K OTP
ZGP323HSP2816C	28-pin PDIP 16K OTP	ZGP323HSS2016C	20-pin SOIC 16K OTP

16KB Extended Temperature: -40° to +105°C				
Part Number	Description	Part Number	Description	
ZGP323HEH4816C	48-pin SSOP 16K OTP	ZGP323HES2816C	28-pin SOIC 16K OTP	
ZGP323HEP4016C	40-pin PDIP 16K OTP	ZGP323HEH2016C	20-pin SSOP 16K OTP	
ZGP323HEH2816C	28-pin SSOP 16K OTP	ZGP323HEP2016C	20-pin PDIP 16K OTP	
ZGP323HEP2816C	28-pin PDIP 16K OTP	ZGP323HES2016C	20-pin SOIC 16K OTP	

# 16KB Automotive Temperature: -40° to +125°CPart NumberDescriptionPart NumberDescriptionZGP323HAH4816C48-pin SSOP 16K OTPZGP323HAS2816C28-pin SOIC 16K OTPZGP323HAP4016C40-pin PDIP 16K OTPZGP323HAH2016C20-pin SSOP 16K OTPZGP323HAH2816C28-pin SSOP 16K OTPZGP323HAP2016C20-pin PDIP 16K OTPZGP323HAP2816C28-pin PDIP 16K OTPZGP323HAS2016C20-pin SOIC 16K OTPZGP323HAP2816C28-pin PDIP 16K OTPZGP323HAS2016C20-pin SOIC 16K OTPReplace C with G for Lead-Free Packaging





#### 4KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4804C	48-pin SSOP 4K OTP	ZGP323HSS2804C	28-pin SOIC 4K OTP
ZGP323HSP4004C	40-pin PDIP 4K OTP	ZGP323HSH2004C	20-pin SSOP 4K OTP
ZGP323HSH2804C	28-pin SSOP 4K OTP	ZGP323HSP2004C	20-pin PDIP 4K OTP
ZGP323HSP2804C	28-pin PDIP 4K OTP	ZGP323HSS2004C	20-pin SOIC 4K OTP

#### 4KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4804C	48-pin SSOP 4K OTP	ZGP323HES2804C	28-pin SOIC 4K OTP
ZGP323HEP4004C	40-pin PDIP 4K OTP	ZGP323HEH2004C	20-pin SSOP 4K OTP
ZGP323HEH2804C	28-pin SSOP 4K OTP	ZGP323HEP2004C	20-pin PDIP 4K OTP
ZGP323HEP2804C	28-pin PDIP 4K OTP	ZGP323HES2004C	20-pin SOIC 4K OTP

#### 4KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description	
ZGP323HAH4804C	48-pin SSOP 4K OTP	ZGP323HAS2804C	28-pin SOIC 4K OTP	
ZGP323HAP4004C	40-pin PDIP 4K OTP	ZGP323HAH2004C	20-pin SSOP 4K OTP	
ZGP323HAH2804C	28-pin SSOP 4K OTP	ZGP323HAP2004C	20-pin PDIP 4K OTP	
ZGP323HAP2804C	28-pin PDIP 4K OTP	ZGP323HAS2004C	20-pin SOIC 4K OTP	
Replace C with G for Lead-Free Packaging				

Additional Components				
Part Number	Description	Part Number	Description	
ZGP323ICE01ZEM (For 3.6V Emulation only)	Emulator/programmer	ZGP32300100ZPR (Ethernet)	Programming system	
		ZGP32300200ZPR (USB)	Programming system	

# ZGP323H Z8<sup>®</sup> OTP Microcontroller with IR Timers



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