Zilog - ZGP323HEH4816C Datasheet





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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323heh4816c

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List of Figures

Figure 1.	Functional Block Diagram	. 3
Figure 2.	Counter/Timers Diagram	. 4
Figure 3.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	. 5
Figure 4.	28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	. 6
Figure 5.	40-Pin PDIP/CDIP* Pin Configuration	. 7
Figure 6.	48-Pin SSOP Pin Configuration	. 8
Figure 7.	Test Load Diagram	10
Figure 8.	AC Timing Diagram	16
Figure 9.	Port 0 Configuration	19
Figure 10.	Port 1 Configuration	20
Figure 11.	Port 2 Configuration	21
Figure 12.	Port 3 Configuration	22
Figure 13.	Port 3 Counter/Timer Output Configuration	24
Figure 14.	Program Memory Map (32K OTP)	26
Figure 15.	Expanded Register File Architecture	28
Figure 16.	Register Pointer	29
Figure 17.	Register Pointer—Detail	31
Figure 18.	Glitch Filter Circuitry	40
Figure 19.	Transmit Mode Flowchart	41
Figure 20.	8-Bit Counter/Timer Circuits	42
Figure 21.	T8_OUT in Single-Pass Mode	43
Figure 22.	T8_OUT in Modulo-N Mode	43
Figure 23.	Demodulation Mode Count Capture Flowchart	44
Figure 24.	Demodulation Mode Flowchart	45
Figure 25.	16-Bit Counter/Timer Circuits	46
Figure 26.	T16_OUT in Single-Pass Mode	47
Figure 27.	T16_OUT in Modulo-N Mode	47
Figure 28.	Ping-Pong Mode Diagram	49
Figure 29.	Output Circuit	49
Figure 30.	Interrupt Block Diagram	51
Figure 31.	Oscillator Configuration	53
Figure 32.	Port Configuration Register (PCON) (Write Only)	55
Figure 33.	STOP Mode Recovery Register	57





Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.





	-			
		\bigcirc		
NC			40	⊐ NC
P25	2		39	⊐ P24
P26	- 3		38	⊐ P23
P27	4		37	⊐ P22
P04	5		36	コ P21
P05	6		35	⊐ P20
P06	7		34	□ P03
P14	8	40-Pin	33	コ P13
P15	9	PDIP	32	⊐ P12
P07	10	CDIP*	31	⊐ VSS
VDD	11		30	⊐ P02
P16	12		39	⊐ P11
P17	13		28	コ P10
XTAL2	14		27	D P01
XTAL1	15		26	D P00
P31	16		25	□ Pref1/P30
P32	17		24	⊐ P36
P33	18		23	D P37
P34	19		22	⊐ P35
NC	20		21	RESET

Figure 5. 40-Pin PDIP/CDIP* Pin Configuration

Note: *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

ZGP323H Product Specification



	I					
NC		1	\bigcirc	48	_	NC
P25		2		47	-	NC
P26		3		46	_	P24
P27		4		45		P23
P04		5			_	P22
N/C		6			-	P21
P05		7			_	P20
P06		8		42		P03
P14		9		40		P13
P15		10		39	-	P12
P07		11		38		VSS
VDD		12	48-Pin	37		VSS
VDD		13	SSOP		_	N/C
N/C		14		35	-	P02
P16		15		34		P11
P17		16				P10
XTAL2		17		32	-	P01
XTAL1	Π	18		31		P00
P31		19		30		N/C
P32		20		29	-	PREF1/P30
P33		21		28		P36
		22		27		P37
		22		26	_	P35
VSS		23		25	_	RESET
		27		25		

Figure 6. 48-Pin SSOP Pin Configuration

Table 6. 40- and 48-Pin Configuration

40-Pin PDIP #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12

ZGP323H Product Specification



40-Pin PDIP #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V _{DD}
31	24, 37, 38	V _{SS}
25	29	Pref1/P30
	48	NC
	6	NC
	14	NC
	30	NC
	36	NC

Table 6. 40- and 48-Pin Configuration (Continued)





Figure 13. Port 3 Counter/Timer Output Configuration



Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 22. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.



Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The Z8 GP does not assert the $\overline{\text{RESET}}$ pin when under VBO.



Note: The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8[®], functionality in consumer and battery-operated applications.

Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

RAM

This device features 256B of RAM. See Figure 14.



Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
T8_Enable	7	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	5	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	43	R/W	0 0**	SCLK
			0 1	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Interrupt
-			1	Enable Data Capture Interrupt



T8/T16_Logic/Edge _Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to "NORMAL OPERATION Mode" terminates the "PING-PONG Mode" operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Note: Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 17 lists and briefly describes the fields for this register.



When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.



Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



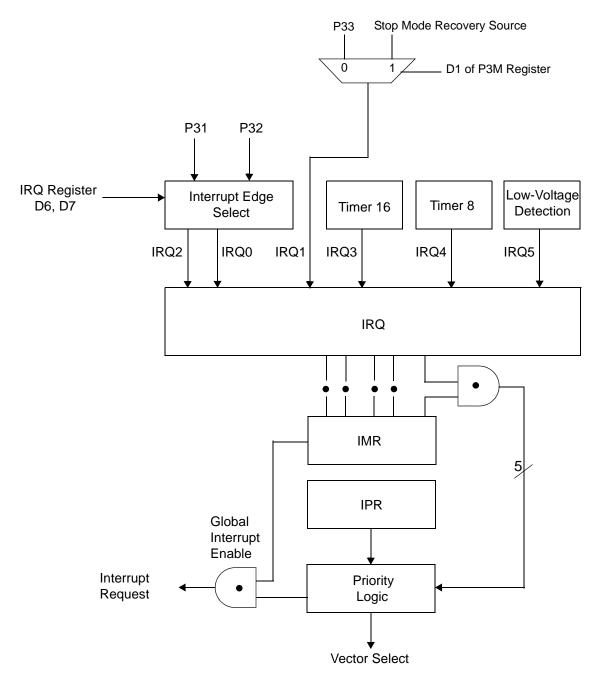


Figure 30. Interrupt Block Diagram



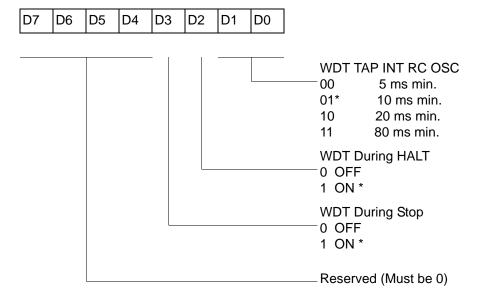
<mark>____</mark> 62

Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8[®] CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



* Default setting after reset

Figure 37. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 23.



Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

			1	1		1		
D7	D6	D5	D4	D3	D2	D1	D0	
								 0 P34 as Port Output * 1 Timer8 Output 0 Disable T8 Timeout Interrupt * * 1 Enable T8 Timeout Interrupt 0 Disable T8 Data Capture Interrupt * * 1 Enable T8 Data Capture Interrupt * * 1 Enable T8 Data Capture Interrupt * * 1 Enable T8 Data Capture Interrupt 00 SCLK on T8* * 01 SCLK/2 on T8 10 SCLK/4 on T8 11 SCLK/8 on T8 R 0 No T8 Counter Timeout * * R 1 T8 Counter Timeout Occurred W 0 No Effect W 1 Reset Flag to 0 0 Modulo-N * 1 Single Pass R 0 T8 Disabled * R 1 T8 Enabled W 0 Stop T8 W 1 Enable T8

* Default setting after reset.

* * Default setting after Reset.. Not reset with a Stop-Mode recovery.

Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)





)7	D6	D5	D4	D3	D2	D1	D0	
		_		_				Transmit Mode* R/W 0 T16_OUT is 0 initially 1 T16_OUT is 1 initially Demodulation Mode R 0 No Falling Edge Detection R 1 Falling Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode*
								R/W 0 T8_OUT is 0 initially* 1 T8_OUT is 1 initially Demodulation Mode R 0 No Rising Edge Detection R 1 Rising Edge Detection W 0 No Effect
								W 1 Reset Flag to 0 Transmit Mode* 0 0 Normal Operation* 0 1 Ping-Pong Mode 1 0 T16_OUT = 0 1 1 T16_OUT = 1
								Demodulation Mode 0 0 No Filter 0 1 4 SCLK Cycle Filter 1 0 8 SCLK Cycle Filter 1 1 Reserved
								Transmit Mode/T8/T16 Logic 0 0 AND** 0 1 OR 1 0 NOR 1 1 NAND
								Demodulation Mode 0 0 Falling Edge Detection 0 1 Rising Edge Detection 1 0 Both Edge Detection 1 1 Reserved
								Transmit Mode* 0 P36 as Port Output * 1 P36 as T8/T16_OUT Demodulation Mode
								0 P31 as Demodulator Inpu 1 P20 as Demodulator Inpu Transmit/Demodulation Mode
	fault se fault se				reset	with a 9	Stop Mor	0 Transmit Mode * 1 Demodulation Mode

Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)



CTR2(0D)02H

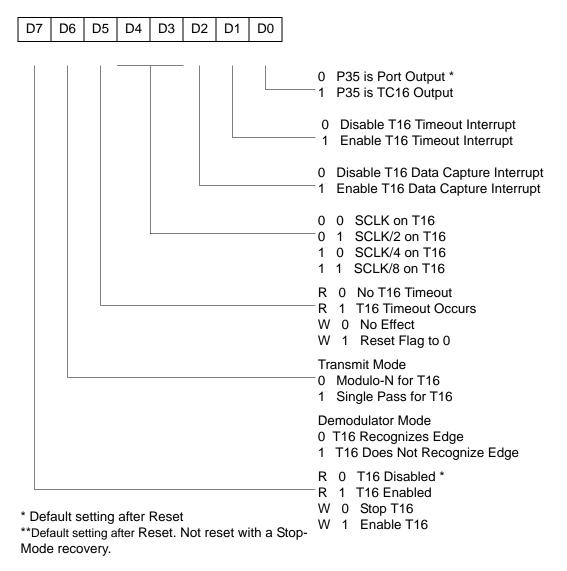


Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)





CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0	
								Reserved No effect when written Always reads 11111 Sync Mode 0* Disable Sync Mode** 1 Enable Sync Mode T ₈ Enable R 0* T ₈ Disabled R 1 T ₈ Enabled W0 Stop T ₈
								W1 Enable T_8 T_{16} Enable R 0* T_{16} Disabled R 1 T_{16} Enabled W 0 Stop T_{16} W 1 Enable T_{16}

* Default setting after reset. ** Default setting after reset. Not reset with a Stop Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)



R254 SPH(FEH)



Figure 56. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)



Stack Pointer Low Byte (SP7–SP0)

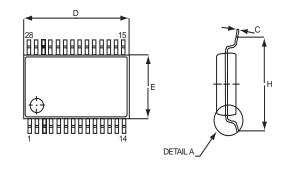
Figure 57. Stack Pointer Low (FFH: Read/Write)

Package Information

Package information for all versions of ZGP323H is depicted in Figures 59 through Figure 68.







¥	≜ A
	A2 A

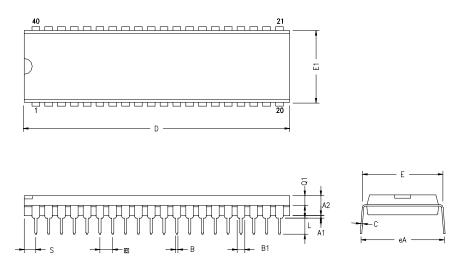
		MILLIMETER	2	INCH			
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX	
А	1.73	1.86	1.99	0.068	0.073	0.078	
A1	0.05	0.13	0.21	0.002	0.005	0.008	
A2	1.68	1.73	1.78	0.066	0.068	0.070	
В	0.25		0.38	0.010		0.015	
С	0.09	-	0.20	0.004	0.006	0.008	
D	10.07	10.20	10.33	0.397	0.402	0.407	
E	5.20	5.30	5.38	0.205	0.209	0.212	
е		0.65 TYP		0.0256 TYP			
Н	7.65	7.80	7.90	0.301	0.307	0.311	
L	0.63	0.75	0.95	0.025	0.030	0.037	

CONTROLLING DIMENSIONS: MM LEADS ARE COPLANAR WITHIN .004 INCHES.

<u>DETAIL 'A'</u>

0-8

Figure 65. 28-Pin SSOP Package Diagram



SYMBOL	MILLIN	IETER	INCH		
STMDUL	MIN	MAX	MIN	MAX	
A1	0.51	1.02	.020	.040	
A2	3.18	3.94	.125	.155	
В	0.38	0.53	.015	.021	
B1	1.02	1.52	.040	.060	
С	0.23	0.38	.009	.015	
D	52.07	52.58	2.050	2.070	
E	15.24	15.75	.600	.620	
E1	13.59	14.22	.535	.560	
e	2.54	TYP	.100 TYP		
eA	15.49	16.76	.610	.660	
L	3.05	3.81	.120	.150	
Q1	1.40	1.91	.055	.075	
S	1.52	2.29	.060	.090	

CONTROLLING DIMENSIONS : INCH

Figure 66. 40-Pin PDIP Package Diagram



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

- 323 = Family Designation
- H = High Voltage
- T = Temparature
 - S = Standard 0° to +70°C
 - $E = Extended 40^{\circ} to + 105^{\circ}C$
 - A = Automotive -40° to $+125^{\circ}$ C
- P = Package Type:
 - K = CDIP
 - P = PDIP
 - H = SSOP
 - S = SOIC

= Number of Pins

- CC = Memory Size
- M = Molding Compound
- C = Standard Plastic Packaging Molding Compound
- G = Green Plastic Molding Compound
- E = Standard Cer Dip flow

ZGP323H Z8[®] OTP Microcontroller with IR Timers



28-pin DIP/SOIC/SSOP 6 40- and 48-pin 8 40-pin DIP 7 48-pin SSOP 8 pin functions port 0 (P07 - P00) 18 port 0 (P17 - P10) 19 port 0 configuration 19 port 1 configuration 20 port 2 (P27 - P20) 20 port 2 (P37 - P30) 21 port 2 configuration 21 port 3 configuration 22 port 3 counter/timer configuration 24 reset) 25 XTAL1 (time-based input 18 XTAL2 (time-based output) 18 ping-pong mode 48 port 0 configuration 19 port 0 pin function 18 port 1 configuration 20 port 1 pin function 19 port 2 configuration 21 port 2 pin function 20 port 3 configuration 22 port 3 pin function 21 port 3counter/timer configuration 24 port configuration register 55 power connections 3 power supply 5 program memory 25 map 26 R ratings, absolute maximum 10 register 61 CTR(D)01h 35 CTR0(D)00h 33 CTR2(D)02h 37 CTR3(D)03h 39 flag 80 HI16(D)09h 32

HI8(D)0Bh 32 interrupt priority 78 interrupt request 79 interruptmask 79 L016(D)08h 32 L08(D)0Ah 32 LVD(D)0Ch 65 pointer 80 port 0 and 1 77 port 2 configuration 75 port 3 mode 76 port configuration 55, 75 SMR2(F)0Dh 40 stack pointer high 81 stack pointer low 81 stop mode recovery 57 stop mode recovery 2 61 stop-mode recovery 73 stop-mode recovery 274 T16 control 69 T8 and T16 common control functions 67 T8/T16 control 70 TC16H(D)07h 32 TC16L(D)06h 33 TC8 control 66 TC8H(D)05h 33 TC8L(D)04h 33 voltage detection 71 watch-dog timer 75 register description Counter/Timer2 LS-Byte Hold 33 Counter/Timer2 MS-Byte Hold 32 Counter/Timer8 Control 33 Counter/Timer8 High Hold 33 Counter/Timer8 Low Hold 33 CTR2 Counter/Timer 16 Control 37 CTR3 T8/T16 Control 39 Stop Mode Recovery2 40 T16 Capture LO 32 T8 and T16 Common functions 35 T8_Capture_HI 32