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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hep2008c

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Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 4.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin #	Symbol	Function	Direction
1–3	P25–P27	Port 2, Bits 5,6,7	Input/Output
4	P07	Port 0, Bit 7	Input/Output
5	V _{DD}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8–10	P31–P33	Port 3, Bits 1,2,3	Input
11,12	P34. P36	Port 3, Bits 4,6	Output
13	P00/Pref1/P30	Port 0, Bit 0/Analog reference input Port 3 Bit 0	Input/Output for P00 Input for Pref1/P30
14	P01	Port 0, Bit 1	Input/Output
15	V _{SS}	Ground	
16–20	P20–P24	Port 2, Bits 0,1,2,3,4	Input/Output





P25 P26 P27 P04 P05 P06 P07 V _{DD} XTAL2 XTAL2 P31 P32 P33	1 2 3 4 5 6 7 8 9 10 11 12 13	28-Pin PDIP SOIC SSOP CDIP*	28 27 26 25 24 23 22 21 20 19 18 17	□ P24 □ P23 □ P22 □ P21 □ P03 □ V _{SS} □ P02 □ P01 □ P00 □ Pref1/P30 □ P36
P32 □ P33 □	12 13		17 16	□ P36 □ P37 □ P35
F 34 L	14		15	LI P35

Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 5. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V _{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30	Input	Analog ref input; connect to V _{CC} if not used
	Port 3 Bit 0		Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V _{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4



Capacitance

Table 8 lists the capacitances.

Table 8. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^{\circ} \text{ C}$, $V_{CC} = \text{GND} = 0 \text{ V}$, f = 1.0 MH	Iz, unmeasured pins returned to GND

DC Characteristics

Table 9. GP323HS DC Characteristics

			T _A =0°C to	o +70°C				
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions N	lotes
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5 5	5
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator	
VIH	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	$I_{OH} = -0.5 \text{mA}$	
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{CC} 1.75	V		
IIL	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled	
R _{PU}	Pull-up Resistance	2.0V	225		675	KΩ	V _{IN} = 0V; Pullups selected by mask	
-		3.6V	75		275	KΩ	option	
		5.0V	40		160	KΩ		



			T _A =0°C	to +70°C				
Symbol	Parameter	V _{CC}	Min	Typ(7)	Мах	Units	Conditions	Notes
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0V, V_{CC}$	
Icc	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
00		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I _{CC1}	Standby Current	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
	(HALT Mode)	3.6V		0.8	2.0	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I _{CC2}	Standby Current (Stop	2.0V		1.6	8	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
	Mode)	3.6V		1.8	10	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
		5.5V		1.9	12	μΑ	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
		2.0V		5	20	μΑ	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		3.6V		8	30	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		5.5V		15	45	μΑ	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage			1.9	2.0	V	8MHz maximum	
20	Protection						Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage			2.4		V		
	Detection							
V _{HVD}	Vcc High Voltage			2.7		V		
	Detection							

Table 9. GP323HS DC Characteristics (Continued)

Notes:

1. All outputs unloaded, inputs at rail.

2. CL1 = CL2 = 100 pF.

3. Oscillator stopped.

4. Oscillator stops when V_{CC} falls below V_{BO} limit.

 It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VCC and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

- 6. Comparator and Timers are on. Interrupt disabled.
- 7. Typical values shown are at 25 degrees C.

Table 10. GP323HE DC Characteristics

	T _A = -40°C to +105°C							
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} 0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	I _{OH} = -0.5mA	



AC Characteristics





Figure 8. AC Timing Diagram



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The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A OH in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.





Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 28)

R253 RP = 00h R0 = Port 0 R1 = Port 1 R2 = Port 2 R3 = Port 3

But if:

R253 RP = 0Dh R0 = CTR0 R1 = CTR1 R2 = CTR2R3 = Reserved







Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



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Table 15.CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	0	R/W	0* 1	P34 as Port Output T8 Output on P34

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

T8 Clock

This bit defines the frequency of the input signal to T8.







Figure 19. Transmit Mode Flowchart



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If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

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Note: Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.





Figure 28. Ping-Pong Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.





The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.



Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XORgate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/ TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address OBH.



WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

Table 24. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.





Low-Voltage Detection Register—LVD(D)0Ch

Note: Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position			Description
LVD	76543			Reserved No Effect
	2	R	1 0*	HVD flag set HVD flag reset
	1-	R	1 0*	LVD flag set LVD flag reset
	0	R/W	1 0*	Enable VD Disable VD
*Default	after POR			

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the V_{CC} level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V_{CC} is higher than V_{HVD}. The LVD flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

Notes: If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.



R248 P01M(F8H)



* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)



R252 Flags(FCH)



Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)



MILLIMETER

MAX

2.65

0.30

2.44

0.46

0.30

12.95

7.60

10.65

0.40

1.00

1.07

1.27 BSC



INCH

мах

.104

.012

.096

.018

.012

.510

.299

.419

.016

.039

.042

.050 BSC

MIN

.094

.004

.088

.014

.009

.496

.291

.394

.012

.024

.038



Figure 60. 20-Pin SOIC Package Diagram

PS023803-0305







Figure 68. 48-Pin SSOP Package Design

Note: Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.



Example



ZGP323H Z8[®] OTP Microcontroller with IR Timers



T8_Capture_LO 32 register file 30 expanded 26 register pointer 29 detail 31 reset pin function 25 resets and WDT 63 S SCLK circuit 58 single-pass mode T16_OUT 47 T8_OUT 43 stack 31 standard test conditions 10 standby modes 1 stop instruction, counter/timer 54 stop mode recovery 2 register 61 source 59 stop mode recovery 2 61 stop mode recovery register 57 Т T16 transmit mode 46 T16_Capture_HI 32 T8 transmit mode 40 T8_Capture_HI 32 test conditions, standard 10 test load diagram 10 timing diagram, AC 16 transmit mode flowchart 41 V VCC 5 voltage brown-out/standby 64 detection and flags 65 voltage detection register 71 W watch-dog timer mode registerwatch-dog timer mode register 62 time select 63

X XTAL1 5 XTAL1 pin function 18 XTAL2 5 XTAL2 pin function 18