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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hep2008g

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Development Features

Table 2 lists the features of ZiLOG[®]'s ZGP323H members.

Table 2. Features

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323H OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–5.5V

- Low power consumption–18mW (typical)
- T = Temperature
 - S = Standard 0° to +70°C
 - $E = Extended -40^{\circ} to +105^{\circ}C$
 - A = Automotive -40° to $+125^{\circ}$ C
- Three standby modes:
 - STOP— (typical 1.8µA)
 - HALT— (typical 0.8mA)
 - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
 - One programmable 8-bit counter/timer with two capture registers and two load registers
 - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
 - Programmable input glitch filter for pulse reception
- Six priority interrupts
 - Three external
 - Two assigned to counter/timers
 - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
 - Port 0: 0–3 pull-up transistors
 - Port 0: 4–7 pull-up transistors





P25 P26 P27 P04 P05 P06 P07 V _{DD} XTAL2 XTAL2 P31 P32 P33	1 2 3 4 5 6 7 8 9 10 11 12 13	28-Pin PDIP SOIC SSOP CDIP*	28 27 26 25 24 23 22 21 20 19 18 17	□ P24 □ P23 □ P22 □ P21 □ P03 □ V _{SS} □ P02 □ P01 □ P00 □ Pref1/P30 □ P36
P32 □ P33 □	12 13		17 16	□ P36 □ P37 □ P35
F 34 L	14		15	LI P35

Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 5. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V _{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30	Input	Analog ref input; connect to V _{CC} if not used
	Port 3 Bit 0		Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V _{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4



				Watch-Dog Timer Mode Register				
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes	(D1, D0)
1	ТрС	Input Clock Period	2.0–5.5	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–5.5		25	ns	1	
3	TwC	Input Clock Width	2.0–5.5	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 5.5	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–5.5	3ТрС			1	
6	TpTin	Timer Input Period	2.0–5.5	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–5.5		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 5.5	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–5.5	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width	2.0–5.5	12		ns	3	
		Spec		5TpC			4	
11	Tost	Oscillator Start-Up Time	2.0–5.5		5TpC		4	
12	Twdt	Watch-Dog Timer	2.0–5.5	5		ms		0, 0
		Delay Time	2.0–5.5	10		ms		0, 1
			2.0-5.5	20		ms		1,0
			2.0-0.0	ðU		ms		1, 1
13	T _{POR}	Power-On Reset	2.0–5.5	2.5	10	ms		

Table 13. AC Characteristics

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0. 2. Interrupt request through Port 3 (P33–P31).

3. SMR – D5 = 1.

4. SMR - D5 = 0.





Figure 13. Port 3 Counter/Timer Output Configuration

ZGP323H Product Specification



Location of 3	2768	Not Accessible
first Byte of	_100	On-Chip
executed		KOM
after RESET	12	Reset Start Address
	11	IRQ5
	10	IRQ5
	9	IRQ4
	8	IRQ4
	7	IRQ3
(Lower Byte)	6	IRQ3
	5	IRQ2
Interrupt Vector	4	→ IRQ2
(Upper Byte)	3	IRQ1
	2	IRQ1
	1	IRQ0
	0	IRQ0



Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8[®] register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the





Expanded Reg. Bank 0/Group 15" Register Pointer [7] [5] [4] [3] [2] [10] Working Register Group Pointer Bank Pointer FF FP Bank Pointer FF FP Bank Pointer FF FF FF FF Bank Pointer FF FF		Z8 [®] Standard	Control Registers	Res	et C	Cond	itior	۱
Register Pointer FF SPL FE U <thu< th=""> <thu< th=""> U U</thu<></thu<>			Expanded Reg. Bank 0/Group 15	** D7 D6 D	5 D4	D3	D2[D1 D0
Register Pointer Image: Construction of the second of					1	ii		
Register Pointer T D								
Register Pointer U <			FD RP		0	0	0	
7 6 5 4 3 2 1 0		Register Pointer	FC FLAGS					
Working Register Group Pointer Expanded Register Bank Pointer FA IRQ 0 <td< td=""><td>7</td><td>7 6 5 4 3 2 1 0</td><td>FB IMB</td><td></td><td></td><td></td><td></td><td></td></td<>	7	7 6 5 4 3 2 1 0	FB IMB					
Working Register Expanded Register F3 F3 <td></td> <td></td> <td>FA IBO</td> <td></td> <td>0</td> <td>0</td> <td>0</td> <td></td>			FA IBO		0	0	0	
Ordop Pollies Dirth Antes PB PD1M 1 0 <t< td=""><td>Working Regist</td><td>ter Expanded Regist</td><td>er F9 IPR</td><td></td><td></td><td></td><td></td><td></td></t<>	Working Regist	ter Expanded Regist	er F9 IPR					
F7 P3M 0	Group Pointer	Dank i ontei	F8 P01M	1 1 0	0	1	1	1 1
F6 P2M 1			F7 P3M		0	0	0	0 0
F5 Reserved I			F6 P2M	1 1 1	1	1	1	1 1
F4 Reserved F3 Reserved F3 Reserved F4 Reserved F5 Reserved F6 F6 F6 F7 F7 F8 F8 F8 F7 F8 F8 F8 F9 F8 <td></td> <td></td> <td>F5 Reserved</td> <td></td> <td></td> <td>$\frac{1}{1}$</td> <td>ii l</td> <td></td>			F5 Reserved			$\frac{1}{1}$	ii l	
Fig Reserved U			F4 Reserved			11	U	
File (Bank 0)** File (Bank 0)** File (Bank 0)** File Reserved U			F3 Reserved		U U	U	U	
Findersterning (bank 0)** Findersterning (bank 0)**			F2 Reserved		U U	U	Ŭ	
F0 Reserved U	FF	Register File (Bank 0)	F1 Reserved		U U	Ŭ	U	υυ
Image: Second State Sta	Fo		F0 Reserved		U U	Ŭ	U	
Figure 1 Expanded Reg. Bank F/Group 0** (F) 0F WD 1MR (F) 0F WD 1MR (F) 0F Reserved (F) 0F Reserved (F) 0R Reserved						1-1	~	
Image: constraint of the second state stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the			Expanded Reg. Bank F/Group 0*	*				
(F) 0E Reserved 0			(F) 0F WDTMR	U U O	0	1	1	0 1
F) OD SMR2 0			(F) 0E Reserved			Π		
7F F			* (F) 0D SMR2	0 0 0	0	0	0	0 0
7F (F) 0B SMR U 0 1 0 0 0 U 0 (F) 0B Reserved (F) 0B Reserved (F) 0B Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved </td <td>_</td> <td></td> <td>(F) 0C Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	_		(F) 0C Reserved					
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(F) 09 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved		_	(F) 0A Reserved			Π		
(F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 00 PCON (F) 01 Reserved (O) 01 P1 U (O) 00 P0 U U = Unknown (D) 00 C T16L * 18 not reset with a Stop-Mode Recovery * 111 Bits 5,4,3,2 not reset with a Stop-Mode Recovery * 111 Bits 5,4,3,2,2 not reset with a			(F) 09 Reserved					
0F (F) 07 Reserved (F) 06 Reserved (F) 06 Reserved (F) 05 Reserved (F) 07 Reserved (F) 04 Reserved (F) 07 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 04 Reserved (F) 04 Reserved			(F) 08 Reserved					
0F (F) 06 Reserved (F) 05 Reserved (F) 04 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 03 P3 0 (F) 01 Reserved (F) 00 PCON (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 00 PCON (F) 01 Reserved (F) 01 P1 (F) 01 Reserved (D) 02 P2 (F) 00 PCON (F) 03 B Hil8 (F) 00 0 0 0 0 0 0 0 (D) 04 LO8 (F) 00 0 0 0 0 0 (F) 03 B LO16 (F) 00 0 0 0 0 0 (F) 04 C LD8 (F) 00 0 0 0 0 0 (D) 05 TC8H (F) 00 0 0 0 0 0 (F) 03 C TR3 (F) 0 0 0 0 0 0 (F) 04 TC8L (F) 0 0 0 0 0 0 (F) 04 C C R2<			(F) 07 Reserved					
0F 0F <td< td=""><td></td><td></td><td>(F) 06 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 06 Reserved					
0F 00 <td< td=""><td></td><td></td><td>(F) 05 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 05 Reserved					
00 Image: constraint of the set with a Stop-Mode Recovery 1 <td>0F</td> <td><u> </u>₩/</td> <td>(F) 04 Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	0F	<u> </u> ₩/	(F) 04 Reserved					
Expanded Reg. Bank 0/Group (0) (F) 02 Reserved 1	00		(F) 03 Reserved					
Expanded Reg. Bank 0/Group (0) (0) 03 P3 0 (0) 02 P2 U (0) 01 P1 U (0) 01 P1 U (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** Di 03 CTR3 0 ** (D) 04 TC8L 0 0 0 ** (D) 03 CTR3 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 01 CTR1 0 ** (D) 00 CTR0 0		\backslash	(F) 02 Reserved					
Expanded Reg. Bank 0/Group (0) (0) 03 P3 0 U (0) 02 P2 U * (0) 01 P1 U (0) 00 P0 U (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** His 5 Is not reset with a Stop-Mode Recovery ** (D) 04 TC8L 0 <			(F) 01 Reserved					
(0) 03 P3 0 U (0) 02 P2 U * (0) 01 P1 U (0) 00 P0 U * (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ^* (D) 05 TC8H 0	Expa	anded Reg. Bank 0/Group (0)	(F) 00 PCON	1 1 1	1	1	1	1 0
(0) 03 P3 0			Expanded Reg. Bank D/Group 0					
(b) 02 P2 U * (0) 01 P1 U (0) 00 P0 U U = Unknown * * All addresses are in hexadecimal * ↑ Bit 5 Is not reset with a Stop-Mode Recovery ** (D) 04 ** (D) 05 ** (D) 06 ** (D) 07 ** (D) 08 ** (D) 08 ** (D) 07 ** (D) 08 ** (D) 07 ** (D) 06 ** (D) 06 ** (D) 07 ** (D) 06 ** (D) 07 ** (D) 08 ** (D) 08 ** (D) 04 ** (D) 05 ** (D) 04 ** (D) 03 ** (D) 02 ** (D) 01 ** (D) 01 ** (D) 01 ** (D) 01 ** (D) 02 ** (D) 01 (D) 0	(0) 03 P3	U U		UUI	υ	U	U	υn
* (0) 01 P1 U (0) 01 P1 U (0) 00 P0 U * (D) 00 A LO8 0<	(0) 02 P2	U	* (D) 0B HI8	0 0 0	0	0	0	0 0
(b) 01 1 1 0	* (0) 01 P1	U	* (D) 0A 08	0 0 0	0	0	0	0 0
(0) 00 P0 U U = Unknown (D) 08 LO16 0	(0) 011 1	<u> </u>	* (D) 09 HI16	0 0 0	0	0	0	0 0
U = Unknown * (D) 07 TC16H 0 <td>(0) 00 P0</td> <td>U</td> <td>* (D) 08 LO16</td> <td>0 0 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td>	(0) 00 P0	U	* (D) 08 LO16	0 0 0	0	0	0	0 0
* Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ^* All addresses are in hexadecimal ^* Is not reset with a Stop-Mode Recovery, except Bit 0 ^* Bit 5 Is not reset with a Stop-Mode Recovery ^* Bit 5 Is not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Diss 5,4,3,2 not reset with a Stop-Mode Recovery ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery ^* CD 00 CTR1 0 0 ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery ^* CD 00 CTR0 ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery			* (D) 07 TC16H	0 0 0	0	0	0	0 0
*** All addresses are in hexadecimal * (D) 05 TC8H 0 <t< td=""><td>* Is not reset with a Ston-Mor</td><td>de Recoverv</td><td>* (D) 06 TC16L</td><td>0 0 0</td><td>0</td><td>0</td><td>0</td><td>0 0</td></t<>	* Is not reset with a Ston-Mor	de Recoverv	* (D) 06 TC16L	0 0 0	0	0	0	0 0
⁺ Is not reset with a Stop-Mode Recovery, except Bit 0 ⁺ 1bit 5 Is not reset with a Stop-Mode Recovery ⁺ (D) 04 TC8L ⁻ 0 0 0 0 0 0 0 0 0 0 0 ⁺ (D) 03 CTR3 ⁻ 0 0 0 0 1 1 1 1 1 ⁺ 1 ⁺ (D) 02 CTR2 ⁻ 0 0 0 0 0 0 0 0 0 ⁻ 1 1 1 1 ⁺	** All addresses are in beyade	ecimal	* (D) 05 TC8H	0 0 0	0	0	0	0 0
	↑ Is not reset with a Stop-Mo	de Recovery, except Bit 0	* (D) 04 TC8L	0 0 0	0	0	0	0 0
[↑] ↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery [↑] ↑↑↑ [↑] ↑↑↑ [↑] ↑↑↑ [↑] ↑↑↑↑ [↑] ↑↑↑ [↑] ↑↑ [↑] ↑ [↑]	↑↑ Bit 5 Is not reset with a Sto	p-Mode Recovery	1↑ (D) 03 CTR3	0 0 0	1	1	1	1 1
^{↑↑↑↑} Bits 5 and 4 not reset with a Stop-Mode Recovery ^{↑↑↑↑↑} (D) 01 CTR1 (D) 01 CTR1 (D) 0 0 0 0 0 0 0 0 (D) 01 CTR1 (D) 00 CTR0 (D)	↑↑↑ Bits 5,4,3.2 not reset with	a Stop-Mode Recoverv	↑↑↑ (D) 02 CTR2	0 0 0	0	0	0	0 0
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery ↑↑↑↑↑↓ (D) 00 CTR0 0 0 0 0 0 0 0 0 0 0	↑↑↑↑ Bits 5 and 4 not reset with	a Stop-Mode Recovery	↑↑↑↑ (D) 01 CTR1	0 0 0	0	0	0	0 0
	↑↑↑↑↑ Bits 5,4,3,2,1 not reset wit	th a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	0 0 0	0	0	0	0 0

Figure 15. Expanded Register File Architecture



Table 15.CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	0	R/W	0* 1	P34 as Port Output T8 Output on P34

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

T8 Clock

This bit defines the frequency of the input signal to T8.



Field	Bit Position		Value	Description
T16_Enable	7	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W		Transmit Mode
			0*	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize
				Edge
Time_Out	5	R	0*	No Counter Timeout
			1	Counter Timeout
				Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	43	R/W	00**	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	1-	R/W	0*	Disable Timeout Int.
				Enable Timeout Int.
P35_Out	0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Table 17. CTR2(D)02H: Counter/Timer16 Control Register

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.







Figure 19. Transmit Mode Flowchart



When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.



Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

)

Note: Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.



Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{DD} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from V_{BO} Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10 μ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:







Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 22).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 21 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Reserved	7		0	Reserved (Must be 0)
Recovery Level	-6	W	0 [†]	Low
-			1	High
Reserved	5		0	Reserved (Must be 0)
Source	432	W	000†	A. POR Only
			001	B. NAND of P23–P20
			010	C. NAND of P27–P20
			011	D. NOR of P33–P31
			100	E. NAND of P33–P31
			101	F. NOR of P33–P31, P00, P07
			110	G. NAND of P33–P31, P00, P07
			111	H. NAND of P33–P31, P22–P20
Reserved	10		00	Reserved (Must be 0)

Table 21.SMR2(F)0DH:Stop	Mode Recovery	Register	2*
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Notes:

* Port pins configured as outputs are ignored as a SMR recovery source. † Indicates the value upon Power-On Reset



Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH

D7	D6	D5	D4	D3	D2	D1	D0	
								Reserved (Must be 0) Reserved (Must be 0) Stop-Mode Recovery Source 2 000 POR Only * 001 NAND P20, P21, P22, P23 010 NAND P20, P21, P22, P23, P24, P25, P26, P27 011 NOR P31, P32, P33 100 NAND P31, P32, P33 101 NOR P31, P32, P33, P00, P07 110 NAND P31, P32, P33, P00, P07
								111 NAND P31, P32, P33, P20, P21, P22
								Reserved (Must be 0)
								Recovery Level * * 0 Low * 1 High
								Reserved (Must be 0)

Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset

* * At the XOR gate input

Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.



Note: Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.



Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

D7	D6	D5	D4	D3	D2	D1	D0	
								 0 P34 as Port Output * 1 Timer8 Output 0 Disable T8 Timeout Interrupt * * 1 Enable T8 Timeout Interrupt 0 Disable T8 Data Capture Interrupt * * 1 Enable T8 Data Capture Interrupt * * 1 Enable T8 Data Capture Interrupt 00 SCLK on T8* * 00 SCLK on T8* * 01 SCLK/2 on T8 10 SCLK/4 on T8 11 SCLK/8 on T8 R 0 No T8 Counter Timeout * * R 1 T8 Counter Timeout Occurred W 0 No Effect W 1 Reset Flag to 0 0 Modulo-N * 1 Single Pass R 0 T8 Disabled * R 1 T8 Enabled W 0 Stop T8 W 4 Enable T9
								VV I ETIADIE IO

* Default setting after reset.

* * Default setting after Reset.. Not reset with a Stop-Mode recovery.

Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)



R252 Flags(FCH)



Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)



MILLIMETER

MAX

2.65

0.30

2.44

0.46

0.30

12.95

7.60

10.65

0.40

1.00

1.07

1.27 BSC



INCH

мах

.104

.012

.096

.018

.012

.510

.299

.419

.016

.039

.042

.050 BSC

MIN

.094

.004

.088

.014

.009

.496

.291

.394

.012

.024

.038



Figure 60. 20-Pin SOIC Package Diagram

PS023803-0305







Figure 62. 28-Pin SOIC Package Diagram





4KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4804C	48-pin SSOP 4K OTP	ZGP323HSS2804C	28-pin SOIC 4K OTP
ZGP323HSP4004C	40-pin PDIP 4K OTP	ZGP323HSH2004C	20-pin SSOP 4K OTP
ZGP323HSH2804C	28-pin SSOP 4K OTP	ZGP323HSP2004C	20-pin PDIP 4K OTP
ZGP323HSP2804C	28-pin PDIP 4K OTP	ZGP323HSS2004C	20-pin SOIC 4K OTP

4KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4804C	48-pin SSOP 4K OTP	ZGP323HES2804C	28-pin SOIC 4K OTP
ZGP323HEP4004C	40-pin PDIP 4K OTP	ZGP323HEH2004C	20-pin SSOP 4K OTP
ZGP323HEH2804C	28-pin SSOP 4K OTP	ZGP323HEP2004C	20-pin PDIP 4K OTP
ZGP323HEP2804C	28-pin PDIP 4K OTP	ZGP323HES2004C	20-pin SOIC 4K OTP

4KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description	
ZGP323HAH4804C	48-pin SSOP 4K OTP	ZGP323HAS2804C	28-pin SOIC 4K OTP	
ZGP323HAP4004C	40-pin PDIP 4K OTP	ZGP323HAH2004C	20-pin SSOP 4K OTP	
ZGP323HAH2804C	28-pin SSOP 4K OTP	ZGP323HAP2004C	20-pin PDIP 4K OTP	
ZGP323HAP2804C	28-pin PDIP 4K OTP	ZGP323HAS2004C	20-pin SOIC 4K OTP	
Replace C with G for Lead-Free Packaging				

Additional Components					
Part Number	Description	Part Number	Description		
ZGP323ICE01ZEM (For 3.6V Emulation only)	Emulator/programmer	ZGP32300100ZPR (Ethernet)	Programming system		
		ZGP32300200ZPR (USB)	Programming system		