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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hep2808g

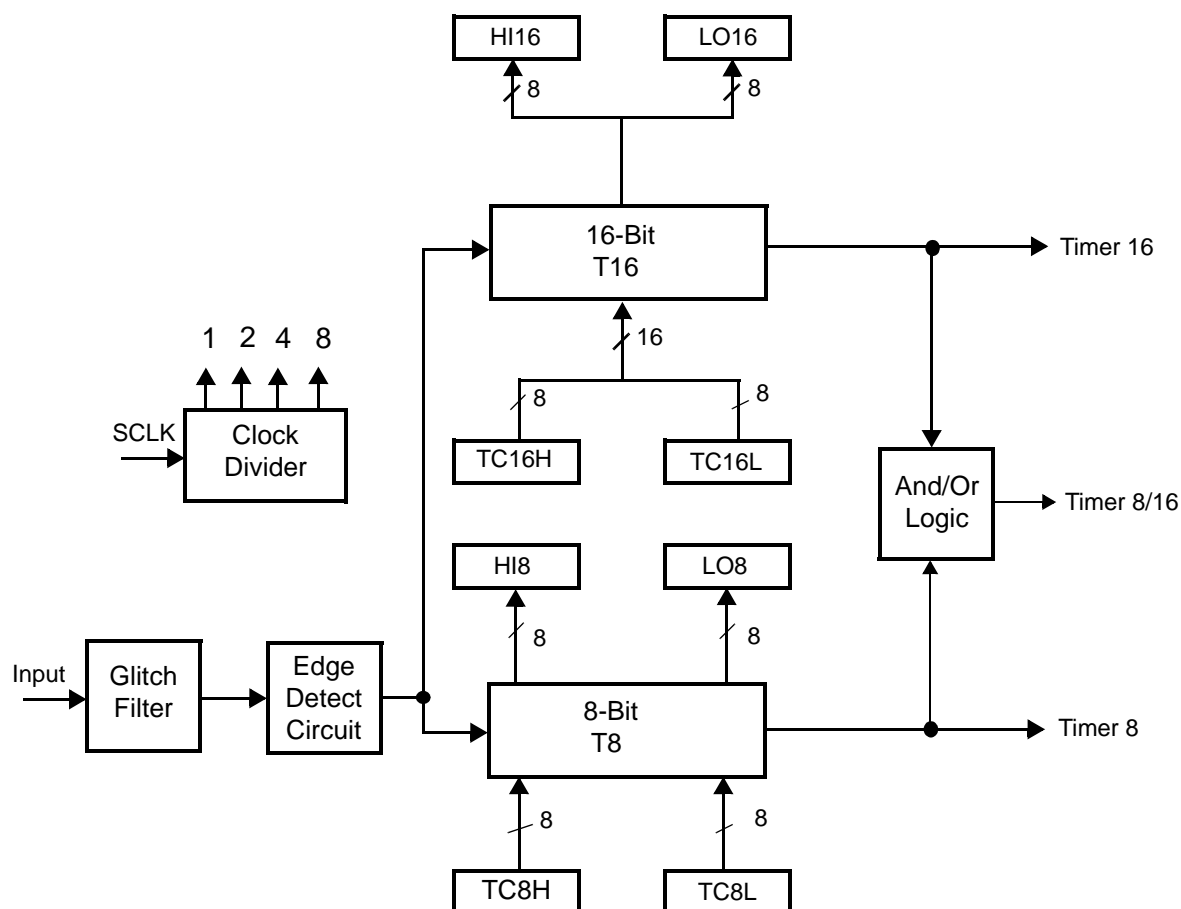


Figure 2. Counter/Timers Diagram

Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.



Table 6. 40- and 48-Pin Configuration (Continued)

40-Pin PDIP #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V _{DD}
31	24, 37, 38	V _{SS}
25	29	Pref1/P30
	48	NC
	6	NC
	14	NC
	30	NC
	36	NC



Table 10. GP323HE DC Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A = -40°C to +105°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	I _{OL} = 4.0mA	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V		
I _{IL}	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled	
R _{PU}	Pull-up Resistance	2.0V	200.0		700.0	KΩ	V _{IN} = 0V; Pullups selected by mask option	
		3.6V	50.0		300.0	KΩ		
		5.0V	25.0		175.0	KΩ		
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC}	
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I _{CC1}	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I _{CC2}	Standby Current (Stop Mode)	2.0V		1.6	12	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		3.6V		1.8	15	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		5.5V		1.9	18	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		2.0V		5	30	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		3.6V		8	40	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		5.5V		15	60	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V		
V _{HVD}	V _{CC} High Voltage Detection			2.7		V		

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V_{CC} and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.



Table 11. GP323HA DC Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A = -40°C to +125°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
V _{HVD}	V _{CC} High Voltage Detection			2.7		V		

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V_{CC} and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

Table 12. EPROM/OTP Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	100			Cycles	1

Notes:

1. For windowed cerdip package only.
2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

$$AF = \exp[(E_a/k) * (1/T_{use} - 1/T_{stress})]$$

Where:

E_a is the intrinsic activation energy (eV; typ. 0.8)

k is Boltzman's constant (8.67 x 10⁻⁵ eV/°K)

°K = -273.16°C

T_{use} = Use Temperature in °K

T_{stress} = Stress Temperature in °K

3. At a stable UV Lamp output of 20mW/CM²



Table 13. AC Characteristics

				T _A =0°C to +70°C (S) –40°C to +105°C (E) –40°C to +125°C (A) 8.0MHz				Watch-Dog Timer Mode Register (D1, D0)
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes	
1	TpC	Input Clock Period	2.0–5.5	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–5.5		25	ns	1	
3	TwC	Input Clock Width	2.0–5.5	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 5.5	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–5.5	3TpC			1	
6	TpTin	Timer Input Period	2.0–5.5	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–5.5		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 5.5	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–5.5	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width Spec	2.0–5.5	12 5TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–5.5		5TpC		4	
12	Twdt	Watch-Dog Timer Delay Time	2.0–5.5 2.0–5.5 2.0–5.5 2.0–5.5	5 10 20 80		ms ms ms ms	0, 0 0, 1 1, 0 1, 1	
13	T _{POR}	Power-On Reset	2.0–5.5	2.5	10	ms		

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.

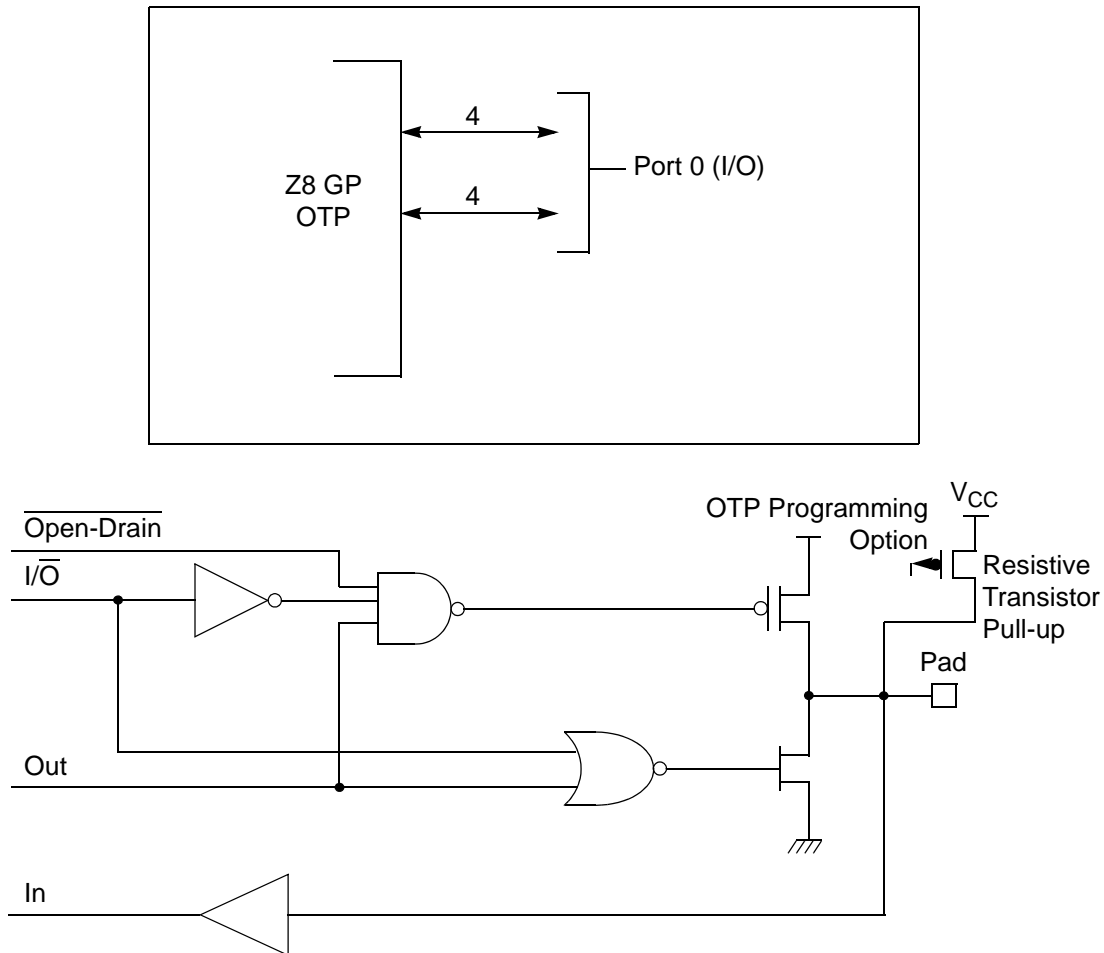


Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Note:** The Port 1 direction is reset to its default state following an SMR.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

Table 16. CTR1(0D)01H T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-----	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/ Demodulator_Input	-6-----	R/W	0*	Transmit Mode
			1	Port Output
				T8/T16 Output
			0*	Demodulation Mode
			1	P31
				P20
T8/T16_Logic/ Edge_Detect	--54----	R/W		Transmit Mode
			00**	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved



T8/T16_Logic/Edge _Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

- **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 17 lists and briefly describes the fields for this register.



Table 17. CTR2(D)02H: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-----	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Transmit Mode
			1	Modulo-N
			0	Single Pass
			1	Demodulation Mode
Time_Out	--5-----	R	0*	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
		W	0	No Counter Timeout
			1	Counter Timeout Occurred
T16_Clock	---43---	R/W	00**	No Effect
			01	Reset Flag to 0
			10	SCLK
			11	SCLK/2
Capture_INT_Mask	-----2--	R/W	0**	SCLK/4
			1	SCLK/8
Counter_INT_Mask	-----1-	R/W	0*	Disable Data Capture Int.
			1	Enable Data Capture Int.
P35_Out	-----0	R/W	0*	Disable Timeout Int.
			1	Enable Timeout Int.

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.

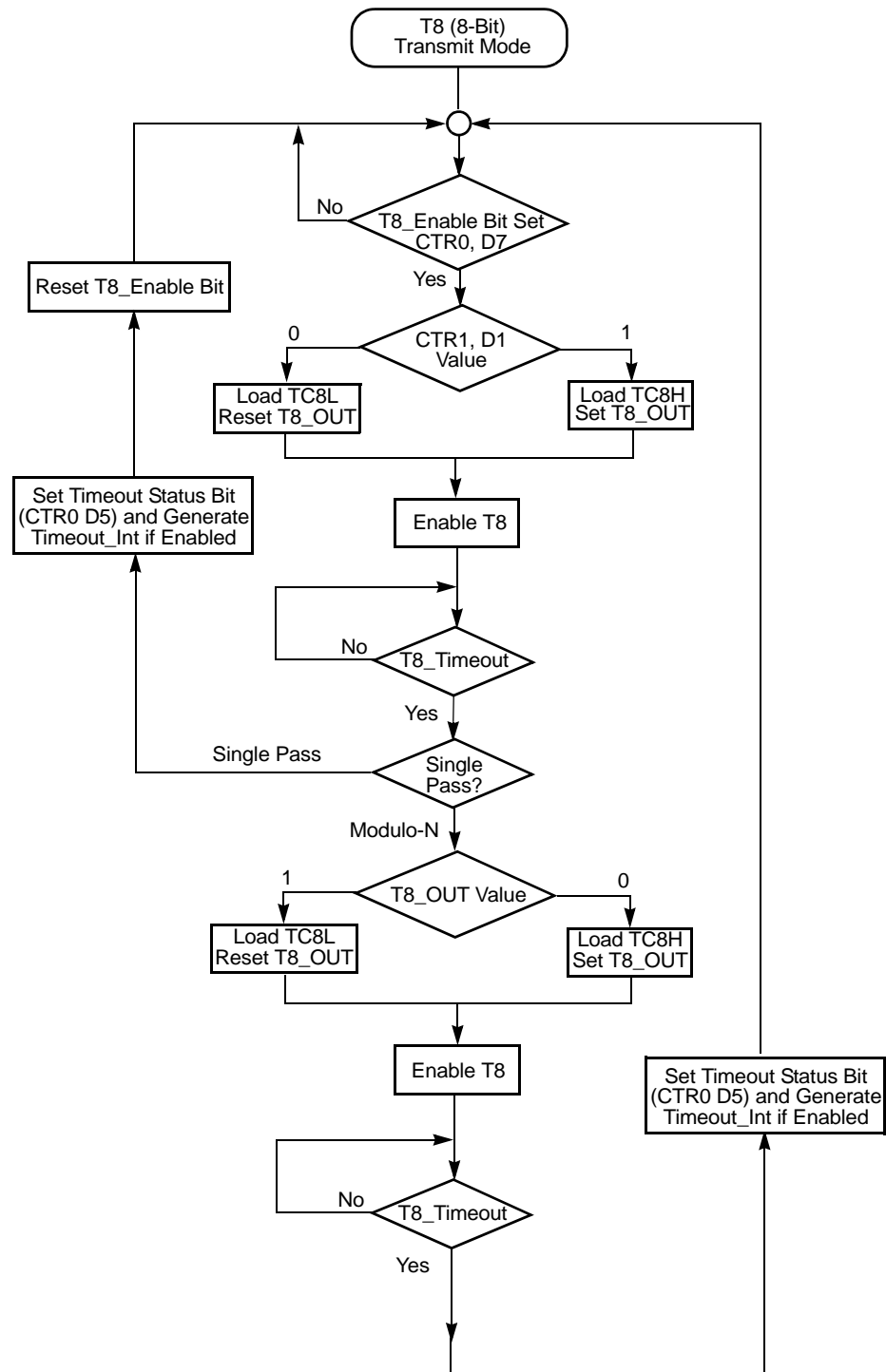


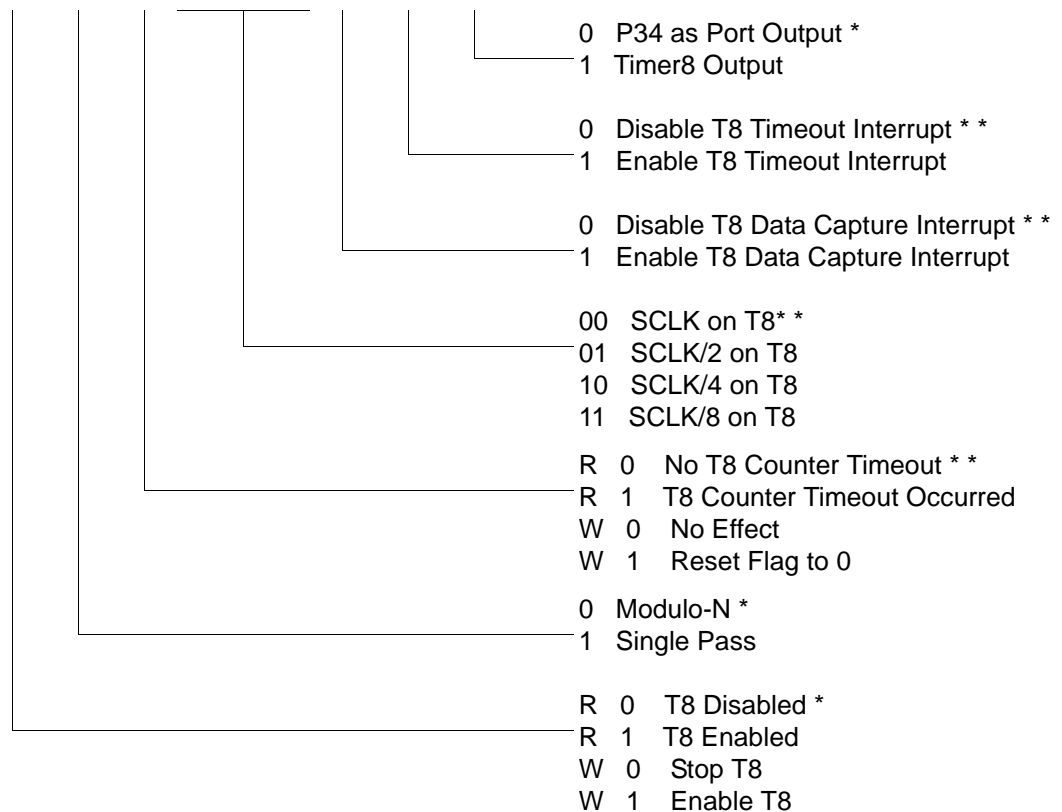
Figure 19. Transmit Mode Flowchart

Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset.

** Default setting after Reset.. Not reset with a Stop-Mode recovery.

Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)



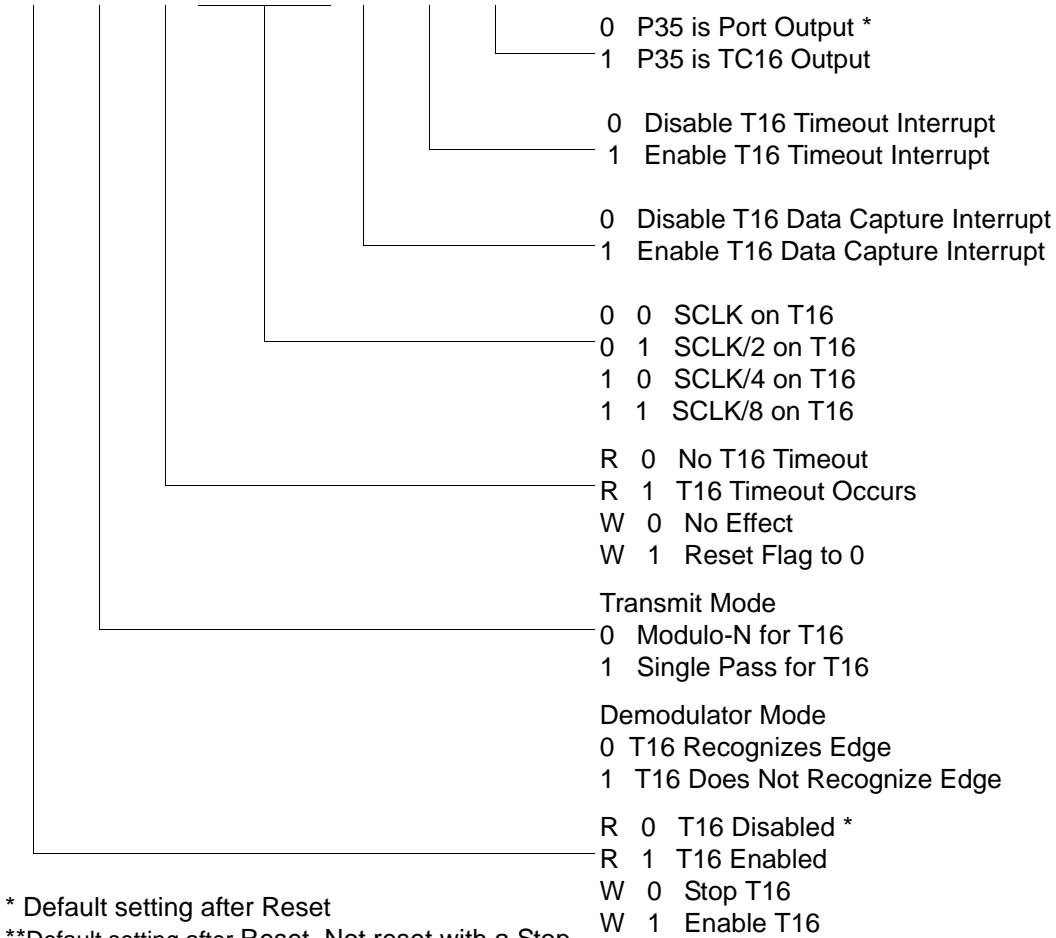
- **Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



CTR2(0D)02H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

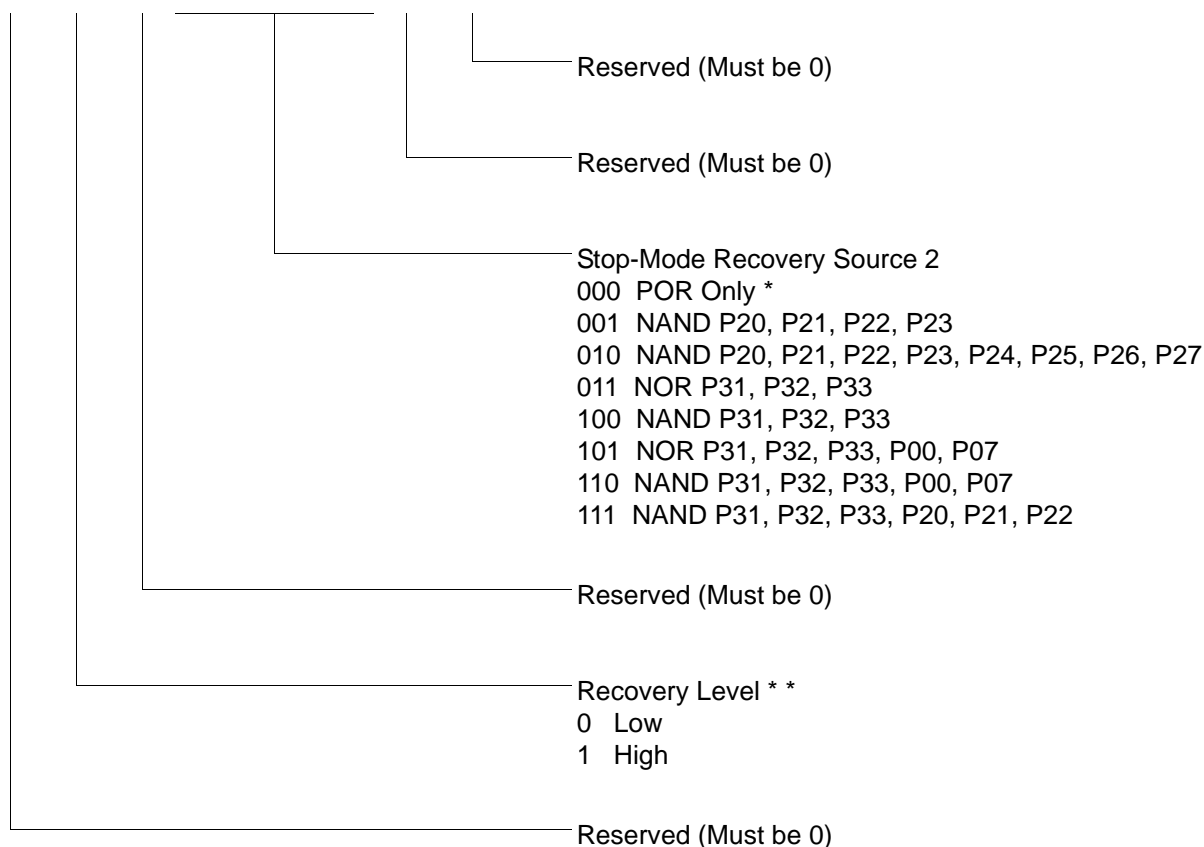


* Default setting after Reset
**Default setting after Reset. Not reset with a Stop-Mode recovery.

Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)

SMR2(0F)0DH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



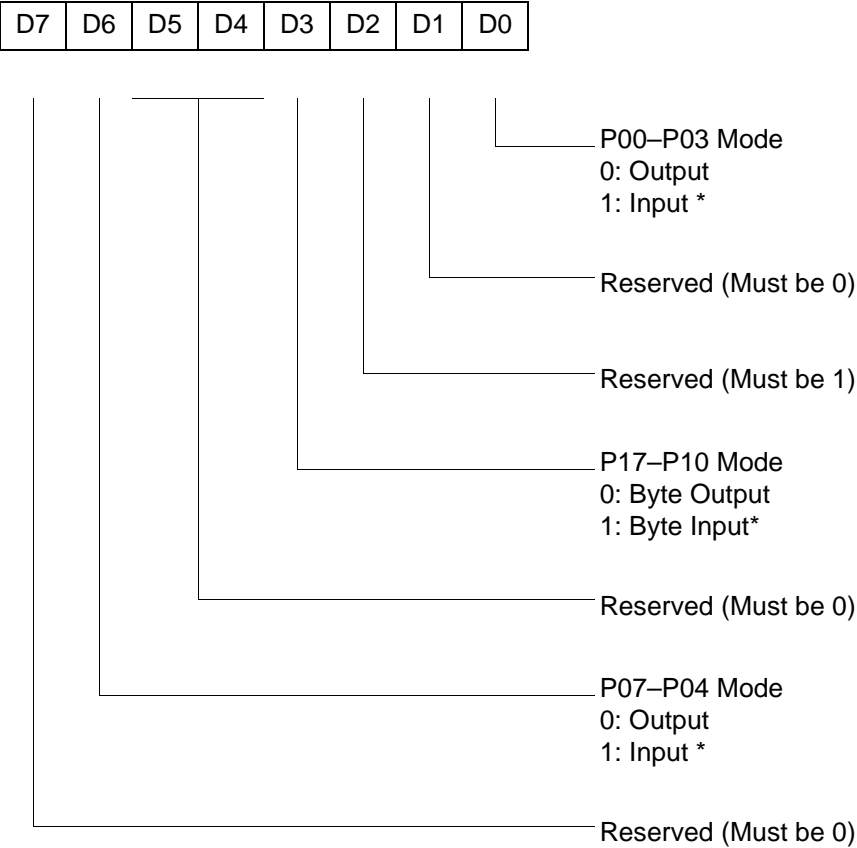
Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset. Not reset with a Stop Mode recovery.

* * At the XOR gate input

Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)

R248 P01M(F8H)



* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)



R249 IPR(F9H)

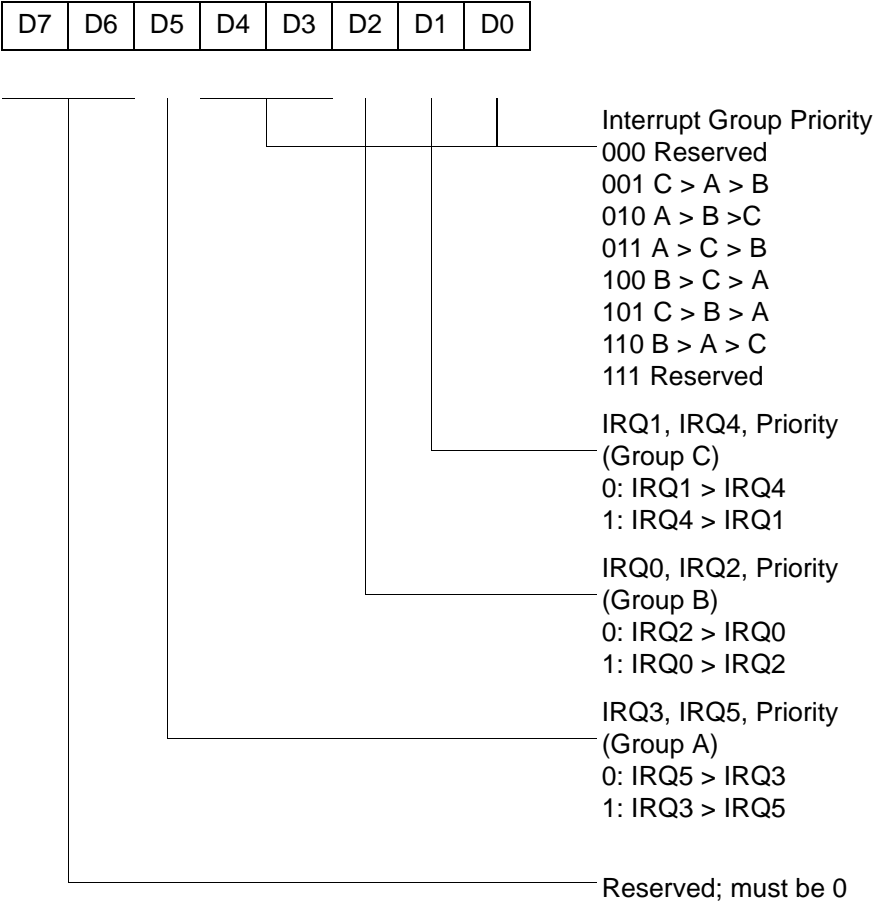


Figure 51. Interrupt Priority Register (F9H: Write Only)

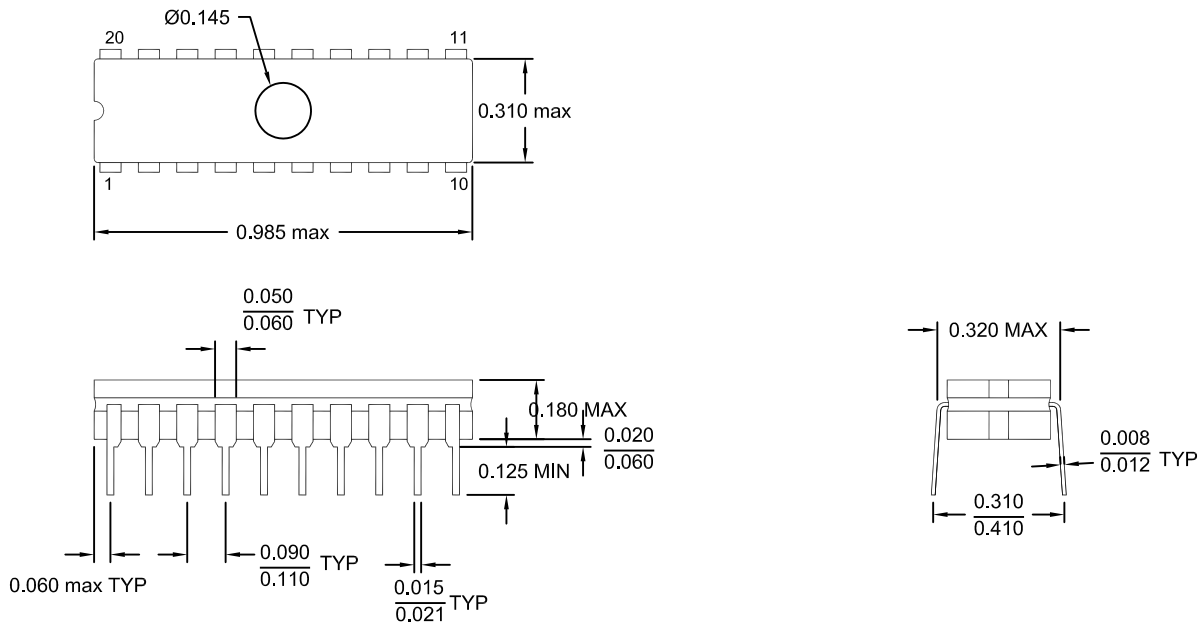


Figure 58. 20-Pin CDIP Package

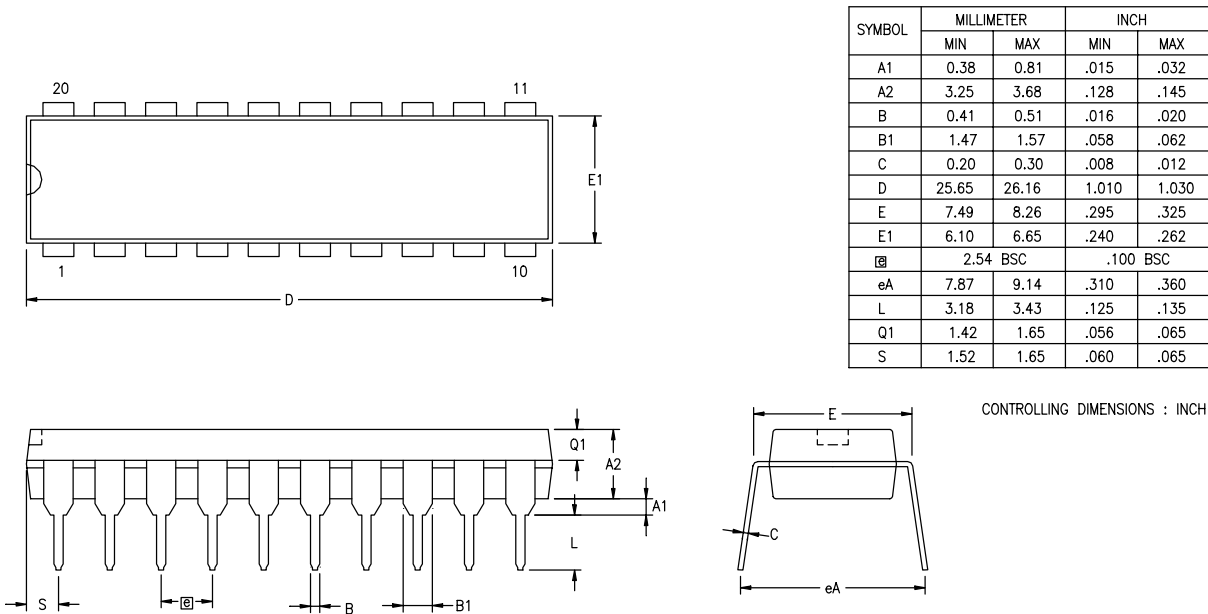


Figure 59. 20-Pin PDIP Package Diagram



Ordering Information

32KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4832C	48-pin SSOP 32K OTP	ZGP323HSS2832C	28-pin SOIC 32K OTP
ZGP323HSP4032C	40-pin PDIP 32K OTP	ZGP323HSH2032C	20-pin SSOP 32K OTP
ZGP323HSK2832E	28-pin CDIP 32K OTP	ZGP323HSK2032E	20-pin CDIP 32K OTP
ZGP323HSK4032E	40-pin CDIP 32K OTP	ZGP323HSP2032C	20-pin PDIP 32K OTP
ZGP323HSH2832C	28-pin SSOP 32K OTP	ZGP323HSS2032C	20-pin SOIC 32K OTP
ZGP323HSP2832C	28-pin PDIP 32K OTP		

32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4832C	48-pin SSOP 32K OTP	ZGP323HES2832C	28-pin SOIC 32K OTP
ZGP323HEP4032C	40-pin PDIP 32K OTP	ZGP323HEH2032C	20-pin SSOP 32K OTP
ZGP323HEH2832C	28-pin SSOP 32K OTP	ZGP323HEP2032C	20-pin PDIP 32K OTP
ZGP323HEP2832C	28-pin PDIP 32K OTP	ZGP323HES2032C	20-pin SOIC 32K OTP

32KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323HAH4832C	48-pin SSOP 32K OTP	ZGP323HAS2832C	28-pin SOIC 32K OTP
ZGP323HAP4032C	40-pin PDIP 32K OTP	ZGP323HAH2032C	20-pin SSOP 32K OTP
ZGP323HAH2832C	28-pin SSOP 32K OTP	ZGP323HAP2032C	20-pin PDIP 32K OTP
ZGP323HAP2832C	28-pin PDIP 32K OTP	ZGP323HAS2032C	20-pin SOIC 32K OTP

Replace C with G for Lead-Free Packaging

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