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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hep2832g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Table 3. Power Connections

Connection	Circuit	Device	
Power	V _{CC}	V _{DD}	
Ground	GND	V _{SS}	



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram





P25 P26 P27 P04 P05 P06 P07 V _{DD} XTAL2 XTAL2 P31 P32 P33	1 2 3 4 5 6 7 8 9 10 11 12 13	28-Pin PDIP SOIC SSOP CDIP*	28 27 26 25 24 23 22 21 20 19 18 17	□ P24 □ P23 □ P22 □ P21 □ P03 □ V _{SS} □ P02 □ P01 □ P00 □ Pref1/P30 □ P36
P32 □ P33 □	12 13		17 16	□ P36 □ P37 □ P35
F 34 L	14		15	ц P35

Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 5. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V _{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30	Input	Analog ref input; connect to V _{CC} if not used
	Port 3 Bit 0		Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V _{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4



Absolute Maximum Ratings

Stresses greater than those listed in Table 8 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	125	° C	1
Storage temperature	-65	+150	° C	
Voltage on any pin with respect to V _{SS}	-0.3	7.0	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	7.0	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	

Notes:

1. See Ordering Information.

2. This voltage applies to all pins except the following: V_{DD}, P32, P33 and RESET.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).



Figure 7. Test Load Diagram



Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 22. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.



Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The Z8 GP does not assert the $\overline{\text{RESET}}$ pin when under VBO.



Note: The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8[®], functionality in consumer and battery-operated applications.

Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

RAM

This device features 256B of RAM. See Figure 14.



The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A OH in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.





Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 28)

R253 RP = 00h R0 = Port 0 R1 = Port 1 R2 = Port 2 R3 = Port 3

But if:

R253 RP = 0Dh R0 = CTR0 R1 = CTR1 R2 = CTR2R3 = Reserved



Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description	
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect	

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data



Field	Bit Position		Value	Description
T16_Enable	7	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W		Transmit Mode
			0*	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize
				Edge
Time_Out	5	R	0*	No Counter Timeout
			1	Counter Timeout
				Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	43	R/W	00**	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	1-	R/W	0*	Disable Timeout Int.
				Enable Timeout Int.
P35_Out	0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Table 17. CTR2(D)02H: Counter/Timer16 Control Register

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.







Figure 19. Transmit Mode Flowchart



When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.



Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFH (see Figure 23 and Figure 24).



Figure 23. Demodulation Mode Count Capture Flowchart



If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

>

Note: Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.







Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 22).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 21 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Reserved	7		0	Reserved (Must be 0)
Recovery Level	-6	W	0 [†]	Low
-			1	High
Reserved	5		0	Reserved (Must be 0)
Source	432	W	000†	A. POR Only
			001	B. NAND of P23–P20
			010	C. NAND of P27–P20
			011	D. NOR of P33–P31
			100	E. NAND of P33–P31
			101	F. NOR of P33–P31, P00, P07
			110	G. NAND of P33–P31, P00, P07
			111	H. NAND of P33–P31, P22–P20
Reserved	10		00	Reserved (Must be 0)

Table 21.SMR2(F)0DH:Stop	Mode Recovery	Register	2*
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Notes:

* Port pins configured as outputs are ignored as a SMR recovery source. † Indicates the value upon Power-On Reset

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

Table 24. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.

Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

D7	D6	D5	D4	D3	D2	D1	D0	
								 0 P34 as Port Output * 1 Timer8 Output 0 Disable T8 Timeout Interrupt * * 1 Enable T8 Timeout Interrupt 0 Disable T8 Data Capture Interrupt * * 1 Enable T8 Data Capture Interrupt * * 1 Enable T8 Data Capture Interrupt 00 SCLK on T8* * 00 SCLK on T8* * 01 SCLK/2 on T8 10 SCLK/4 on T8 11 SCLK/8 on T8 R 0 No T8 Counter Timeout * * R 1 T8 Counter Timeout Occurred W 0 No Effect W 1 Reset Flag to 0 0 Modulo-N * 1 Single Pass R 0 T8 Disabled * R 1 T8 Enabled W 0 Stop T8 W 4 Enable T9
								VV I ETIADIE IO

* Default setting after reset.

* * Default setting after Reset.. Not reset with a Stop-Mode recovery.

Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)

R247 P3M(F7H)

* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)

R250 IRQ(FAH)

Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)

* Default setting after reset

* * Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)

R254 SPH(FEH)

Figure 56. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

Stack Pointer Low Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFH: Read/Write)

Package Information

Package information for all versions of ZGP323H is depicted in Figures 59 through Figure 68.

Figure 58. 20-Pin CDIP Package

Figure 59. 20-Pin PDIP Package Diagram

CONTROLLING DIMENSIONS : INCH

ZGP323H Product Specification

Ordering Information

32KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4832C	48-pin SSOP 32K OTP	ZGP323HSS2832C	28-pin SOIC 32K OTP
ZGP323HSP4032C	40-pin PDIP 32K OTP	ZGP323HSH2032C	20-pin SSOP 32K OTP
ZGP323HSK2832E	28-pin CDIP 32K OTP	ZGP323HSK2032E	20-pin CDIP 32K OTP
ZGP323HSK4032E	40-pin CDIP 32K OTP	ZGP323HSP2032C	20-pin PDIP 32K OTP
ZGP323HSH2832C	28-pin SSOP 32K OTP	ZGP323HSS2032C	20-pin SOIC 32K OTP
ZGP323HSP2832C	28-pin PDIP 32K OTP		

32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4832C	48-pin SSOP 32K OTP	ZGP323HES2832C	28-pin SOIC 32K OTP
ZGP323HEP4032C	40-pin PDIP 32K OTP	ZGP323HEH2032C	20-pin SSOP 32K OTP
ZGP323HEH2832C	28-pin SSOP 32K OTP	ZGP323HEP2032C	20-pin PDIP 32K OTP
ZGP323HEP2832C	28-pin PDIP 32K OTP	ZGP323HES2032C	20-pin SOIC 32K OTP

32KB Automotive Temperature: -40° to +125°C					
Part Number	Description	Part Number	Description		
ZGP323HAH4832C	48-pin SSOP 32K OTP	ZGP323HAS2832C	28-pin SOIC 32K OTP		
ZGP323HAP4032C	40-pin PDIP 32K OTP	ZGP323HAH2032C	20-pin SSOP 32K OTP		
ZGP323HAH2832C	28-pin SSOP 32K OTP	ZGP323HAP2032C	20-pin PDIP 32K OTP		
ZGP323HAP2832C	28-pin PDIP 32K OTP	ZGP323HAS2032C	20-pin SOIC 32K OTP		
Replace C with G fo	r Lead-Free Packaging				

ZGP323H Z8[®] OTP Microcontroller with IR Timers

28-pin DIP/SOIC/SSOP 6 40- and 48-pin 8 40-pin DIP 7 48-pin SSOP 8 pin functions port 0 (P07 - P00) 18 port 0 (P17 - P10) 19 port 0 configuration 19 port 1 configuration 20 port 2 (P27 - P20) 20 port 2 (P37 - P30) 21 port 2 configuration 21 port 3 configuration 22 port 3 counter/timer configuration 24 reset) 25 XTAL1 (time-based input 18 XTAL2 (time-based output) 18 ping-pong mode 48 port 0 configuration 19 port 0 pin function 18 port 1 configuration 20 port 1 pin function 19 port 2 configuration 21 port 2 pin function 20 port 3 configuration 22 port 3 pin function 21 port 3counter/timer configuration 24 port configuration register 55 power connections 3 power supply 5 program memory 25 map 26 R ratings, absolute maximum 10 register 61 CTR(D)01h 35 CTR0(D)00h 33 CTR2(D)02h 37 CTR3(D)03h 39 flag 80 HI16(D)09h 32

HI8(D)0Bh 32 interrupt priority 78 interrupt request 79 interruptmask 79 L016(D)08h 32 L08(D)0Ah 32 LVD(D)0Ch 65 pointer 80 port 0 and 1 77 port 2 configuration 75 port 3 mode 76 port configuration 55, 75 SMR2(F)0Dh 40 stack pointer high 81 stack pointer low 81 stop mode recovery 57 stop mode recovery 2 61 stop-mode recovery 73 stop-mode recovery 274 T16 control 69 T8 and T16 common control functions 67 T8/T16 control 70 TC16H(D)07h 32 TC16L(D)06h 33 TC8 control 66 TC8H(D)05h 33 TC8L(D)04h 33 voltage detection 71 watch-dog timer 75 register description Counter/Timer2 LS-Byte Hold 33 Counter/Timer2 MS-Byte Hold 32 Counter/Timer8 Control 33 Counter/Timer8 High Hold 33 Counter/Timer8 Low Hold 33 CTR2 Counter/Timer 16 Control 37 CTR3 T8/T16 Control 39 Stop Mode Recovery2 40 T16 Capture LO 32 T8 and T16 Common functions 35 T8_Capture_HI 32