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Zilog - ZGP323HES2008C00TR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hes2008c00tr

Email: info@E-XFL.COM

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Figure 68.	48-Pin SSOP Package Design		J



Capacitance

Table 8 lists the capacitances.

Table 8. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^{\circ} \text{ C}$, $V_{CC} = \text{GND} = 0 \text{ V}$, f = 1.0 MH	Iz, unmeasured pins returned to GND

DC Characteristics

Table 9. GP323HS DC Characteristics

T _A =0°C to +70°C										
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions N	lotes		
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5 5	5		
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator			
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator			
VIH	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V				
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.2 V _{CC}	V				
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	$I_{OH} = -0.5 \text{mA}$			
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA			
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$			
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA			
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV				
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{CC} 1.75	V				
IIL	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled			
R _{PU}	Pull-up Resistance	2.0V	225		675	KΩ	V _{IN} = 0V; Pullups selected by mask			
-		3.6V	75		275	KΩ	option			
		5.0V	40		160	KΩ				



Table 11. GP323HA DC Characteristics

T _A = -40°C to +125°C										
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions	Notes		
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5		
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator			
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} –0.3		0.4	V	Driven by External Clock Generator			
V _{IH}	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V				
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.2 V _{CC}	V				
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	I _{OH} = -0.5mA			
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA			
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$			
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA			
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV				
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V				
IIL	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled			
R _{PU}	Pull-up Resistance	2.0V	200		700	KΩ	V _{IN} = 0V; Pullups selected by mask			
		3.6V	50		300	KΩ	option			
		5.0V	25		175	KΩ	_			
I _{OL}	Output Leakage	2.0-5.5	-1		1	μΑ	$V_{IN} = 0V, V_{CC}$			
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2		
		3.6V		5	10	mA	at 8.0 MHz	1, 2		
		5.5V		10	15	mA	at 8.0 MHz	1, 2		
I _{CC1}	Standby Current	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6		
	(HALI Mode)	3.6V		0.8	2.0	mA	$V_{IN} = 0V$, Clock at 8.0MHz	1, 2, 6		
<u> </u>		5.5V		1.3	3.2	mA	$V_{IN} = 0V$, Clock at 8.0MHz	1, 2, 6		
I _{CC2}	Standby Current (Stop	2.0V		1.6	15	μA	$V_{IN} = 0$ V, V_{CC} WDT not Running	3		
	Mode)	3.6V		1.8	20	μA	$V_{IN} = 0$ V, V_{CC} WDT not Running	3		
		5.5V		1.9	25	μΑ	$v_{IN} = 0$ V, v_{CC} WDT not Running	3		
		2.00		о 0	30	μΑ	$v_{IN} = 0$ V, v_{CC} WDT is Running	ა ი		
		3.0V 5.5V		0 15	40 60	μΑ	$v_{IN} = 0.0$, v_{CC} wDT is Running	ა ვ		
	Chan allow Course at	0.00		10	00	μΑ	$V_{\rm IN} = 0.0$, $V_{\rm CC}$ with the Ruthing	3		
	(Low Voltage)			1.2	0	μΑ		4		
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.			
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V				







Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—



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Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 22. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.



Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

RESET (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The Z8 GP does not assert the $\overline{\text{RESET}}$ pin when under VBO.



Note: The external Reset does not initiate an exit from STOP mode.

Functional Description

This device incorporates special functions to enhance the Z8[®], functionality in consumer and battery-operated applications.

Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

RAM

This device features 256B of RAM. See Figure 14.





Expanded Reg. Bank 0/Group 15" Register Pointer [7] [5] [4] [3] [2] [10] Working Register Group Pointer Bank Pointer FF FP Bank Pointer FF FP Bank Pointer FF FF FF FF Bank Pointer FF FF		Z8 [®] Standard Control Registers								
Register Pointer FF SPL FE U <td></td> <td></td> <td>Expanded Reg. Bank 0/Group 15</td> <td>** D7 D6 D</td> <td>5 D4</td> <td>D3</td> <td>D2[</td> <td>D1 D0</td>			Expanded Reg. Bank 0/Group 15	** D7 D6 D	5 D4	D3	D2[D1 D0		
Register Pointer Image: Construction of the second of					1	ii				
Register Pointer T D										
Register Pointer U <			FD RP		0	0	0			
7 6 5 4 3 2 1 0		Register Pointer	FC FLAGS							
Working Register Group Pointer Expanded Register Bank Pointer FA IRQ 0 <td< td=""><td>7</td><td>7 6 5 4 3 2 1 0</td><td>FB IMB</td><td></td><td></td><td></td><td></td><td></td></td<>	7	7 6 5 4 3 2 1 0	FB IMB							
Working Register Expanded Register F3 F3 <td></td> <td></td> <td>FA IBO</td> <td></td> <td>0</td> <td>0</td> <td>0</td> <td></td>			FA IBO		0	0	0			
Ordop Pollies Dirth Antes PB PD1M 1 0 <t< td=""><td>Working Regist</td><td>ter Expanded Regist</td><td>er F9 IPR</td><td></td><td></td><td></td><td></td><td></td></t<>	Working Regist	ter Expanded Regist	er F9 IPR							
F7 P3M 0	Group Pointer	Dank Fonter	F8 P01M	1 1 0	0	1	1	1 1		
F6 P2M 1			F7 P3M		0	0	0	0 0		
F5 Reserved I			F6 P2M	1 1 1	1	1	1	1 1		
F4 Reserved F3 Reserved F3 Reserved F4 Reserved F5 Reserved F6 F6 F6 F7 F7 F8 F8 F8 F7 F8 F8 F8 F9 F8 <td></td> <td></td> <td>F5 Reserved</td> <td></td> <td></td> <td>$\frac{1}{1}$</td> <td>ii l</td> <td></td>			F5 Reserved			$\frac{1}{1}$	ii l			
Fig Reserved U			F4 Reserved			11	U			
File (Bank 0)** File (Bank 0)** File (Bank 0)** File Reserved U			F3 Reserved		U U	U	U			
Findersterning (bank 0)** Findersterning (bank 0)**			F2 Reserved		U U	U	Ŭ			
F0 Reserved U	FF	Register File (Bank 0)	F1 Reserved		U U	Ŭ	U	υυ		
Image: Second State Sta	Fo		F0 Reserved		U U	Ŭ	U			
Figure 1 Expanded Reg. Bank F/Group 0** (F) 0F WD 1MR (F) 0F WD 1MR (F) 0F Reserved (F) 0F Reserved (F) 0R Reserved						1-1	~			
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F) OD SMR2 0			(F) 0E Reserved			Π				
7F F			* (F) 0D SMR2	0 0 0	0	0	0	0 0		
7F (F) 0B SMR U 0 1 0 0 0 U 0 (F) 0B Reserved (F) 0B Reserved (F) 0B Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved </td <td>_</td> <td></td> <td>(F) 0C Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	_		(F) 0C Reserved							
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0F (F) 07 Reserved (F) 06 Reserved (F) 06 Reserved (F) 05 Reserved (F) 07 Reserved (F) 04 Reserved (F) 07 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 04 Reserved (F) 04 Reserved			(F) 08 Reserved							
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0F 0F <td< td=""><td></td><td></td><td>(F) 06 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 06 Reserved							
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00 Image: constraint of the set with a Stop-Mode Recovery 1 <td>0F</td> <td><u> </u>₩/</td> <td>(F) 04 Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	0F	<u> </u> ₩/	(F) 04 Reserved							
Expanded Reg. Bank 0/Group (0) (F) 02 Reserved 1	00		(F) 03 Reserved							
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Expanded Reg. Bank 0/Group (0) (0) 03 P3 0 U (0) 02 P2 U * (0) 01 P1 U (0) 00 P0 U (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** His 5 Is not reset with a Stop-Mode Recovery ** (D) 04 TC8L 0 <			(F) 01 Reserved							
(0) 03 P3 0 U (0) 02 P2 U * (0) 01 P1 U (0) 00 P0 U * (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ^* (D) 05 TC8H 0	Expa	anded Reg. Bank 0/Group (0)	(F) 00 PCON	1 1 1	1	1	1	1 0		
(0) 03 P3 0			Expanded Reg. Bank D/Group 0							
(b) 02 P2 U * (0) 01 P1 U (0) 00 P0 U U = Unknown * * All addresses are in hexadecimal * ↑ Bit 5 Is not reset with a Stop-Mode Recovery ** (D) 04 ** (D) 05 ** (D) 06 ** (D) 07 ** (D) 08 ** (D) 08 ** (D) 07 ** (D) 08 ** (D) 07 ** (D) 06 ** (D) 06 ** (D) 07 ** (D) 06 ** (D) 07 ** (D) 08 ** (D) 08 ** (D) 04 ** (D) 05 ** (D) 04 ** (D) 03 ** (D) 02 ** (D) 01 ** (D) 01 ** (D) 01 ** (D) 01 ** (D) 02 ** (D) 01 (D) 0	(0) 03 P3	U U		UUI	υ	U	U	υn		
* (0) 01 P1 U (0) 01 P1 U (0) 00 P0 U * (D) 00 A LO8 0<	(0) 02 P2	U	* (D) 0B HI8	0 0 0	0	0	0	0 0		
(b) 01 1 1 0	* (0) 01 P1	U	* (D) 0A 08	0 0 0	0	0	0	0 0		
(0) 00 P0 U U = Unknown (D) 08 LO16 0	(0) 011 1	<u> </u>	* (D) 09 HI16	0 0 0	0	0	0	0 0		
U = Unknown * (D) 07 TC16H 0 <td>(0) 00 P0</td> <td>U</td> <td>* (D) 08 LO16</td> <td>0 0 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td>	(0) 00 P0	U	* (D) 08 LO16	0 0 0	0	0	0	0 0		
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⁺ Is not reset with a Stop-Mode Recovery, except Bit 0 ⁺ 1bit 5 Is not reset with a Stop-Mode Recovery ⁺ (D) 04 TC8L ⁻ 0 0 0 0 0 0 0 0 0 0 0 ⁺ (D) 03 CTR3 ⁻ 0 0 0 0 1 1 1 1 1 ⁺ 1 ⁺ (D) 02 CTR2 ⁻ 0 0 0 0 0 0 0 0 0 ⁻ 1 1 1 1 ⁺	** All addresses are in beyade	ecimal	* (D) 05 TC8H	0 0 0	0	0	0	0 0		
	↑ Is not reset with a Stop-Mo	de Recovery, except Bit 0	* (D) 04 TC8L	0 0 0	0	0	0	0 0		
[↑] ↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery [↑] ↑↑↑ [↑] ↑↑↑ [↑] ↑↑↑ [↑] ↑↑↑↑ [↑] ↑↑↑ [↑] ↑↑ [↑] ↑ [↑]	↑↑ Bit 5 Is not reset with a Sto	p-Mode Recovery	1↑ (D) 03 CTR3	0 0 0	1	1	1	1 1		
^{↑↑↑↑} Bits 5 and 4 not reset with a Stop-Mode Recovery ^{↑↑↑↑↑} (D) 01 CTR1 (D) 01 CTR1 (D) 0 0 0 0 0 0 0 0 (D) 01 CTR1 (D) 00 CTR0 (D)	↑↑↑ Bits 5,4,3.2 not reset with	a Stop-Mode Recoverv	↑↑↑ (D) 02 CTR2	0 0 0	0	0	0	0 0		
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery ↑↑↑↑↑↓ (D) 00 CTR0 0 0 0 0 0 0 0 0 0 0	↑↑↑↑ Bits 5 and 4 not reset with	a Stop-Mode Recovery	↑↑↑↑ (D) 01 CTR1	0 0 0	0	0	0	0 0		
	↑↑↑↑↑ Bits 5,4,3,2,1 not reset wit	th a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	0 0 0	0	0	0	0 0		

Figure 15. Expanded Register File Architecture







Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



T8/T16_Logic/Edge _Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to "NORMAL OPERATION Mode" terminates the "PING-PONG Mode" operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Note: Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 17 lists and briefly describes the fields for this register.







Figure 19. Transmit Mode Flowchart



Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.







Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put





Figure 28. Ping-Pong Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.





The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.



Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T _{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	Т8	8,9	Internal
IRQ5	LVD	10,11	Internal

Table 19. Interrupt Types, Sources, and Vectors

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All ZGP323H interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 20.

I	RQ	Interrupt Edge				
D7	D6	IRQ2 (P31)	IRQ0 (P32)			
0	0	F	F			
0	1	F	R			
1	0	R	F			
1	1	R/F	R/F			
Note: F = Falling Edge; R = Rising Edge						

Table 20. IRQ Register



Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XORgate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/ TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address OBH.





СП	R1(0L))01H							
D7	D6	D5	D4	D3	D2	D1	D0		
									Transmit Mode* R/W 0 T16_OUT is 0 initially 1 T16_OUT is 1 initially Demodulation Mode R 0 No Falling Edge Detection R 1 Falling Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* R/W 0 T8_OUT is 0 initially* 1 T8_OUT is 1 initially Demodulation Mode R 0 No Rising Edge Detection R 1 Rising Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* 0 0 Normal Operation* 0 1 Ping-Pong Mode 1 0 T16_OUT = 0 1 1 T16_OUT = 1 Demodulation Mode 0 0 No Filter 0 1 4 SCLK Cycle Filter 1 0 8 SCLK Cycle Filter 1 0 R SCLK Cycle Filter 1 0 R SCLK Cycle Filter 1 0 NOR 1 0 NOR 1 1 NAND Demodulation Mode 0 0 0 Falling Edge Detection
									 0 0 Falling Edge Detection 0 1 Rising Edge Detection 1 0 Both Edge Detection 1 1 Reserved Transmit Mode*
	L								0 P36 as Port Output * 1 P36 as T8/T16_OUT Demodulation Mode 0 P31 as Demodulator Input 1 P20 as Demodulator Input
* De **De recc	efault se efault se overy.	etting after etting aft	er Res er Res	et et Not	reset v	with a S	Stop-N	lode	Transmit/Demodulation Mode 0 Transmit Mode * 1 Demodulation Mode

Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)







Notes: Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



R249 IPR(F9H)



Figure 51. Interrupt Priority Register (F9H: Write Only)







	MILLIMETER		INCH			
MIN	NOM	MAX	MIN	NOM	MAX	
1.73	1.85	1.98	0.068	0.073	0.078	
0.05	0.13	0.21	0.002	0.005	0.008	
1.68	1.73	1.83	0.066	0.068	0.072	
0.25	0.30	0.38	0.010	0.012	0.015	
0.13	0.15	0.22	0.005	0.006	0.009	
7.07	7.20	7.33	0.278	0.283	0.289	
5.20	5.30	5.38	0.205	0.209	0.212	
	0.65 BSC		0.0256 BSC			
7.65	7.80	7.90	0.301	0.307	0.311	
0.56	0.75	0.94	0.022	0.030	0.037	
0.74	0.78	0.82	0.029	0.031	0.032	
	MIN 1.73 0.05 1.68 0.25 0.13 7.07 5.20 7.65 0.56 0.74	MILLIMETER MIN NOM 1.73 1.85 0.05 0.13 1.68 1.73 0.25 0.30 0.13 0.15 7.07 7.20 5.20 5.30 0.65 BSC 7.65 7.80 0.56 0.75 0.74 0.78	MILLIMETER MIN NOM MAX 1.73 1.85 1.98 0.05 0.13 0.21 1.68 1.73 1.83 0.25 0.30 0.38 0.13 0.15 0.22 7.07 7.20 7.33 5.20 5.30 5.38 0.65 BSC 7.65 7.80 7.90 0.56 0.75 0.94 0.74 0.78 0.82	MILLIMETER MIN NOM MAX MIN 1.73 1.85 1.98 0.068 0.05 0.13 0.21 0.002 1.68 1.73 1.83 0.066 0.25 0.30 0.38 0.010 0.13 0.15 0.22 0.005 7.07 7.20 7.33 0.278 5.20 5.30 5.38 0.205 0.65 BSC - - 7.65 7.80 7.90 0.301 0.56 0.75 0.94 0.022 0.74 0.78 0.82 0.029	MILLIMETER INCH MIN NOM MAX MIN NOM 1.73 1.85 1.98 0.068 0.073 0.05 0.13 0.21 0.002 0.005 1.68 1.73 1.83 0.066 0.068 0.25 0.30 0.38 0.010 0.012 0.13 0.15 0.22 0.005 0.006 7.07 7.20 7.33 0.278 0.283 5.20 5.30 5.38 0.205 0.209 O.055 BSC 7.65 7.80 7.90 0.301 0.307 0.56 0.75 0.94 0.022 0.030 0.74 0.78 0.82 0.029 0.31	



DETAIL A

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Figure 61. 20-Pin SSOP Package Diagram











Figure 63. 28-Pin CDIP Package Diagram



SYMBOL	OPT #	MILLIMETER		INCH	
		MíN	MAX	MIN	MAX
A1		0.38	1.02	.015	.040
A2		3.18	4.19	.125	.165
В		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
С		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 BSC	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.40	1.91	.055	.075
	02	1.40	1.78	.055	.070
s	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

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01

02

STANDARD

Figure 64. 28-Pin PDIP Package Diagram



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

- 323 = Family Designation
- H = High Voltage
- T = Temparature
 - S = Standard 0° to +70°C
 - $E = Extended 40^{\circ} to + 105^{\circ}C$
 - A = Automotive -40° to $+125^{\circ}$ C
- P = Package Type:
 - K = CDIP
 - P = PDIP
 - H = SSOP
 - S = SOIC

= Number of Pins

- CC = Memory Size
- M = Molding Compound
- C = Standard Plastic Packaging Molding Compound
- G = Green Plastic Molding Compound
- E = Standard Cer Dip flow