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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hes2008g



Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Document

Date	Revision Level	Section	Description	Page #
December 2004	02		Changed low power consumption, STOP and HALT mode current values, deleted mask option note, clarified temperature ranges in Tables 6 and 8 and 10. Added new Tables 9 and 10. Also added Characterization data to Table 11 and changed Program/Erase Endurance value in Table 12.	1,2,10 11,12, 13,14, 15
			Removed Preliminary designation	All
March 2005	03		Minor change to Table 9 Electrical Characteristics. Added 20, 28 and 40-pin CDIP parts in the Ordering Section.	11,90



Development Features

Table 2 lists the features of ZiLOG[®]'s ZGP323H members.

Table 2. Features

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323H OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–5.5V

- Low power consumption—18mW (typical)
- T = Temperature
S = Standard 0° to +70°C
E = Extended -40° to +105°C
A = Automotive -40° to +125°C
- Three standby modes:
 - STOP— (typical 1.8μA)
 - HALT— (typical 0.8mA)
 - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
 - One programmable 8-bit counter/timer with two capture registers and two load registers
 - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
 - Programmable input glitch filter for pulse reception
- Six priority interrupts
 - Three external
 - Two assigned to counter/timers
 - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
 - Port 0: 0–3 pull-up transistors
 - Port 0: 4–7 pull-up transistors

Capacitance

Table 8 lists the capacitances.

Table 8. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{MHz}$, unmeasured pins returned to GND	

DC Characteristics

Table 9. GP323HS DC Characteristics

Symbol	Parameter	V_{CC}	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$			Units	Conditions	Notes
			Min	Typ(7)	Max			
V_{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-5.5	$0.8 V_{CC}$		$V_{CC}+0.3$	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-5.5	$V_{SS}-0.3$		0.4	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-5.5	$0.7 V_{CC}$		$V_{CC}+0.3$	V		
V_{IL}	Input Low Voltage	2.0-5.5	$V_{SS}-0.3$		$0.2 V_{CC}$	V		
V_{OH1}	Output High Voltage	2.0-5.5	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{mA}$	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	$V_{CC}-0.8$			V	$I_{OH} = -7\text{mA}$	
V_{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0\text{mA}$	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	$I_{OL} = 10\text{mA}$	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-5.5	0		V_{CC} 1.75	V		
I_{IL}	Input Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0\text{V}$, V_{CC} Pull-ups disabled	
R_{PU}	Pull-up Resistance	2.0V	225		675	$\text{K}\Omega$	$V_{IN} = 0\text{V}$; Pullups selected by mask option	
		3.6V	75		275	$\text{K}\Omega$		
		5.0V	40		160	$\text{K}\Omega$		

Table 11. GP323HA DC Characteristics

T_A = -40°C to +125°C								
Symbol	Parameter	V_{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	I _{OH} = -0.5mA	
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	I _{OL} = 4.0mA	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V		
I _{IL}	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled	
R _{PU}	Pull-up Resistance	2.0V	200		700	KΩ	V _{IN} = 0V; Pullups selected by mask option	
		3.6V	50		300	KΩ		
		5.0V	25		175	KΩ		
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC}	
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I _{CC1}	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I _{CC2}	Standby Current (Stop Mode)	2.0V		1.6	15	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		3.6V		1.8	20	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		5.5V		1.9	25	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		2.0V		5	30	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		3.6V		8	40	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		5.5V		15	60	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V		



Table 11. GP323HA DC Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A = -40°C to +125°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
V _{HVD}	V _{CC} High Voltage Detection			2.7		V		

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V_{CC} and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

Table 12. EPROM/OTP Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	100			Cycles	1

Notes:

1. For windowed cerdip package only.
2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

$$AF = \exp[(E_a/k) * (1/T_{use} - 1/T_{stress})]$$

Where:

E_a is the intrinsic activation energy (eV; typ. 0.8)

k is Boltzman's constant (8.67 x 10⁻⁵ eV/°K)

°K = -273.16°C

T_{use} = Use Temperature in °K

T_{stress} = Stress Temperature in °K

3. At a stable UV Lamp output of 20mW/CM²



Table 13. AC Characteristics

				T _A =0°C to +70°C (S) –40°C to +105°C (E) –40°C to +125°C (A) 8.0MHz				Watch-Dog Timer Mode Register (D1, D0)
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes	
1	TpC	Input Clock Period	2.0–5.5	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–5.5		25	ns	1	
3	TwC	Input Clock Width	2.0–5.5	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 5.5	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–5.5	3TpC			1	
6	TpTin	Timer Input Period	2.0–5.5	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–5.5		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 5.5	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–5.5	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width Spec	2.0–5.5	12 5TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–5.5		5TpC		4	
12	Twdt	Watch-Dog Timer Delay Time	2.0–5.5 2.0–5.5 2.0–5.5 2.0–5.5	5 10 20 80		ms ms ms ms	0, 0 0, 1 1, 0 1, 1	
13	T _{POR}	Power-On Reset	2.0–5.5	2.5	10	ms		

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.

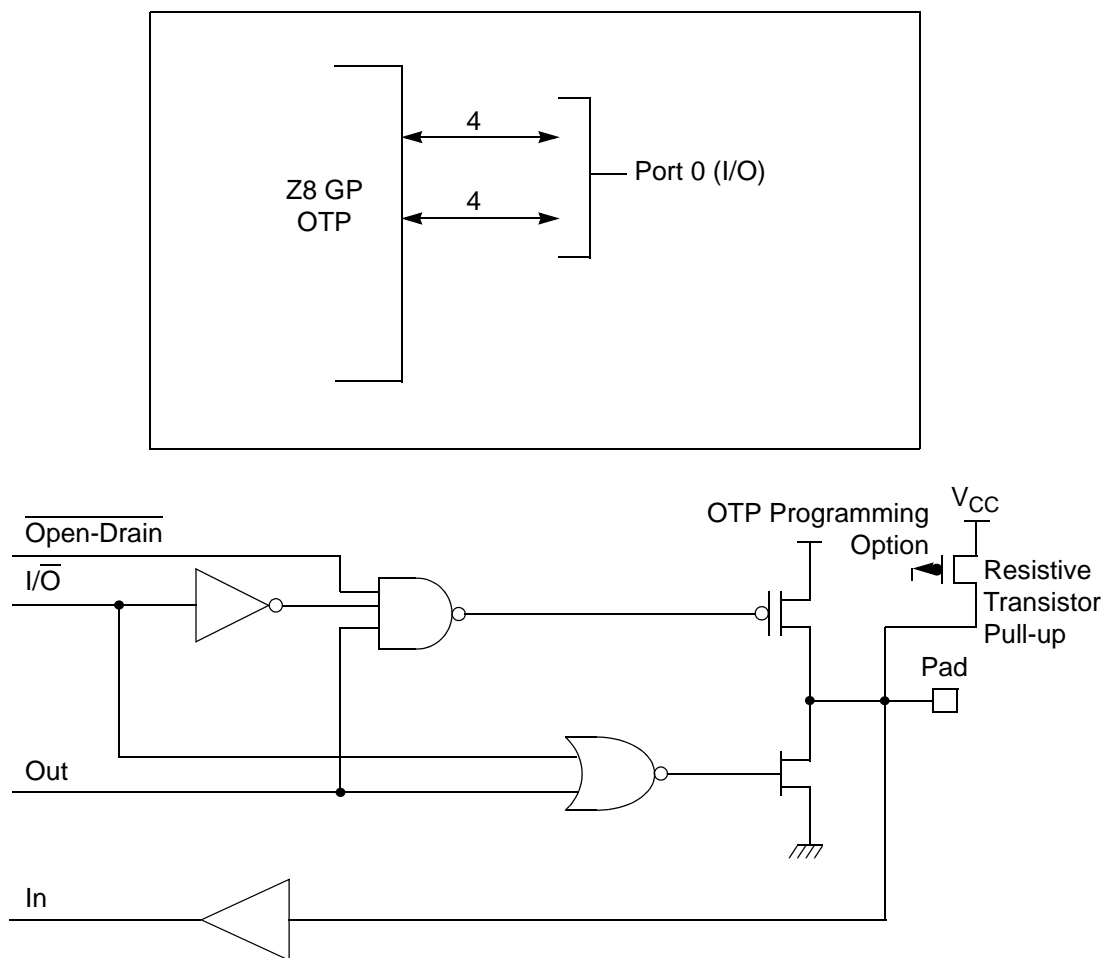


Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Note:** The Port 1 direction is reset to its default state following an SMR.

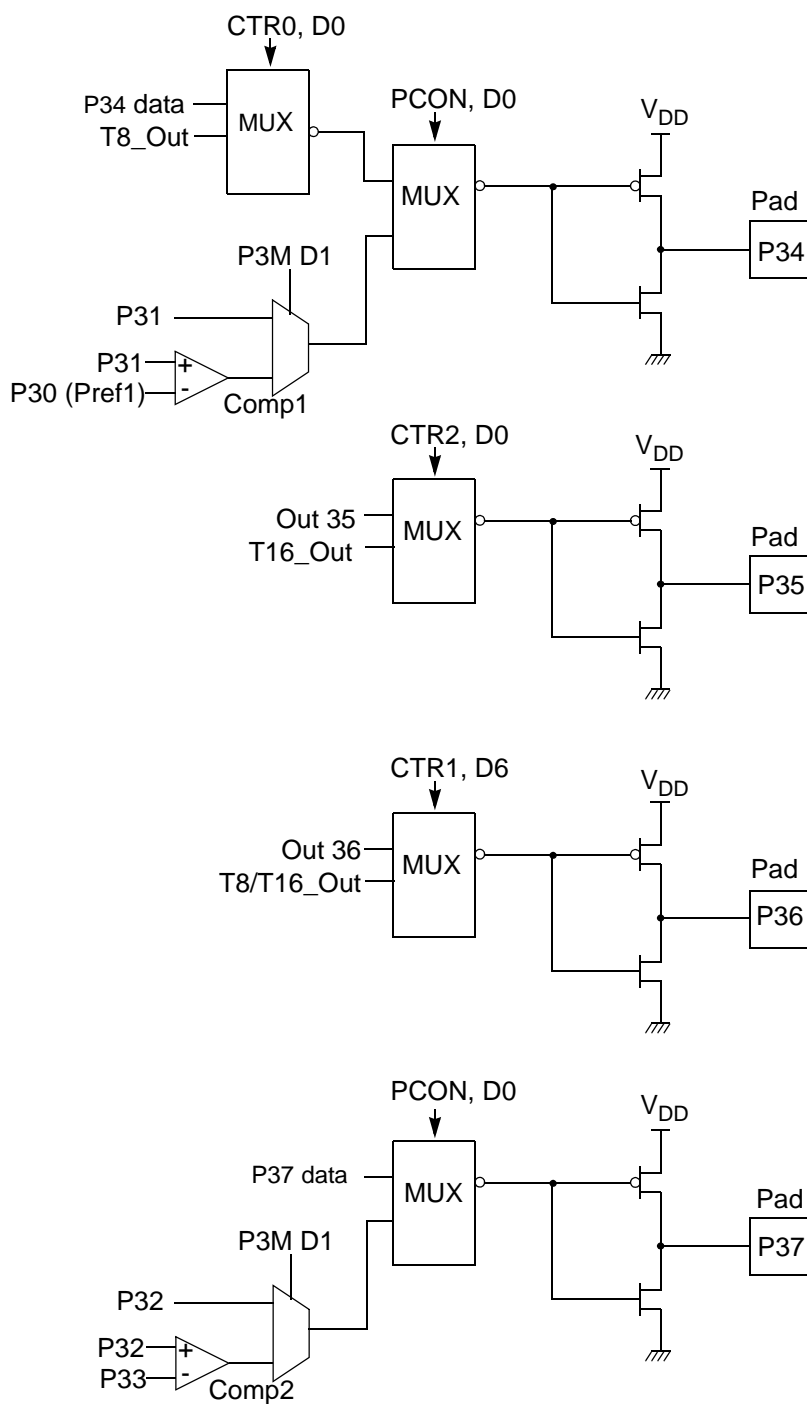


Figure 13. Port 3 Counter/Timer Output Configuration

Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position	Description
T16_Data_LO	[7:0]	R/W Data

Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position	Description
T8_Level_HI	[7:0]	R/W Data

Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position	Description
T8_Level_LO	[7:0]	R/W Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

Table 15. CTR0(D)00H Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-----	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5-----	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8_Clock	---43---	R/W	0 0**	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_Mask	----2--	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt

Table 15. CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	-----1-	R/W	0**	Disable Time-Out Interrupt
			1	Enable Time-Out Interrupt
P34_Out	-----0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.



Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

T8 Clock

This bit defines the frequency of the input signal to T8.



Table 16. CTR1(0D)01H T8 and T16 Common Functions (Continued)

Field	Bit Position		Value	Description
Transmit_Submode/ Glitch_Filter	----32--	R/W		Transmit Mode
			00*	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/ Rising Edge	-----1-	R/W	0*	Transmit Mode
			1	T8_OUT is 0 Initially
		R	0*	T8_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Rising Edge
			1	Rising Edge Detected
			0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/ Falling_Edge	-----0	R/W	0*	Transmit Mode
			1	T16_OUT is 0 Initially
		R	0*	T16_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Falling Edge
			1	Falling Edge Detected
			0	No Effect
			1	Reset Flag to 0

Note:

*Default at Power-On Reset

*Default at Power-On Reset. Not reset with Stop Mode recovery.

Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

P36_Out/Demodulator_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.



Table 17. CTR2(D)02H: Counter/Timer16 Control Register

Field	Bit Position		Value	Description
T16_Enable	7-----	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Transmit Mode
			1	Modulo-N
			0	Single Pass
			1	Demodulation Mode
Time_Out	--5-----	R	0*	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
		W	0	No Counter Timeout
			1	Counter Timeout Occurred
T16_Clock	---43---	R/W	00**	No Effect
			01	Reset Flag to 0
			10	SCLK
			11	SCLK/2
Capture_INT_Mask	-----2--	R/W	0**	SCLK/4
			1	SCLK/8
Counter_INT_Mask	-----1-	R/W	0*	Disable Data Capture Int.
			1	Enable Data Capture Int.
P35_Out	-----0	R/W	0*	Disable Timeout Int.
			1	Enable Timeout Int.

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T16_Enable

This field enables T16 when set to 1.

Single/Modulo-N

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.

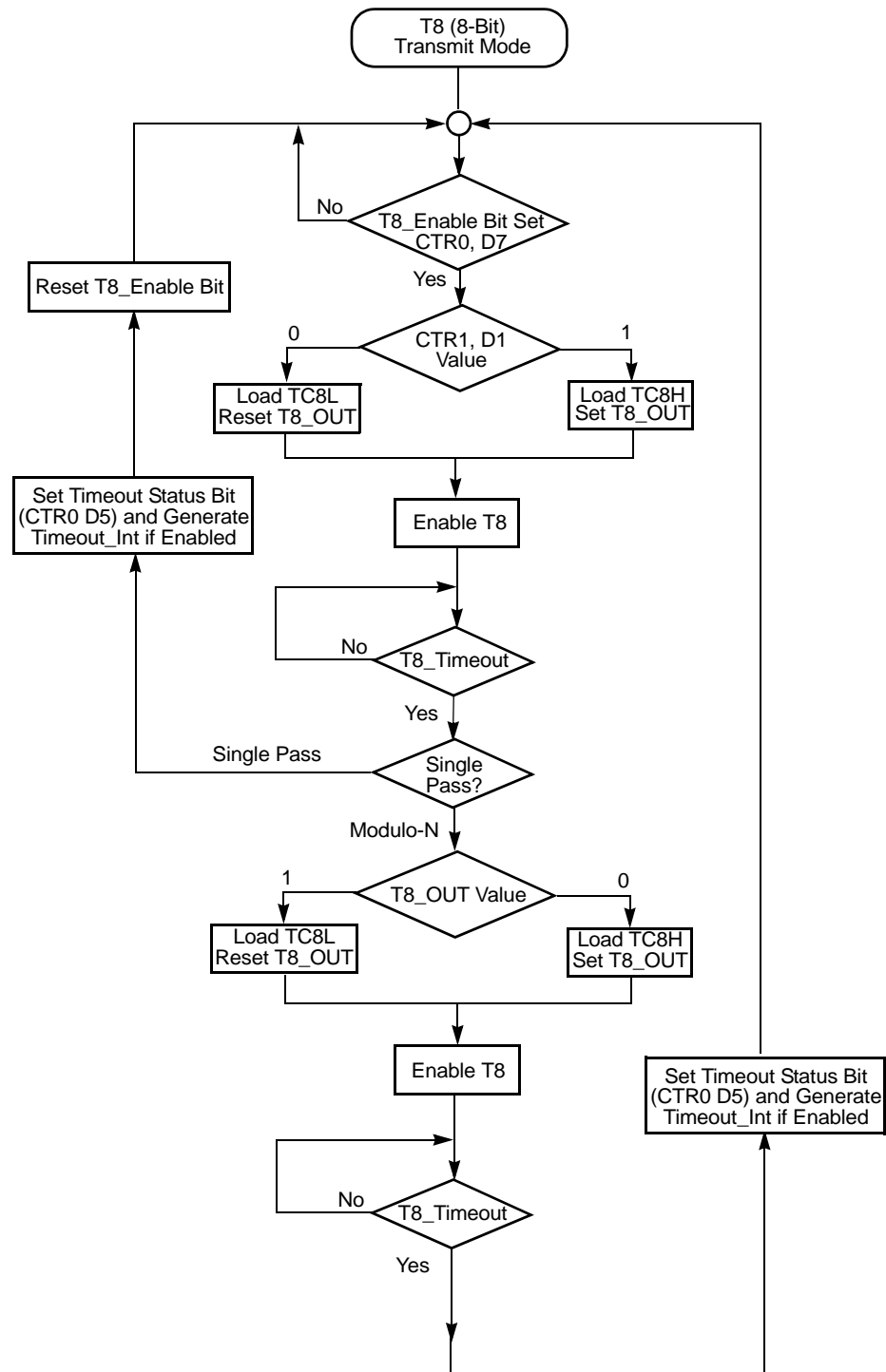


Figure 19. Transmit Mode Flowchart



Caution:

Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFE_H. Transition from 0 to FFFF_H is not a timeout condition.

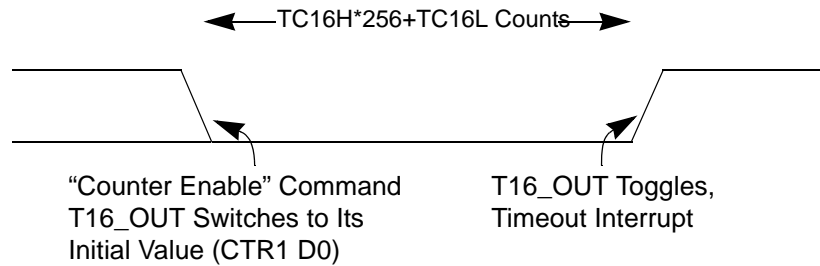


Figure 26. T16_OUT in Single-Pass Mode

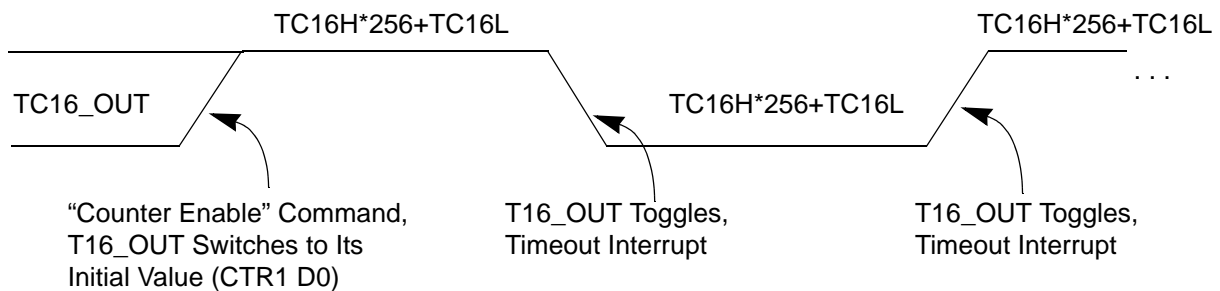


Figure 27. T16_OUT in Modulo-N Mode

T16 DEMODULATION Mode

The user must program TC16L and TC16H to FF_H. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFF_H and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

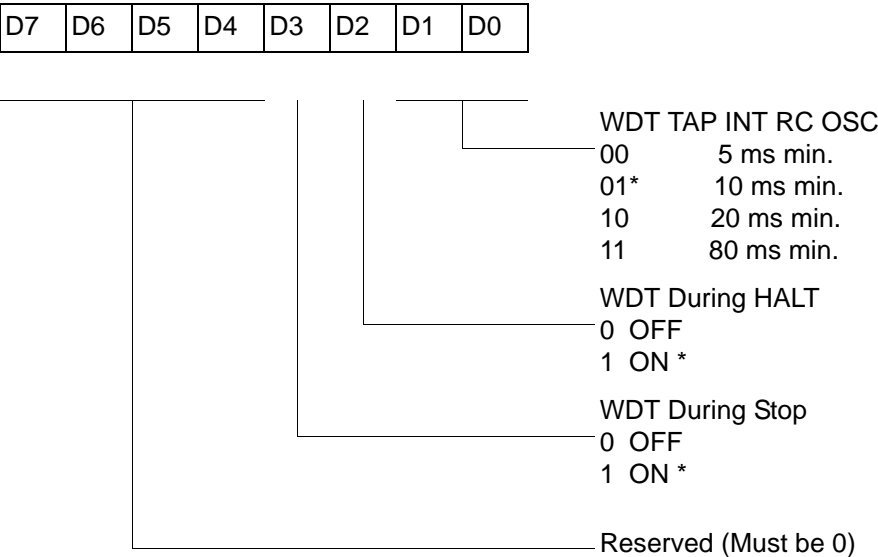


Watch-Dog Timer Mode Register (WDTMR)

The Watch-Dog Timer (WDT) is a retriggerable one-shot timer that resets the Z8[®] CPU if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction. On subsequent executions of the WDT instruction, the WDT is refreshed. The WDT circuit is driven by an on-board RC-oscillator. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source the internal RC-oscillator. Bits 0 and 1 of the WDT register control a tap circuit that determines the minimum timeout period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during Stop. Bits 4 through 7 are reserved (Figure 37). This register is accessible only during the first 60 processor cycles (120 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 36). After this point, the register cannot be modified by any means (intentional or otherwise). The WDTMR cannot be read. The register is located in Bank F of the Expanded Register Group at address location 0Fh. It is organized as shown in Figure 37.

WDTMR(0F)0Fh



* Default setting after reset

Figure 37. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 23.

Low-Voltage Detection Register—LVD(D)0Ch

- **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position	Description		
LVD	76543---	Reserved No Effect		
	----2--	R	1 0*	HVD flag set HVD flag reset
	-----1-	R	1 0*	LVD flag set LVD flag reset
	-----0	R/W	1 0*	Enable VD Disable VD

*Default after POR

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the V_{CC} level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V_{CC} is higher than V_{HVD} . The LVD flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD} . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.



R249 IPR(F9H)

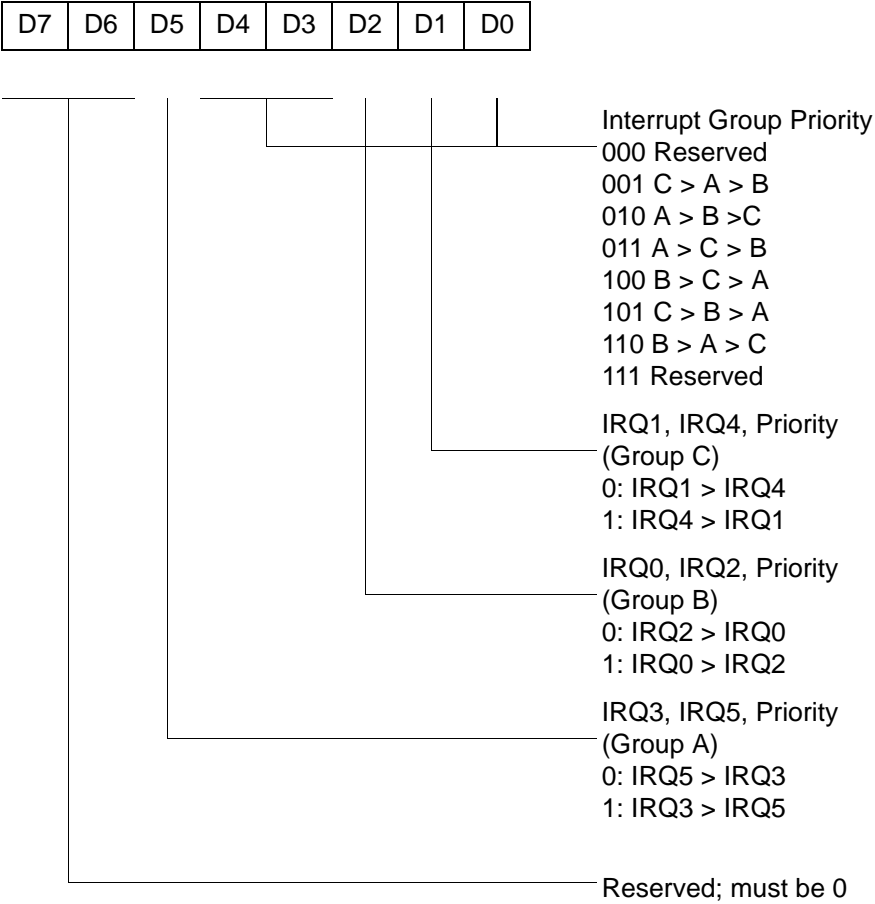
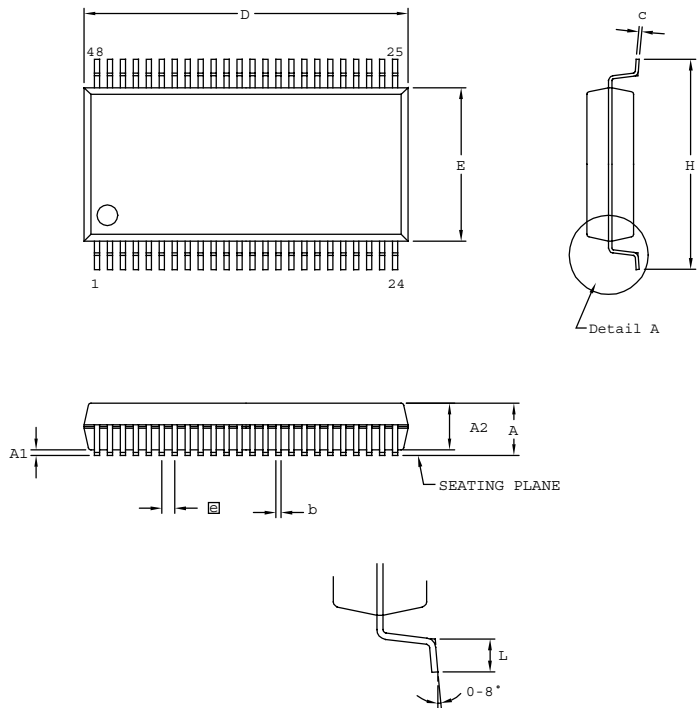


Figure 51. Interrupt Priority Register (F9H: Write Only)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
ⓐ	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

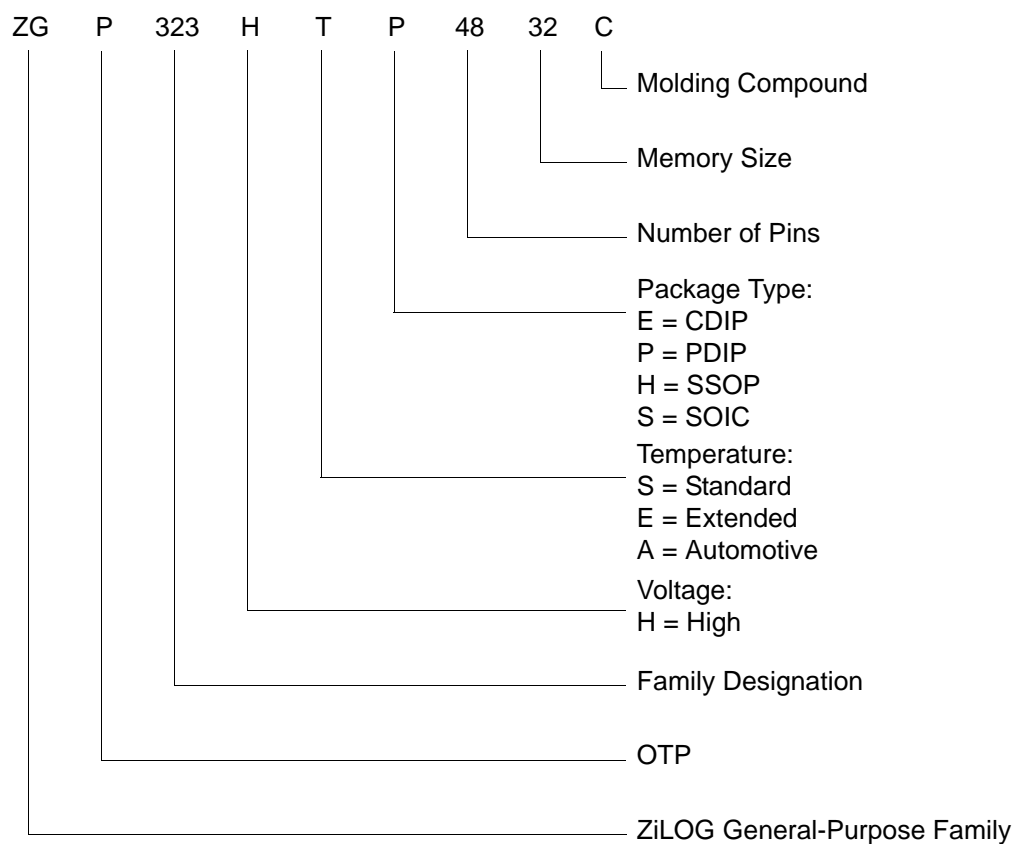
CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 68. 48-Pin SSOP Package Design

► **Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.



Example



- 28-pin DIP/SOIC/SSOP 6
- 40- and 48-pin 8
- 40-pin DIP 7
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 - reset) 25
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- port 1 pin function 19
- port 2 configuration 21
- port 2 pin function 20
- port 3 configuration 22
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 - interruptmask 79
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 - L08(D)0Ah 32
 - LVD(D)0Ch 65
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 - T8 and T16 Common functions 35
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