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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Obsolete
Z8
8-Bit
8MHz
-
HLVD, POR, WDT
16
16KB (16K x 8)
ОТР
-
237 x 8
2V ~ 5.5V
-
Internal
-40°C ~ 105°C (TA)
Surface Mount
20-SOIC (0.295", 7.50mm Width)
-
https://www.e-xfl.com/product-detail/zilog/zgp323hes2016c

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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Figure 68.	48-Pin SSOP Package Design		J

ZGP323H Product Specification



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ZGP323H Product Specification



	1	-	\			
NC		1	\bigcirc	48	_	NC
DOF		2		17	_	NC
F 20		2		47		NC DO4
P20		3		40		P24
P2/		4		45		P23
P04		5		44		P22
N/C		6		43		P21
P05	q	7		42		P20
P06		8		41		P03
P14		9		40		P13
P15		10		39		P12
P07		11	40 Dia	38		VSS
VDD		12	48-PIN	37		VSS
VDD		13	330P	36		N/C
N/C		14		35		P02
P16	Е	15		34		P11
P17		16		33		P10
XTAL2		17		32		P01
XTAL1		18		31		P00
P31		19		30		N/C
P32		20		29		PREF1/P30
P33		21		28		P36
P34		22		27		P37
NC		22		26		P35
VSS	Д	20		20	_	RESET
100	-	24		ZD		NEOL I

Figure 6. 48-Pin SSOP Pin Configuration

Table 6. 40- and 48-Pin Configuration

40-Pin PDIP #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12



Capacitance

Table 8 lists the capacitances.

Table 8. Capacitance

Parameter	Maximum			
Input capacitance	12pF			
Output capacitance	12pF			
I/O capacitance	12pF			
Note: $T_A = 25^{\circ}$ C, $V_{CC} = GND = 0$ V, f = 1.0 MHz, unmeasured pins returned to GND				

DC Characteristics

Table 9. GP323HS DC Characteristics

T₄=0°C to +70°C										
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions N	lotes		
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5 5	5		
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator			
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator			
VIH	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V				
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.2 V _{CC}	V				
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	$I_{OH} = -0.5 \text{mA}$			
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA			
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$			
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA			
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV				
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{CC} 1.75	V				
IIL	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled			
R _{PU}	Pull-up Resistance	2.0V	225		675	KΩ	V _{IN} = 0V; Pullups selected by mask			
-		3.6V	75		275	KΩ	option			
		5.0V	40		160	KΩ				



	T ₄ = -40°C to +105°C									
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions	Notes		
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA			
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$			
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA			
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV				
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V				
IIL	Input Leakage	2.0-5.5	-1		1	μΑ	V _{IN} = 0V, V _{CC} Pull-ups disabled			
R _{PU}	Pull-up Resistance	2.0V	200.0		700.0	KΩ	V _{IN} = 0V; Pullups selected by mask			
		3.6V	50.0		300.0	KΩ	option			
		5.0V	25.0		175.0	KΩ	_			
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0V, V_{CC}$			
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2		
		3.6V		5	10	mA	at 8.0 MHz	1, 2		
		5.5V		10	15	mA	at 8.0 MHz	1, 2		
I _{CC1}	Standby Current	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6		
	(HALT Mode)	3.6V		0.8	2.0	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6		
		5.5V		1.3	3.2	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6		
I _{CC2}	Standby Current (Stop	2.0V		1.6	12	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3		
	Mode)	3.6V		1.8	15	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3		
		5.5V		1.9	18	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3		
		2.0V		5	30	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3		
		3.6V		8	40	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3		
		5.5V		15	60	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3		
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4		
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.			
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V				
V _{HVD}	Vcc High Voltage Detection			2.7		V				

Table 10. GP323HE DC Characteristics (Continued)

Notes:

1. All outputs unloaded, inputs at rail.

2. CL1 = CL2 = 100 pF.

3. Oscillator stopped.

4. Oscillator stops when V_{CC} falls below V_{BO} limit.

 It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VCC and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

6. Comparator and Timers are on. Interrupt disabled.

7. Typical values shown are at 25 degrees C.



AC Characteristics





Figure 8. AC Timing Diagram







Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—





Figure 13. Port 3 Counter/Timer Output Configuration





Expanded Reg. Bank 0/Group 15" Register Pointer [7] [5] [4] [3] [2] [10] Working Register Group Pointer Bank Pointer FF FP Bank Pointer FF FP Bank Pointer FF FF FF FF Bank Pointer FF FF		Res	et C	Cond	itior	۱			
Register Pointer FF SPL FE U <thu< th=""> <thu< th=""> U U</thu<></thu<>		Expanded Reg. Bank 0/Group 15**							
Register Pointer Image: Construction of the second of					1	ii			
Register Pointer T D									
Register Pointer U <			FD RP		0	0	0		
7 6 5 4 3 2 1 0		Register Pointer	FC FLAGS						
Working Register Group Pointer Expanded Register Bank Pointer FA IRQ 0 <td< td=""><td>7</td><td>7 6 5 4 3 2 1 0</td><td>FB IMB</td><td></td><td></td><td></td><td></td><td></td></td<>	7	7 6 5 4 3 2 1 0	FB IMB						
Working Register Expanded Register F3 F3 <td></td> <td></td> <td>FA IBO</td> <td></td> <td>0</td> <td>0</td> <td>0</td> <td></td>			FA IBO		0	0	0		
Ordop Pollies Dirth Antes PB PD1M 1 0 <t< td=""><td>Working Regist</td><td>ter Expanded Regist</td><td>er F9 IPR</td><td></td><td></td><td></td><td></td><td></td></t<>	Working Regist	ter Expanded Regist	er F9 IPR						
F7 P3M 0	Group Pointer	Dank Fonter	F8 P01M	1 1 0	0	1	1	1 1	
F6 P2M 1			+ F7 P3M		0	0	0	0 0	
F5 Reserved I			F6 P2M	1 1 1	1	1	1	1 1	
F4 Reserved F3 Reserved F3 Reserved F4 Reserved F5 Reserved F6 F6 F6 F7 F7 F8 F8 F8 F7 F8 F8 F8 F9 F8 <td></td> <td></td> <td>F5 Reserved</td> <td></td> <td></td> <td>$\frac{1}{1}$</td> <td>ii l</td> <td></td>			F5 Reserved			$\frac{1}{1}$	ii l		
Fig Reserved U			F4 Reserved			11	U		
File (Bank 0)** File (Bank 0)** File (Bank 0)** File Reserved U			F3 Reserved		U U	U	U		
Findersterning (bank 0)** Findersterning (bank 0)**			F2 Reserved		U U	U	Ŭ		
F0 Reserved U	FF	Register File (Bank 0)	F1 Reserved		U U	Ŭ	U	υυ	
Image: Second State Sta	Fo		F0 Reserved		U U	Ŭ	U		
Figure 1 Expanded Reg. Bank F/Group 0** (F) 0F WD 1MR (F) 0F WD 1MR (F) 0F Reserved (F) 0F Reserved (F) 0R Reserved						1-1	~		
Image: constraint of the second state stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the			Expanded Reg. Bank F/Group 0*	*					
(F) 0E Reserved 0			(F) 0F WDTMR	U U O	0	1	1	0 1	
F) OD SMR2 0			(F) 0E Reserved			Π			
7F F			* (F) 0D SMR2	0 0 0	0	0	0	0 0	
7F (F) 0B SMR U 0 1 0 0 0 U 0 (F) 0B Reserved (F) 0B Reserved (F) 0B Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved </td <td>_</td> <td></td> <td>(F) 0C Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	_		(F) 0C Reserved						
(F) 0A Reserved (F) 09 Reserved (F) 06 Reserved (F) 06 Reserved (F) 07 Reserved (F) 06 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 09 Reserved (F) 07 Reserved (F) 00 Reserved (F) 00 Reserved (D) 00 C LVD (D) 0 0 0 0 0 0 0 0	7F	· ↓	↑ (F) 0B SMR	U 0 1	0	0	0	U 0	
(F) 09 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved		_	(F) 0A Reserved			Π			
(F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 00 PCON (F) 01 Reserved (O) 01 P1 U (O) 00 P0 U U = Unknown (D) 00 C T16L * 18 not reset with a Stop-Mode Recovery * 111 Bits 5,4,3,2 not reset with a Stop-Mode Recovery * 111 Bits 5,4,3,2,2 not reset with a			(F) 09 Reserved						
0F (F) 07 Reserved (F) 06 Reserved (F) 06 Reserved (F) 05 Reserved (F) 07 Reserved (F) 04 Reserved (F) 07 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 04 Reserved (F) 04 Reserved			(F) 08 Reserved						
0F (F) 06 Reserved (F) 05 Reserved (F) 04 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 03 P3 0 (F) 01 Reserved (F) 00 PCON (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 00 PCON (F) 01 Reserved (F) 01 P1 (F) 01 Reserved (D) 02 P2 (F) 00 PCON (F) 03 B Hil8 (F) 00 0 0 0 0 0 0 0 (D) 04 LO8 (F) 00 0 0 0 0 0 (F) 03 B LO16 (F) 00 0 0 0 0 0 (F) 04 C LD8 (F) 00 0 0 0 0 0 (D) 05 TC8H (F) 00 0 0 0 0 0 (F) 03 C TR3 (F) 0 0 0 0 0 0 (F) 04 TC8L (F) 0 0 0 0 0 0 (F) 04 C C R2<			(F) 07 Reserved						
0F 0F <td< td=""><td></td><td></td><td>(F) 06 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 06 Reserved						
0F 00 <td< td=""><td></td><td></td><td>(F) 05 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 05 Reserved						
00 Image: constraint of the set with a Stop-Mode Recovery 1 <td>0F</td> <td><u> </u>₩/</td> <td>(F) 04 Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	0F	<u> </u> ₩/	(F) 04 Reserved						
Expanded Reg. Bank 0/Group (0) (F) 02 Reserved 1	00		(F) 03 Reserved						
Expanded Reg. Bank 0/Group (0) (0) 03 P3 0 (0) 02 P2 U (0) 01 P1 U (0) 01 P1 U (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** Di 03 CTR3 0 ** (D) 04 TC8L 0 0 0 ** (D) 03 CTR3 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 01 CTR1 0 ** (D) 00 CTR0 0		\backslash	(F) 02 Reserved						
Expanded Reg. Bank 0/Group (0) (0) 03 P3 0 U (0) 02 P2 U * (0) 01 P1 U (0) 00 P0 U (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** His 5 Is not reset with a Stop-Mode Recovery ** (D) 04 TC8L 0 <			(F) 01 Reserved						
(0) 03 P3 0 U (0) 02 P2 U * (0) 01 P1 U (0) 00 P0 U * (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ^* (D) 05 TC8H 0	Expa	anded Reg. Bank 0/Group (0)	(F) 00 PCON	1 1 1	1	1	1	1 0	
(0) 03 P3 0			Expanded Reg. Bank D/Group 0						
(b) 02 P2 U * (0) 01 P1 U (0) 00 P0 U U = Unknown * * All addresses are in hexadecimal * ↑ Bit 5 Is not reset with a Stop-Mode Recovery ** (D) 04 ** (D) 05 ** (D) 06 ** (D) 07 ** (D) 08 ** (D) 08 ** (D) 07 ** (D) 08 ** (D) 07 ** (D) 06 ** (D) 06 ** (D) 07 ** (D) 06 ** (D) 07 ** (D) 08 ** (D) 08 ** (D) 04 ** (D) 05 ** (D) 04 ** (D) 03 ** (D) 02 ** (D) 01 ** (D) 01 ** (D) 01 ** (D) 01 ** (D) 02 ** (D) 01 (D) 0	(0) 03 P3	U U		UUI	υ	U	U	υn	
* (0) 01 P1 U (0) 01 P1 U (0) 00 P0 U * (D) 00 A LO8 0<	(0) 02 P2	U	* (D) 0B HI8	0 0 0	0	0	0	0 0	
(b) 01 1 1 0	* (0) 01 P1	U	* (D) 0A 08	0 0 0	0	0	0	0 0	
(0) 00 P0 U U = Unknown (D) 08 LO16 0	(0) 011 1	<u> </u>	* (D) 09 HI16	0 0 0	0	0	0	0 0	
U = Unknown * (D) 07 TC16H 0 <td>(0) 00 P0</td> <td>U</td> <td>* (D) 08 LO16</td> <td>0 0 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td>	(0) 00 P0	U	* (D) 08 LO16	0 0 0	0	0	0	0 0	
* Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ^* All addresses are in hexadecimal ^* Is not reset with a Stop-Mode Recovery, except Bit 0 ^* Bit 5 Is not reset with a Stop-Mode Recovery ^* Bit 5 Is not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Diss 5,4,3,2 not reset with a Stop-Mode Recovery ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery ^* CD 00 CTR1 0 0 ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery ^* CD 00 CTR0 ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery			* (D) 07 TC16H	0 0 0	0	0	0	0 0	
*** All addresses are in hexadecimal * (D) 05 TC8H 0 <t< td=""><td>* Is not reset with a Ston-Mor</td><td>de Recoverv</td><td>* (D) 06 TC16L</td><td>0 0 0</td><td>0</td><td>0</td><td>0</td><td>0 0</td></t<>	* Is not reset with a Ston-Mor	de Recoverv	* (D) 06 TC16L	0 0 0	0	0	0	0 0	
⁺ Is not reset with a Stop-Mode Recovery, except Bit 0 ⁺ 1bit 5 Is not reset with a Stop-Mode Recovery ⁺ (D) 04 TC8L ⁻ 0 0 0 0 0 0 0 0 0 0 0 ⁺ (D) 03 CTR3 ⁻ 0 0 0 0 1 1 1 1 1 ⁺ 1 ⁺ (D) 02 CTR2 ⁻ 0 0 0 0 0 0 0 0 0 ⁻ 1 1 1 1 ⁺	** All addresses are in beyade	ecimal	* (D) 05 TC8H	0 0 0	0	0	0	0 0	
	↑ Is not reset with a Stop-Mo	de Recovery, except Bit 0	* (D) 04 TC8L	0 0 0	0	0	0	0 0	
[↑] ↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery [↑] ↑↑↑ [↑] ↑↑↑ [↑] ↑↑↑ [↑] ↑↑↑↑ [↑] ↑↑↑ [↑] ↑↑ [↑] ↑ [↑]	↑↑ Bit 5 Is not reset with a Sto	p-Mode Recovery	1↑ (D) 03 CTR3	0 0 0	1	1	1	1 1	
^{↑↑↑↑} Bits 5 and 4 not reset with a Stop-Mode Recovery ^{↑↑↑↑↑} (D) 01 CTR1 (D) 01 CTR1 (D) 0 0 0 0 0 0 0 0 (D) 01 CTR1 (D) 00 CTR0 (D)	↑↑↑ Bits 5,4,3.2 not reset with	a Stop-Mode Recoverv	↑↑↑ (D) 02 CTR2	0 0 0	0	0	0	0 0	
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery ↑↑↑↑↑↓ (D) 00 CTR0 0 0 0 0 0 0 0 0 0 0	↑↑↑↑ Bits 5 and 4 not reset with	a Stop-Mode Recovery	↑↑↑↑ (D) 01 CTR1	0 0 0	0	0	0	0 0	
	↑↑↑↑↑ Bits 5,4,3,2,1 not reset wit	th a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	0 0 0	0	0	0	0 0	

Figure 15. Expanded Register File Architecture







Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



Table 18. CTR3 (D)03H: T8/T16 Control Register (Continued)

Field	Bit Position		Value	Description
Reserved	43210	R	1	Always reads 11111
		W	x	No Effect

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5– D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).



Figure 18. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.



Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.







Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put



T16 Transmit Mode

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.



Figure 25. 16-Bit Counter/Timer Circuits

Note: Global interrupts override this function as described in "Interrupts" on page 50.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.



Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal or ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.



f = 8mHz

Figure 31. Oscillator Configuration



Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XORgate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/ TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address OBH.



SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

* * Default setting after Reset and Stop Mode Recovery

* * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.







Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 22).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 21 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Reserved	7		0	Reserved (Must be 0)
Recovery Level	-6	W	0 [†]	Low
-			1	High
Reserved	5		0	Reserved (Must be 0)
Source	432	W	000†	A. POR Only
			001	B. NAND of P23–P20
			010	C. NAND of P27–P20
			011	D. NOR of P33–P31
			100	E. NAND of P33–P31
			101	F. NOR of P33–P31, P00, P07
			110	G. NAND of P33–P31, P00, P07
			111	H. NAND of P33–P31, P22–P20
Reserved	10		00	Reserved (Must be 0)

Table 21.SMR2(F)0DH:Stop	Mode Recovery	Register	2*
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Notes:

* Port pins configured as outputs are ignored as a SMR recovery source. † Indicates the value upon Power-On Reset



WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

Table 24. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO}. A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM}, the RAM content is preserved. When the power level is returned to above V_{BO}, the device performs a POR and functions normally.



CTR2(0D)02H



Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)

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