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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323hes2032g">https://www.e-xfl.com/product-detail/zilog/zgp323hes2032g</a>



- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

## General Description

The ZGP323H is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The ZGP323H architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

► **Note:** All signals with an overline, " $\overline{\phantom{x}}$ ", are active Low. For example,  $\overline{B/W}$ , in which WORD is active Low, and  $\overline{B/W}$ , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 3.

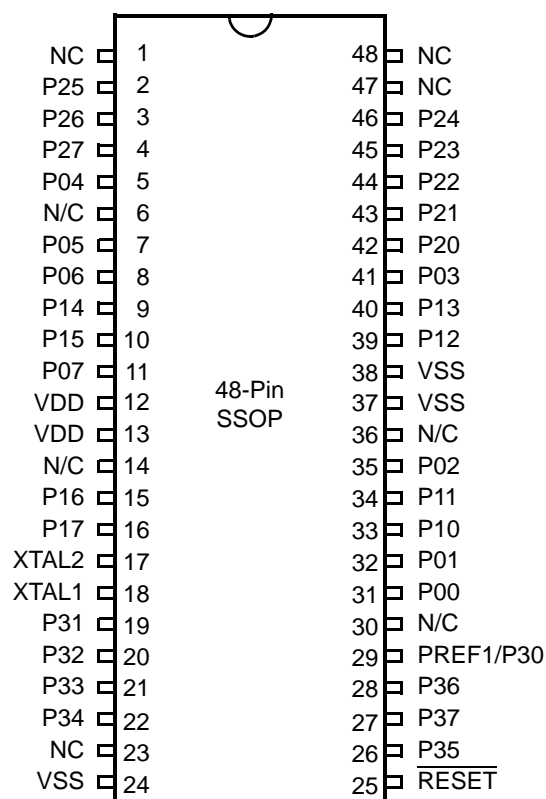


Figure 6. 48-Pin SSOP Pin Configuration

Table 6. 40- and 48-Pin Configuration

40-Pin PDIP #	48-Pin SSOP #	Symbol
26	31	P00
27	32	P01
30	35	P02
34	41	P03
5	5	P04
6	7	P05
7	8	P06
10	11	P07
28	33	P10
29	34	P11
32	39	P12

**Table 11. GP323HA DC Characteristics**

<b>T<sub>A</sub> = -40°C to +125°C</b>								
<b>Symbol</b>	<b>Parameter</b>	<b>V<sub>CC</sub></b>	<b>Min</b>	<b>Typ(7)</b>	<b>Max</b>	<b>Units</b>	<b>Conditions</b>	<b>Notes</b>
V <sub>CC</sub>	Supply Voltage		2.0		5.5	V	See Note 5	5
V <sub>CH</sub>	Clock Input High Voltage	2.0-5.5	0.8 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.4	V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	2.0-5.5	0.7 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V		
V <sub>IL</sub>	Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.2 V <sub>CC</sub>	V		
V <sub>OH1</sub>	Output High Voltage	2.0-5.5	V <sub>CC</sub> -0.4			V	I <sub>OH</sub> = -0.5mA	
V <sub>OH2</sub>	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V <sub>CC</sub> -0.8			V	I <sub>OH</sub> = -7mA	
V <sub>OL1</sub>	Output Low Voltage	2.0-5.5			0.4	V	I <sub>OL</sub> = 4.0mA	
V <sub>OL2</sub>	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I <sub>OL</sub> = 10mA	
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V <sub>REF</sub>	Comparator Reference Voltage	2.0-5.5	0		V <sub>DD</sub> -1.75	V		
I <sub>IL</sub>	Input Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub> Pull-ups disabled	
R <sub>PU</sub>	Pull-up Resistance	2.0V	200		700	KΩ	V <sub>IN</sub> = 0V; Pullups selected by mask option	
		3.6V	50		300	KΩ		
		5.0V	25		175	KΩ		
I <sub>OL</sub>	Output Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>CC</sub>	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I <sub>CC1</sub>	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
I <sub>CC2</sub>	Standby Current (Stop Mode)	2.0V		1.6	15	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		3.6V		1.8	20	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		5.5V		1.9	25	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		2.0V		5	30	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		3.6V		8	40	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		5.5V		15	60	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
I <sub>LV</sub>	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage Detection			2.4		V		



AC Characteristics

Figure 8 and Table 13 describe the Alternating Current (AC) characteristics.

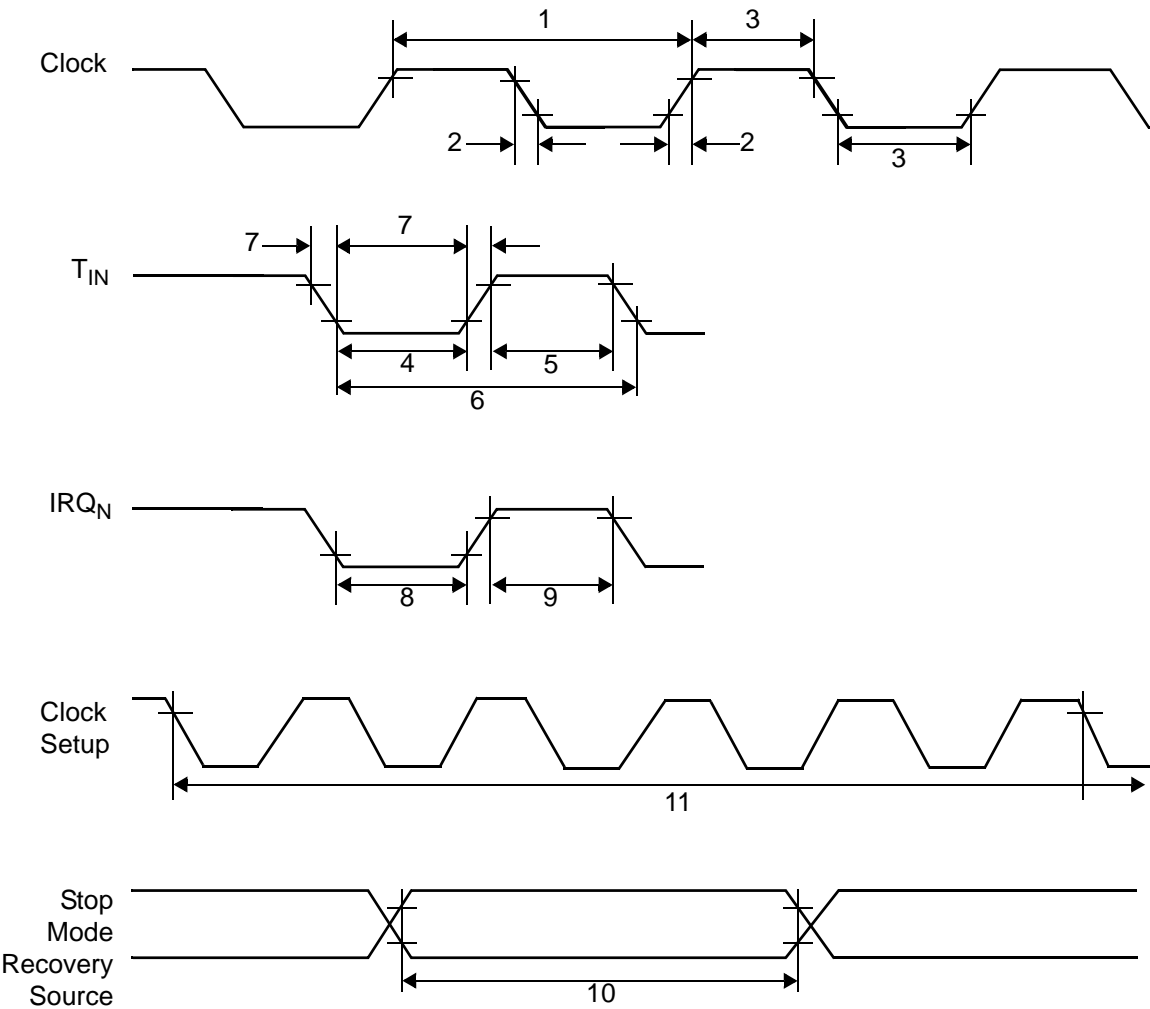
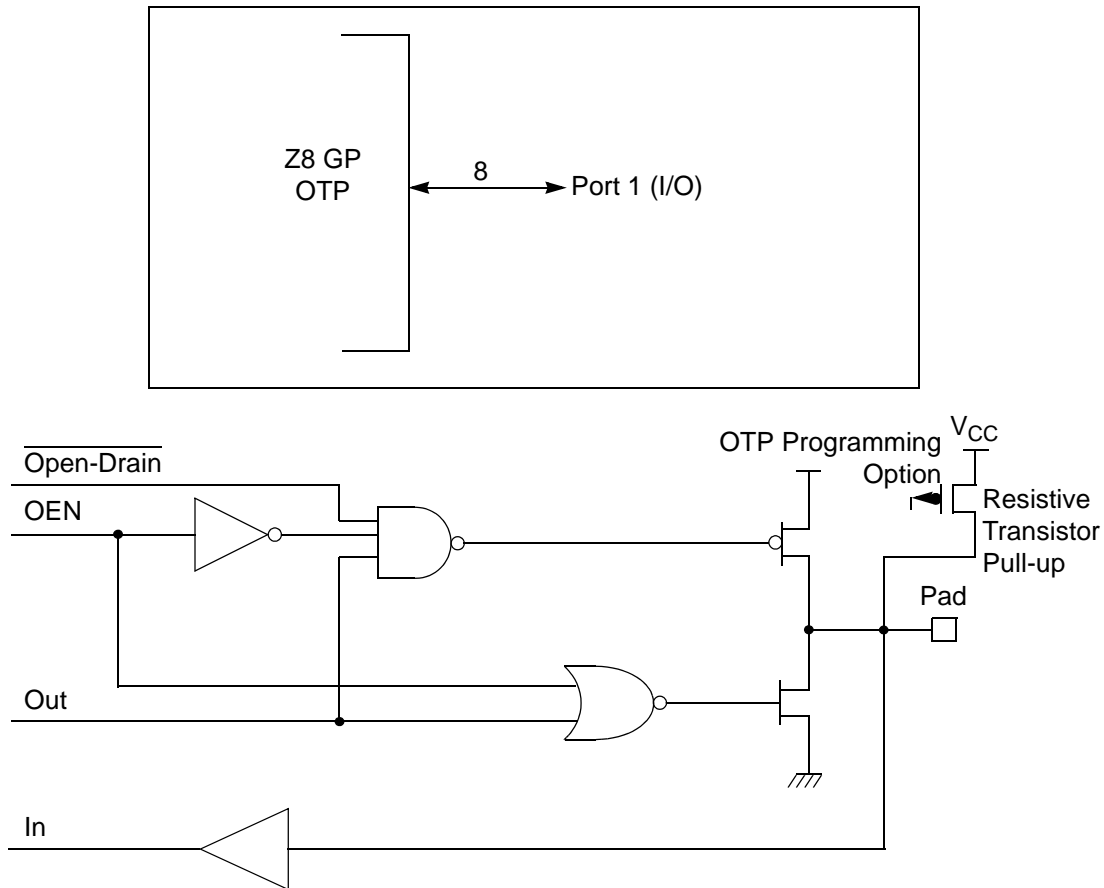


Figure 8. AC Timing Diagram



**Figure 10. Port 1 Configuration**

## Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.





### **T8/T16\_Logic/Edge \_Detect**

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

### **Transmit\_Submode/Glitch Filter**

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

### **Initial\_T8\_Out/Rising\_Edge**

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

### **Initial\_T16 Out/Falling \_Edge**

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

► **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/T16\_OUT.

### **CTR2 Counter/Timer 16 Control Register—CTR2(D)02H**

Table 17 lists and briefly describes the fields for this register.





**Table 17. CTR2(D)02H: Counter/Timer16 Control Register**

Field	Bit Position		Value	Description
T16_Enable	7-----	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Transmit Mode
			1	Modulo-N
			0	Single Pass
			1	Demodulation Mode
Time_Out	--5-----	R	0*	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
		W	0	No Counter Timeout
			1	Counter Timeout Occurred
T16_Clock	---43---	R/W	00**	No Effect
			01	Reset Flag to 0
			10	SCLK
			11	SCLK/2
Capture_INT_Mask	-----2--	R/W	0**	SCLK/4
			1	SCLK/8
Counter_INT_Mask	-----1-	R/W	0*	Disable Data Capture Int.
			1	Enable Data Capture Int.
P35_Out	-----0	R/W	0*	Disable Timeout Int.
			1	Enable Timeout Int.

**Note:**

\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

**T16\_Enable**

This field enables T16 when set to 1.

**Single/Modulo-N**

In TRANSMIT Mode, when set to 0, the counter reloads the initial value when it reaches the terminal count. When set to 1, the counter stops when the terminal count is reached.

**Table 18. CTR3 (D)03H: T8/T16 Control Register (Continued)**

Field	Bit Position		Value	Description
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

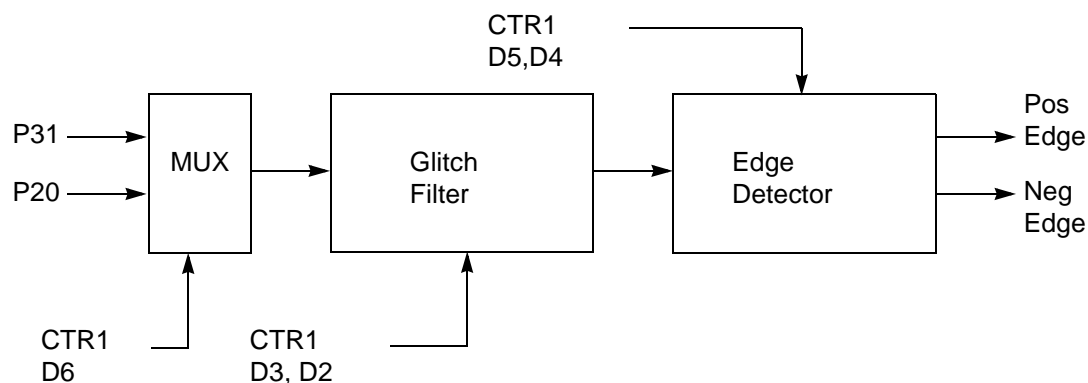
\*Indicates the value upon Power-On Reset.

\*\*Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

## Counter/Timer Functional Blocks

### Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).



**Figure 18. Glitch Filter Circuitry**

### T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8\_OUT is 1; if it is 1, T8\_OUT is 0. See Figure 19.

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).

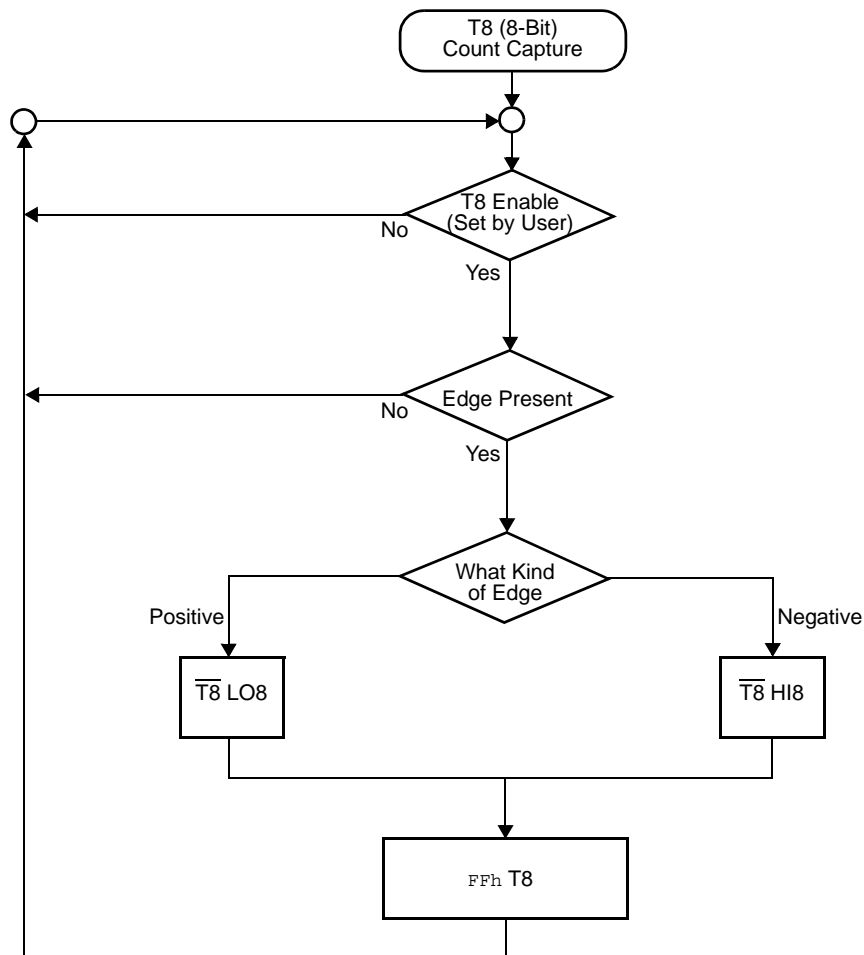
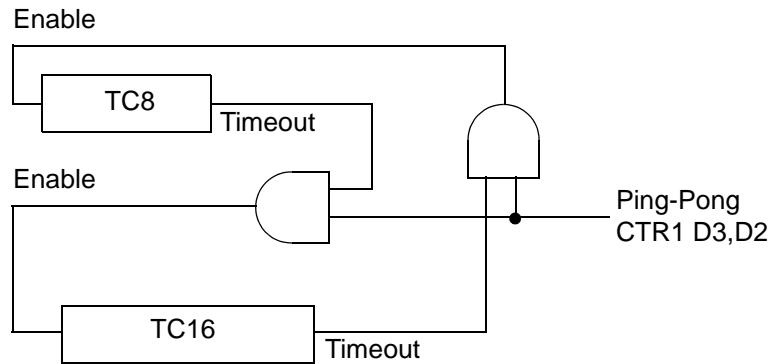


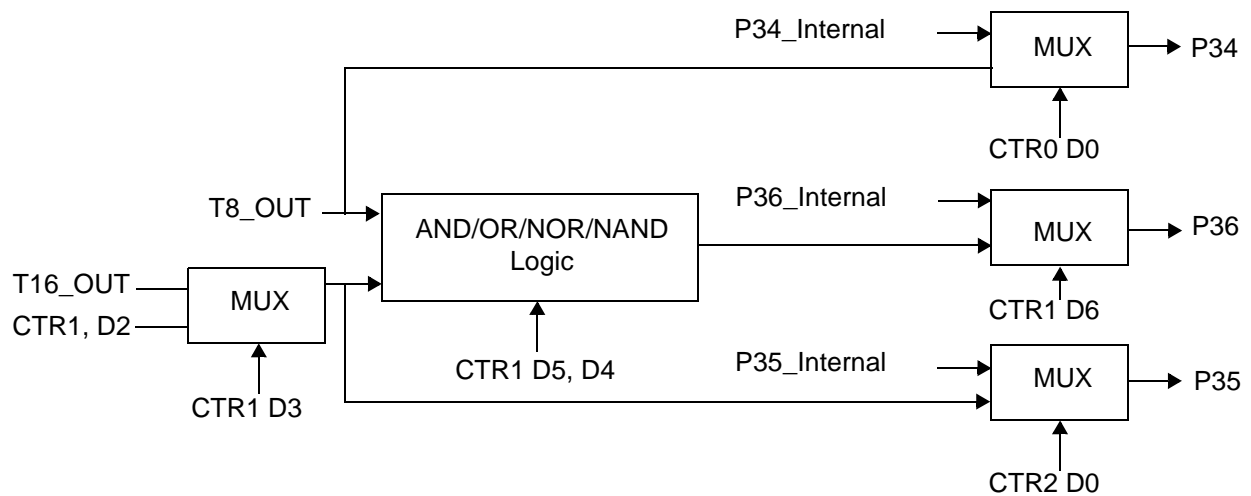
Figure 23. Demodulation Mode Count Capture Flowchart



**Figure 28. Ping-Pong Mode Diagram**

### Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.

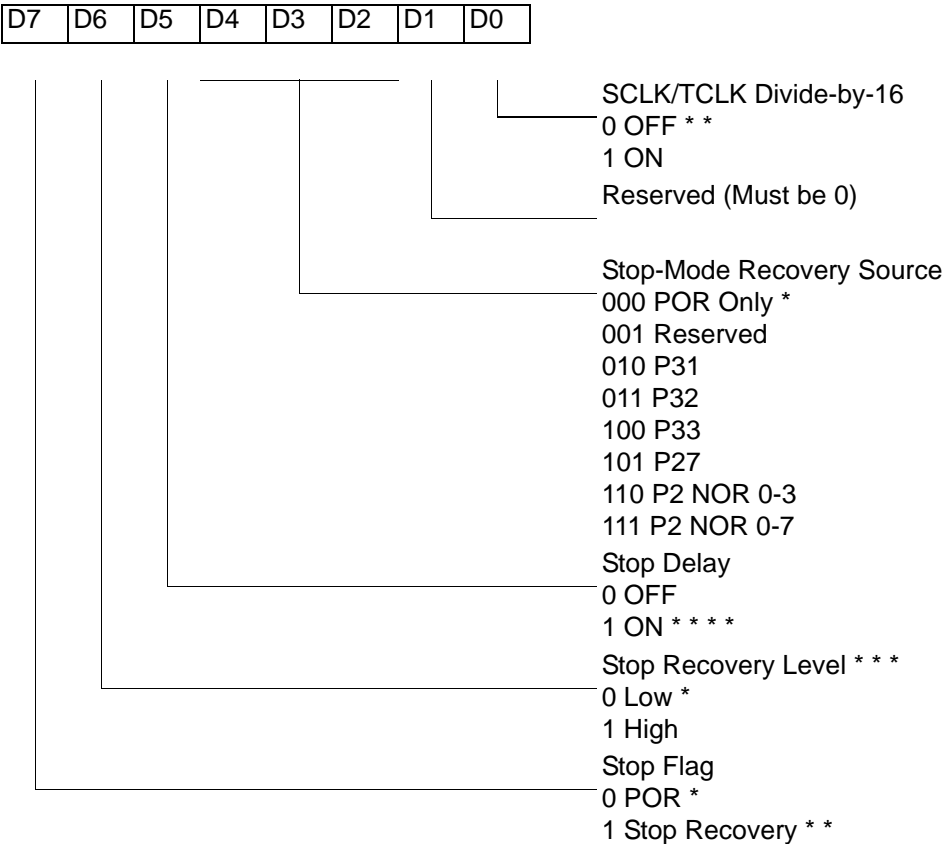


**Figure 29. Output Circuit**

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.



SMR(0F)0BH



\* Default after Power On Reset or Watch-Dog Reset  
\* \* Default setting after Reset and Stop Mode Recovery  
\* \* \* At the XOR gate input  
\* \* \* \* Default setting after reset. Must be 1 if using a crystal or resonator clock source.

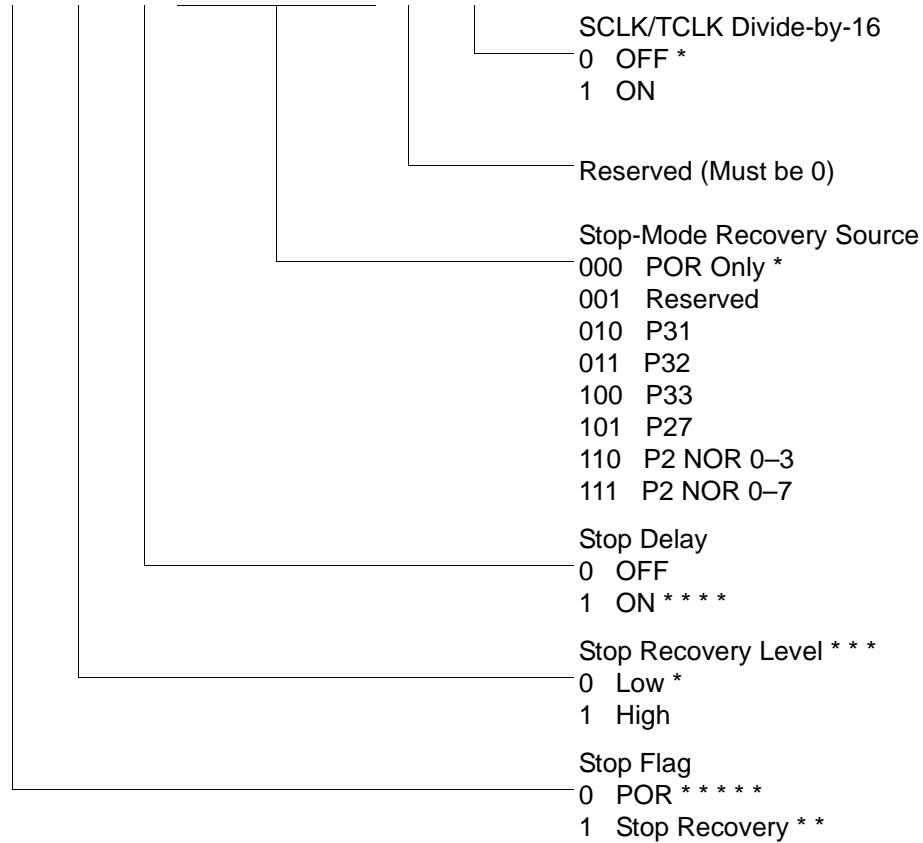
Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after reset

\* \* Set after Stop Mode Recovery

\* \* \* At the XOR gate input

\* \* \* \* Default setting after reset. Must be 1 if using a crystal or resonator clock source.

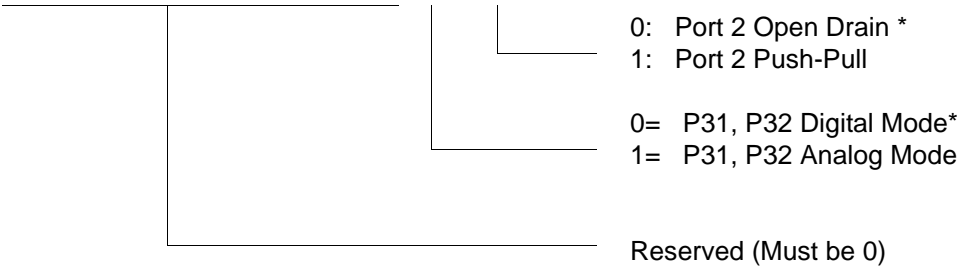
\* \* \* \* \* Default setting after Power On Reset. Not reset with a Stop Mode recovery.

**Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)**



R247 P3M(F7H)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)

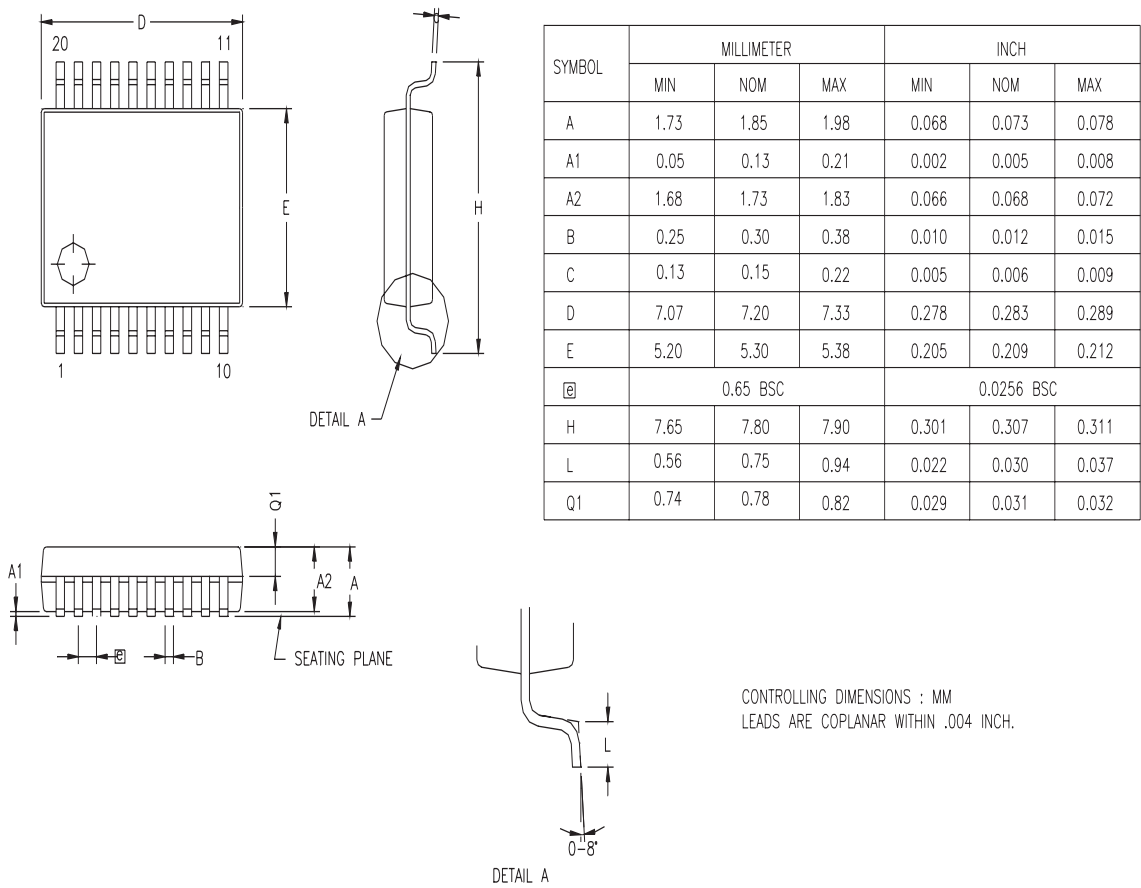


Figure 61. 20-Pin SSOP Package Diagram





## Ordering Information

### 32KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4832C	48-pin SSOP 32K OTP	ZGP323HSS2832C	28-pin SOIC 32K OTP
ZGP323HSP4032C	40-pin PDIP 32K OTP	ZGP323HSH2032C	20-pin SSOP 32K OTP
ZGP323HSK2832E	28-pin CDIP 32K OTP	ZGP323HSK2032E	20-pin CDIP 32K OTP
ZGP323HSK4032E	40-pin CDIP 32K OTP	ZGP323HSP2032C	20-pin PDIP 32K OTP
ZGP323HSH2832C	28-pin SSOP 32K OTP	ZGP323HSS2032C	20-pin SOIC 32K OTP
ZGP323HSP2832C	28-pin PDIP 32K OTP		

### 32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4832C	48-pin SSOP 32K OTP	ZGP323HES2832C	28-pin SOIC 32K OTP
ZGP323HEP4032C	40-pin PDIP 32K OTP	ZGP323HEH2032C	20-pin SSOP 32K OTP
ZGP323HEH2832C	28-pin SSOP 32K OTP	ZGP323HEP2032C	20-pin PDIP 32K OTP
ZGP323HEP2832C	28-pin PDIP 32K OTP	ZGP323HES2032C	20-pin SOIC 32K OTP

### 32KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323HAH4832C	48-pin SSOP 32K OTP	ZGP323HAS2832C	28-pin SOIC 32K OTP
ZGP323HAP4032C	40-pin PDIP 32K OTP	ZGP323HAH2032C	20-pin SSOP 32K OTP
ZGP323HAH2832C	28-pin SSOP 32K OTP	ZGP323HAP2032C	20-pin PDIP 32K OTP
ZGP323HAP2832C	28-pin PDIP 32K OTP	ZGP323HAS2032C	20-pin SOIC 32K OTP

Replace C with G for Lead-Free Packaging



**16KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323HSH4816C	48-pin SSOP 16K OTP	ZGP323HSS2816C	28-pin SOIC 16K OTP
ZGP323HSP4016C	40-pin PDIP 16K OTP	ZGP323HSH2016C	20-pin SSOP 16K OTP
ZGP323HSH2816C	28-pin SSOP 16K OTP	ZGP323HSP2016C	20-pin PDIP 16K OTP
ZGP323HSP2816C	28-pin PDIP 16K OTP	ZGP323HSS2016C	20-pin SOIC 16K OTP

**16KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323HEH4816C	48-pin SSOP 16K OTP	ZGP323HES2816C	28-pin SOIC 16K OTP
ZGP323HEP4016C	40-pin PDIP 16K OTP	ZGP323HEH2016C	20-pin SSOP 16K OTP
ZGP323HEH2816C	28-pin SSOP 16K OTP	ZGP323HEP2016C	20-pin PDIP 16K OTP
ZGP323HEP2816C	28-pin PDIP 16K OTP	ZGP323HES2016C	20-pin SOIC 16K OTP

**16KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323HAH4816C	48-pin SSOP 16K OTP	ZGP323HAS2816C	28-pin SOIC 16K OTP
ZGP323HAP4016C	40-pin PDIP 16K OTP	ZGP323HAH2016C	20-pin SSOP 16K OTP
ZGP323HAH2816C	28-pin SSOP 16K OTP	ZGP323HAP2016C	20-pin PDIP 16K OTP
ZGP323HAP2816C	28-pin PDIP 16K OTP	ZGP323HAS2016C	20-pin SOIC 16K OTP

Replace C with G for Lead-Free Packaging



**4KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323HSH4804C	48-pin SSOP 4K OTP	ZGP323HSS2804C	28-pin SOIC 4K OTP
ZGP323HSP4004C	40-pin PDIP 4K OTP	ZGP323HSH2004C	20-pin SSOP 4K OTP
ZGP323HSH2804C	28-pin SSOP 4K OTP	ZGP323HSP2004C	20-pin PDIP 4K OTP
ZGP323HSP2804C	28-pin PDIP 4K OTP	ZGP323HSS2004C	20-pin SOIC 4K OTP

**4KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323HEH4804C	48-pin SSOP 4K OTP	ZGP323HES2804C	28-pin SOIC 4K OTP
ZGP323HEP4004C	40-pin PDIP 4K OTP	ZGP323HEH2004C	20-pin SSOP 4K OTP
ZGP323HEH2804C	28-pin SSOP 4K OTP	ZGP323HEP2004C	20-pin PDIP 4K OTP
ZGP323HEP2804C	28-pin PDIP 4K OTP	ZGP323HES2004C	20-pin SOIC 4K OTP

**4KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323HAH4804C	48-pin SSOP 4K OTP	ZGP323HAS2804C	28-pin SOIC 4K OTP
ZGP323HAP4004C	40-pin PDIP 4K OTP	ZGP323HAH2004C	20-pin SSOP 4K OTP
ZGP323HAH2804C	28-pin SSOP 4K OTP	ZGP323HAP2004C	20-pin PDIP 4K OTP
ZGP323HAP2804C	28-pin PDIP 4K OTP	ZGP323HAS2004C	20-pin SOIC 4K OTP

Replace C with G for Lead-Free Packaging

**Additional Components**

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM (For 3.6V Emulation only)	Emulator/programmer	ZGP32300100ZPR (Ethernet)	Programming system
		ZGP32300200ZPR (USB)	Programming system

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