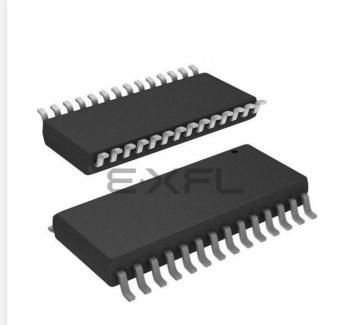
#### Zilog - ZGP323HES2804G Datasheet





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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	28
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hes2804g

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

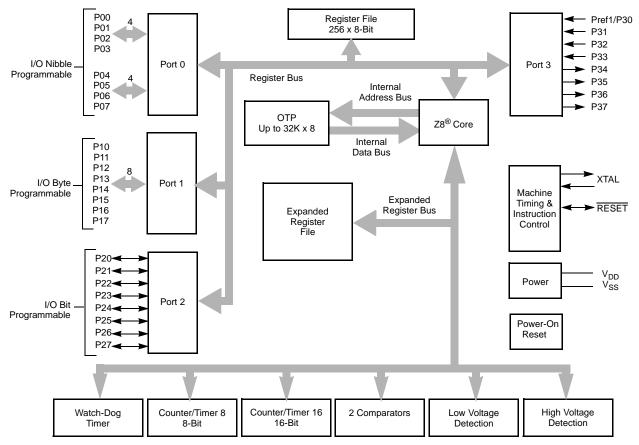


<b>-</b> : 00		04	~
Figure 68.	48-Pin SSOP Package Design		J



#### Table 3. Power Connections

Connection	Circuit	Device	
Power	V <sub>CC</sub>	V <sub>DD</sub>	
Ground	GND	V <sub>SS</sub>	



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram





Figure 2. Counter/Timers Diagram

## **Pin Description**

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.





P25 P26 P27 P04 P05 P07 V <sub>DD</sub> XTAL2 XTAL1 P31 P32 P34	1 2 3 4 5 6 7 8 9 10 11 12 13 14	28-Pin PDIP SOIC SSOP CDIP*	28 27 26 25 24 23 22 21 20 19 18 17 16	<ul> <li>P24</li> <li>P23</li> <li>P22</li> <li>P21</li> <li>P20</li> <li>P03</li> <li>V<sub>SS</sub></li> <li>P02</li> <li>P01</li> <li>P00</li> <li>Pref1/P30</li> <li>P36</li> <li>P35</li> </ul>
P34 🗖	14		15	🖵 P35

## Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

#### Table 5. 28-Pin PDIP/SOIC/SSOP/CDIP\* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V <sub>DD</sub>		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30	Input	Analog ref input; connect to V <sub>CC</sub> if not used
	Port 3 Bit 0		Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V <sub>SS</sub>		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4



#### Table 11. GP323HA DC Characteristics (Continued)

			T <sub>A</sub> = -40°	C to +125	°C			
Symbol	Parameter	V <sub>CC</sub>	Min	Typ(7)	Max	Units	Conditions	Notes
V <sub>HVD</sub>	Vcc High Voltage Detection			2.7		V		
Notes:								
1. All o	outputs unloaded, inpu	ıts at rail.						
2. CL1	1 = CL2 = 100 pF.							
3. Osc	cillator stopped.							
4. Osc	cillator stops when V <sub>CC</sub>	falls below	V <sub>BO</sub> limit.					
volt	age fluctuations are a	nticipated, su	ch as thos	e resulting			cally close to VCC and nfrared LED.	$V_{SS}$ pins if operating
6. Cor	mparator and Timers a	re on. Interru	pt disabled	1.				

7. Typical values shown are at 25 degrees C.

#### Table 12. EPROM/OTP Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes
	Erase Time	15			Minutes	1,3
	Data Retention @ use years		10		Years	2
	Program/Erase Endurance	100			Cycles	1

Notes:

1. For windowed cerdip package only.

2. Standard: 0°C to 70°C; Extended: -40°C to +105°C; Automotive: -40°C to +125°C. Determined using the Arrhenius model, which is an industry standard for estimating data retention of floating gate technologies:

AF = exp[(Ea/k)\*(1/Tuse - 1/TStress)] Where: Ea is the intrinsic activation energy (eV; typ. 0.8) k is Boltzman's constant (8.67 x 10-5 eV/°K) °K = -273.16°C Tuse = Use Temperature in °K TStress = Stress Temperature in °K 3. At a stable UV Lamp output of 20mW/CM<sup>2</sup>



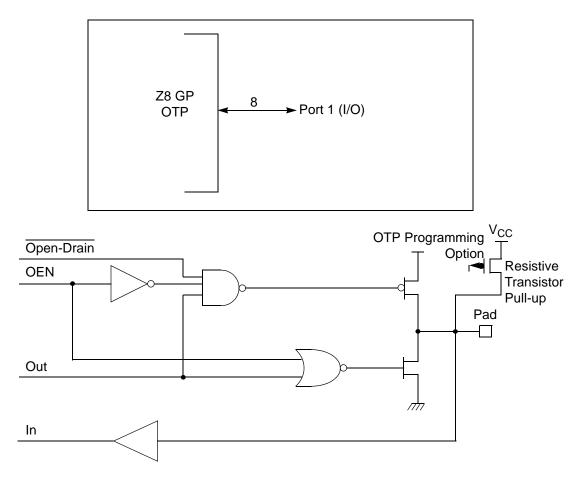


Figure 10. Port 1 Configuration

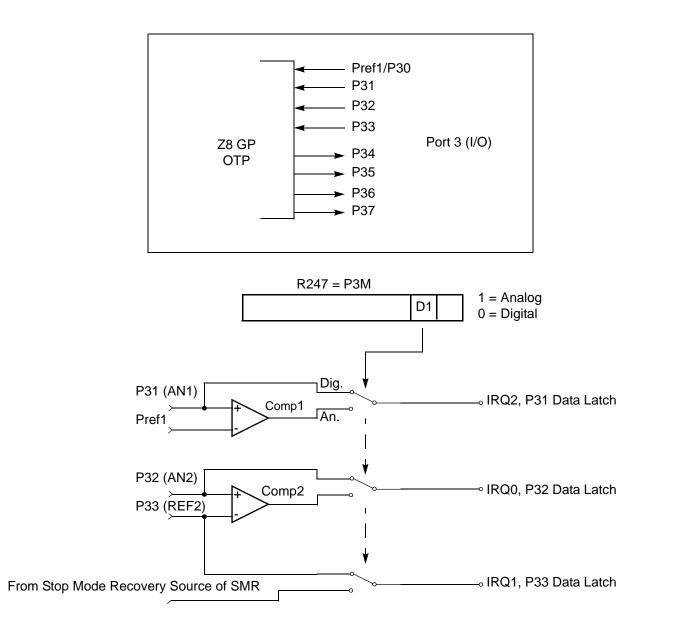
## Port 2 (P27-P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 11). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. The POR resets with the eight bits of Port 2 configured as inputs.

Port 2 also has an 8-bit input OR and AND gate, which can be used to wake up the part. P20 can be programmed to access the edge-detection circuitry in demodulation mode.







#### Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—



CTR1(0D)01H" on page 35). Other edge detect and IRQ modes are described in Table 14.

**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	Т8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

#### Table 14. Port 3 Pin Function Summary

>

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.



## Timers

## T8\_Capture\_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

#### T8\_Capture\_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position		Description	
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect	

#### T16\_Capture\_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

#### T16\_Capture\_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

#### Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position	Description	
T16_Data_HI	[7:0]	R/W	Data



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## Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position		Description
T16_Data_LO	[7:0]	R/W	Data

## Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position		Description
T8_Level_HI	[7:0]	R/W	Data

## Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

## CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

Field	<b>Bit Position</b>		Value	Description
T8_Enable	7	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	5	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	43	R/W	0 0**	SCLK
			0 1	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Interrupt
-			1	Enable Data Capture Interrupt



Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.



**Caution:** Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.





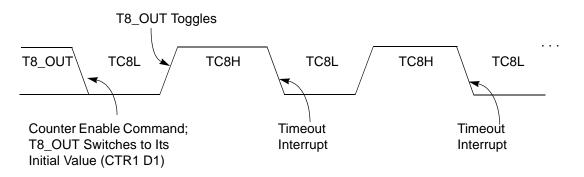


Figure 22. T8\_OUT in Modulo-N Mode

## **T8 Demodulation Mode**

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

ZGP323H Product Specification



Caution: Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFFH. Transition from 0 to FFFFH is not a timeout condition.







Figure 27. T16\_OUT in Modulo-N Mode

## **T16 DEMODULATION Mode**

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

## If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).



FF	NOP	; clear the pipeline
6F	Stop	; enter Stop Mode
or		
FF	NOP	; clear the pipeline
7F	HALT	; enter HALT Mode

## **Port Configuration Register**

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

#### PCON(FH)00H



\* Default setting after reset

#### Figure 32. Port Configuration Register (PCON) (Write Only)

#### Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

#### Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.



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#### CTR2(0D)02H

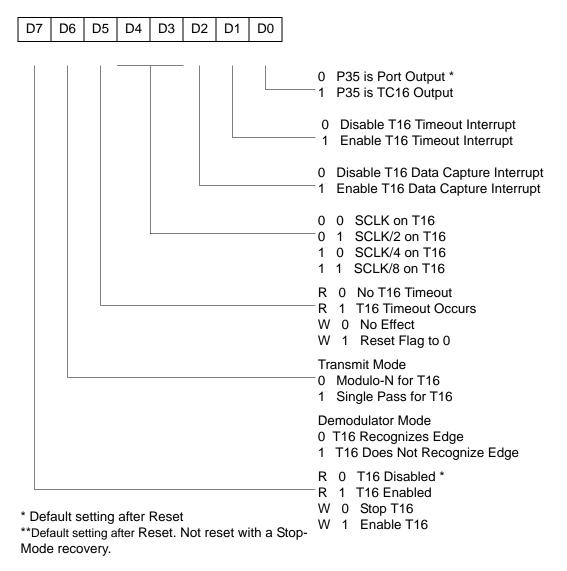


Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)





## CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0	
								Reserved No effect when written Always reads 11111 Sync Mode 0* Disable Sync Mode** 1 Enable Sync Mode T <sub>8</sub> Enable R 0* T <sub>8</sub> Disabled R 1 T <sub>8</sub> Enabled W0 Stop T <sub>8</sub>
								W1 Enable $T_8$ $T_{16}$ Enable $R 0^* T_{16}$ Disabled $R 1 T_{16}$ Enabled $W 0$ Stop $T_{16}$ $W 1$ Enable $T_{16}$

\* Default setting after reset. \*\* Default setting after reset. Not reset with a Stop Mode recovery.

## Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)



## R249 IPR(F9H)

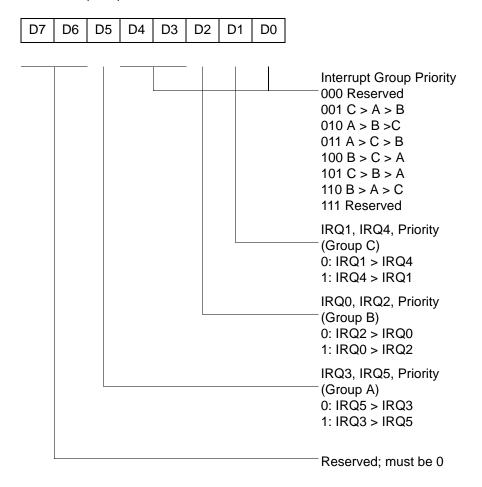


Figure 51. Interrupt Priority Register (F9H: Write Only)



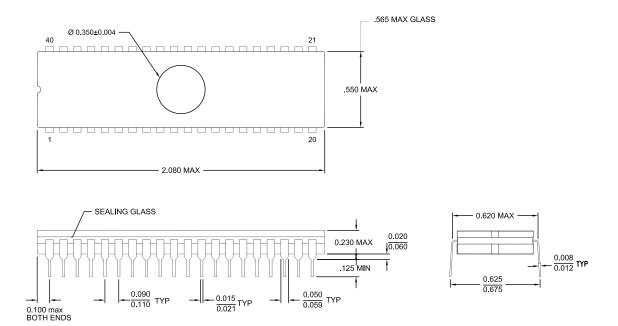


Figure 67. 40-Pin CDIP Package Diagram



## Example



#### ZGP323H Z8<sup>®</sup> OTP Microcontroller with IR Timers



pin 4 Ε **EPROM** selectable options 64 expanded register file 26 expanded register file architecture 28 expanded register file control registers 71 flag 80 interrupt mask register 79 interrupt priority register 78 interrupt request register 79 port 0 and 1 mode register 77 port 2 configuration register 75 port 3 mode register 76 port configuration register 75 register pointer 80 stack pointer high register 81 stack pointer low register 81 stop-mode recovery register 73 stop-mode recovery register 2 74 T16 control register 69 T8 and T16 common control functions register 67 T8/T16 control register 70 TC8 control register 66 watch-dog timer register 75 F features standby modes 1 functional description counter/timer functional blocks 40 CTR(D)01h register 35 CTR0(D)00h register 33 CTR2(D)02h register 37 CTR3(D)03h register 39 expanded register file 26 expanded register file architecture 28 HI16(D)09h register 32 HI8(D)0Bh register 32 L08(D)0Ah register 32 L0I6(D)08h register 32

program memory map 26 **RAM 25** register description 65 register file 30 register pointer 29 register pointer detail 31 SMR2(F)0D1h register 40 stack 31 TC16H(D)07h register 32 TC16L(D)06h register 33 TC8H(D)05h register 33 TC8L(D)04h register 33 G glitch filter circuitry 40 Η halt instruction, counter/timer 54 input circuit 40 interrupt block diagram, counter/timer 51 interrupt types, sources and vectors 52 L low-voltage detection register 65 Μ memory, program 25 modulo-N mode T16 OUT 47 T8 OUT 43 0 oscillator configuration 53 output circuit, counter/timer 49 Ρ package information 20-pin DIP package diagram 82 20-pin SSOP package diagram 84 28-pin DIP package diagram 86 28-pin SOIC package diagram 85 28-pin SSOP package diagram 87 40-pin DIP package diagram 87 48-pin SSOP package diagram 89 pin configuration 20-pin DIP/SOIC/SSOP 5

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T8\_Capture\_LO 32 register file 30 expanded 26 register pointer 29 detail 31 reset pin function 25 resets and WDT 63 S SCLK circuit 58 single-pass mode T16\_OUT 47 T8\_OUT 43 stack 31 standard test conditions 10 standby modes 1 stop instruction, counter/timer 54 stop mode recovery 2 register 61 source 59 stop mode recovery 2 61 stop mode recovery register 57 Т T16 transmit mode 46 T16\_Capture\_HI 32 T8 transmit mode 40 T8\_Capture\_HI 32 test conditions, standard 10 test load diagram 10 timing diagram, AC 16 transmit mode flowchart 41 V VCC 5 voltage brown-out/standby 64 detection and flags 65 voltage detection register 71 W watch-dog timer mode registerwatch-dog timer mode register 62 time select 63

X XTAL1 5 XTAL1 pin function 18 XTAL2 5 XTAL2 pin function 18