



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hsh2004c



Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1. Revision History of this Document

Date	Revision Level	Section	Description	Page #
December 2004	02		Changed low power consumption, STOP and HALT mode current values, deleted mask option note, clarified temperature ranges in Tables 6 and 8 and 10. Added new Tables 9 and 10. Also added Characterization data to Table 11 and changed Program/Erase Endurance value in Table 12.	1,2,10 11,12, 13,14, 15
			Removed Preliminary designation	All
March 2005	03		Minor change to Table 9 Electrical Characteristics. Added 20, 28 and 40-pin CDIP parts in the Ordering Section.	11,90



List of Figures

Figure 1.	Functional Block Diagram	3
Figure 2.	Counter/Timers Diagram	4
Figure 3.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	5
Figure 4.	28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	6
Figure 5.	40-Pin PDIP/CDIP* Pin Configuration	7
Figure 6.	48-Pin SSOP Pin Configuration	8
Figure 7.	Test Load Diagram	10
Figure 8.	AC Timing Diagram	16
Figure 9.	Port 0 Configuration	19
Figure 10.	Port 1 Configuration	20
Figure 11.	Port 2 Configuration	21
Figure 12.	Port 3 Configuration	22
Figure 13.	Port 3 Counter/Timer Output Configuration	24
Figure 14.	Program Memory Map (32K OTP)	26
Figure 15.	Expanded Register File Architecture	28
Figure 16.	Register Pointer	29
Figure 17.	Register Pointer—Detail	31
Figure 18.	Glitch Filter Circuitry	40
Figure 19.	Transmit Mode Flowchart	41
Figure 20.	8-Bit Counter/Timer Circuits	42
Figure 21.	T8_OUT in Single-Pass Mode	43
Figure 22.	T8_OUT in Modulo-N Mode	43
Figure 23.	Demodulation Mode Count Capture Flowchart	44
Figure 24.	Demodulation Mode Flowchart	45
Figure 25.	16-Bit Counter/Timer Circuits	46
Figure 26.	T16_OUT in Single-Pass Mode	47
Figure 27.	T16_OUT in Modulo-N Mode	47
Figure 28.	Ping-Pong Mode Diagram	49
Figure 29.	Output Circuit	49
Figure 30.	Interrupt Block Diagram	51
Figure 31.	Oscillator Configuration	53
Figure 32.	Port Configuration Register (PCON) (Write Only)	55
Figure 33.	STOP Mode Recovery Register	57



Figure 34. SCLK Circuit	58
Figure 35. Stop Mode Recovery Source	59
Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only) . .	61
Figure 37. Watch-Dog Timer Mode Register (Write Only)	62
Figure 38. Resets and WDT	63
Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted) .	66
Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write) . .	67
Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted) .	69
Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)	70
Figure 43. Voltage Detection Register	71
Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)	72
Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)	73
Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only) .	74
Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only).	75
Figure 48. Port 2 Mode Register (F6H: Write Only).	75
Figure 49. Port 3 Mode Register (F7H: Write Only)	76
Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)	77
Figure 51. Interrupt Priority Register (F9H: Write Only)	78
Figure 52. Interrupt Request Register (FAH: Read/Write)	79
Figure 53. Interrupt Mask Register (FBH: Read/Write)	79
Figure 54. Flag Register (FCH: Read/Write)	80
Figure 55. Register Pointer (FDH: Read/Write)	80
Figure 56. Stack Pointer High (FEH: Read/Write)	81
Figure 57. Stack Pointer Low (FFH: Read/Write)	81
Figure 58. 20-Pin CDIP Package	82
Figure 59. 20-Pin PDIP Package Diagram	82
Figure 60. 20-Pin SOIC Package Diagram	83
Figure 61. 20-Pin SSOP Package Diagram	84
Figure 62. 28-Pin SOIC Package Diagram	85
Figure 63. 28-Pin CDIP Package Diagram	86
Figure 64. 28-Pin PDIP Package Diagram	86
Figure 65. 28-Pin SSOP Package Diagram.	87
Figure 66. 40-Pin PDIP Package Diagram	87
Figure 67. 40-Pin CDIP Package Diagram	88

Absolute Maximum Ratings

Stresses greater than those listed in Table 8 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	125	° C	1
Storage temperature	-65	+150	° C	
Voltage on any pin with respect to V_{SS}	-0.3	7.0	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	7.0	V	
Maximum current on input and/or inactive output pin	-5	+5	μ A	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	

Notes:

1. See Ordering Information.
2. This voltage applies to all pins except the following: V_{DD} , P32, P33 and RESET.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).

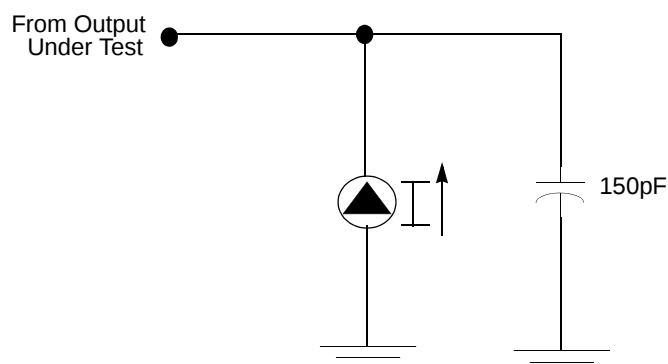


Figure 7. Test Load Diagram

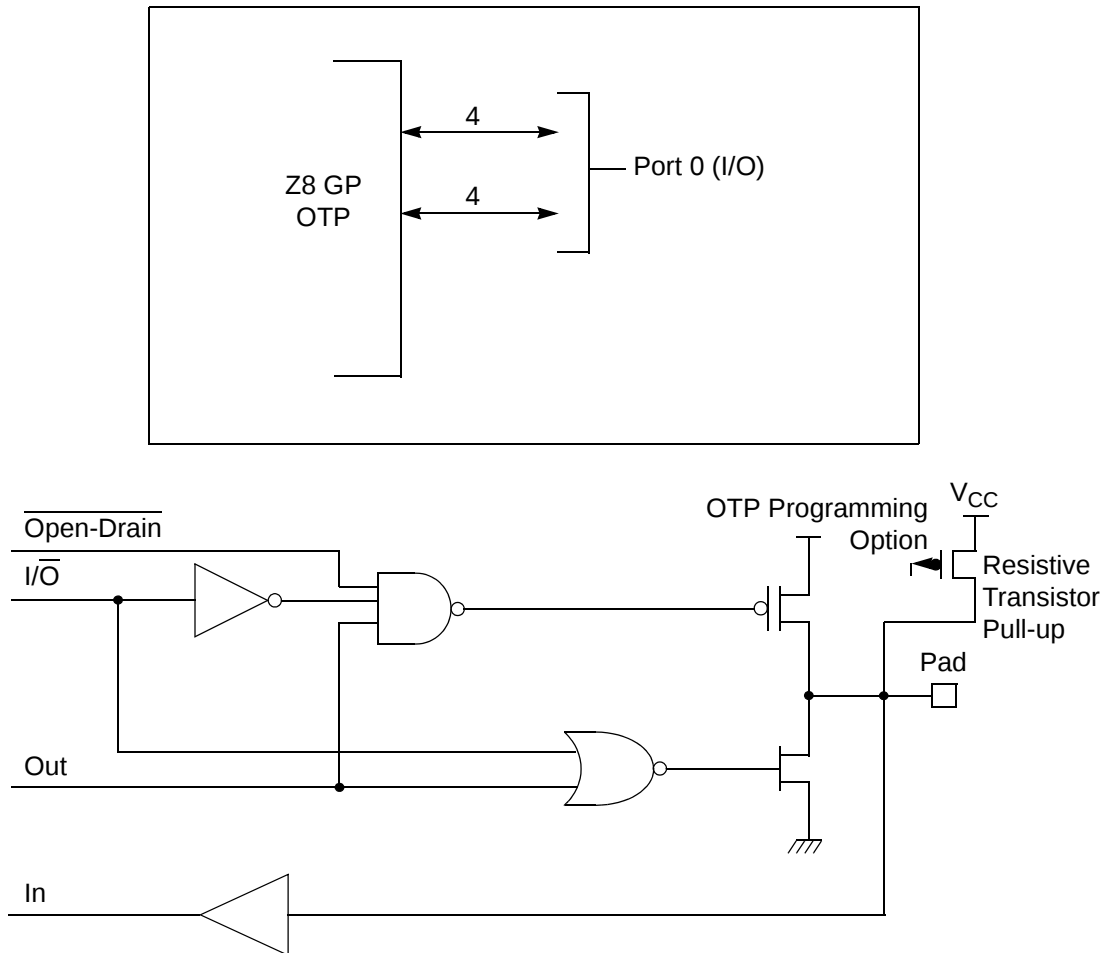


Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Note:** The Port 1 direction is reset to its default state following an SMR.

Table 18. CTR3 (D)03H: T8/T16 Control Register (Continued)

Field	Bit Position		Value	Description
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).

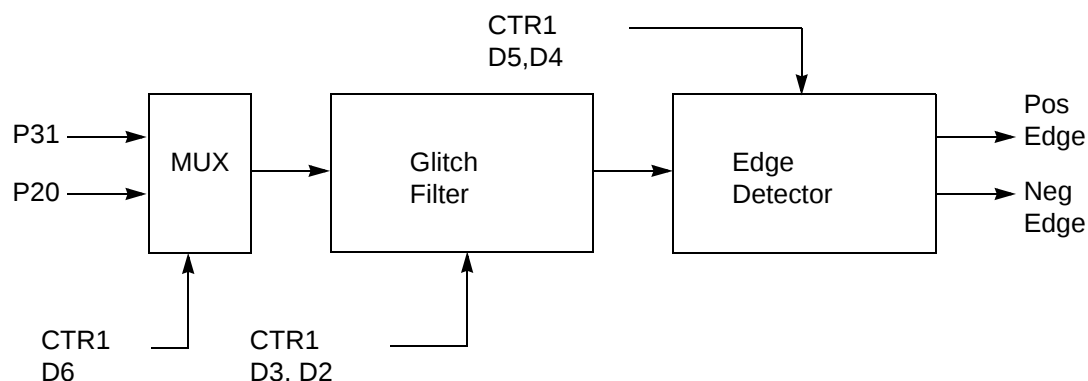


Figure 18. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.

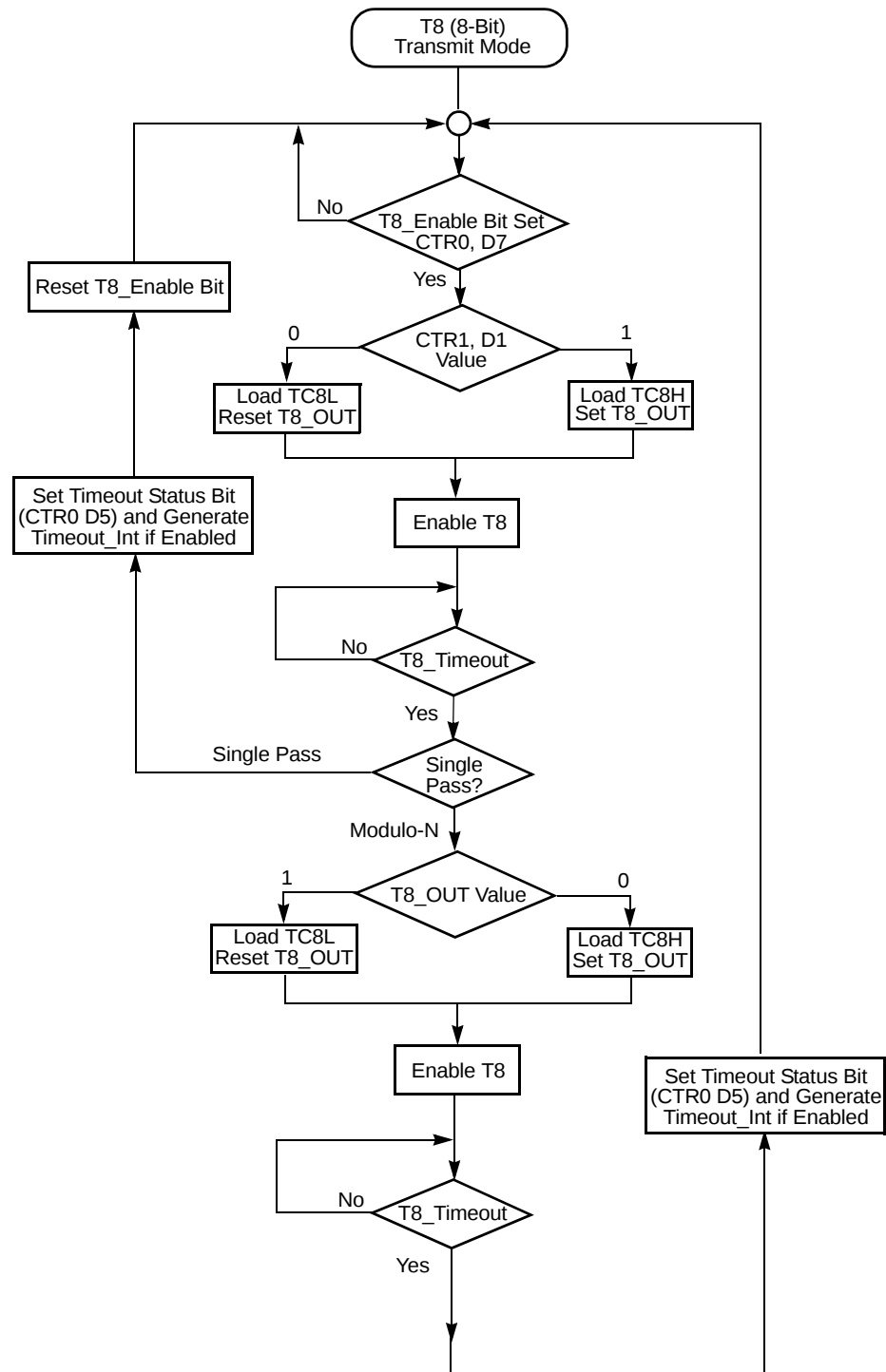


Figure 19. Transmit Mode Flowchart

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.

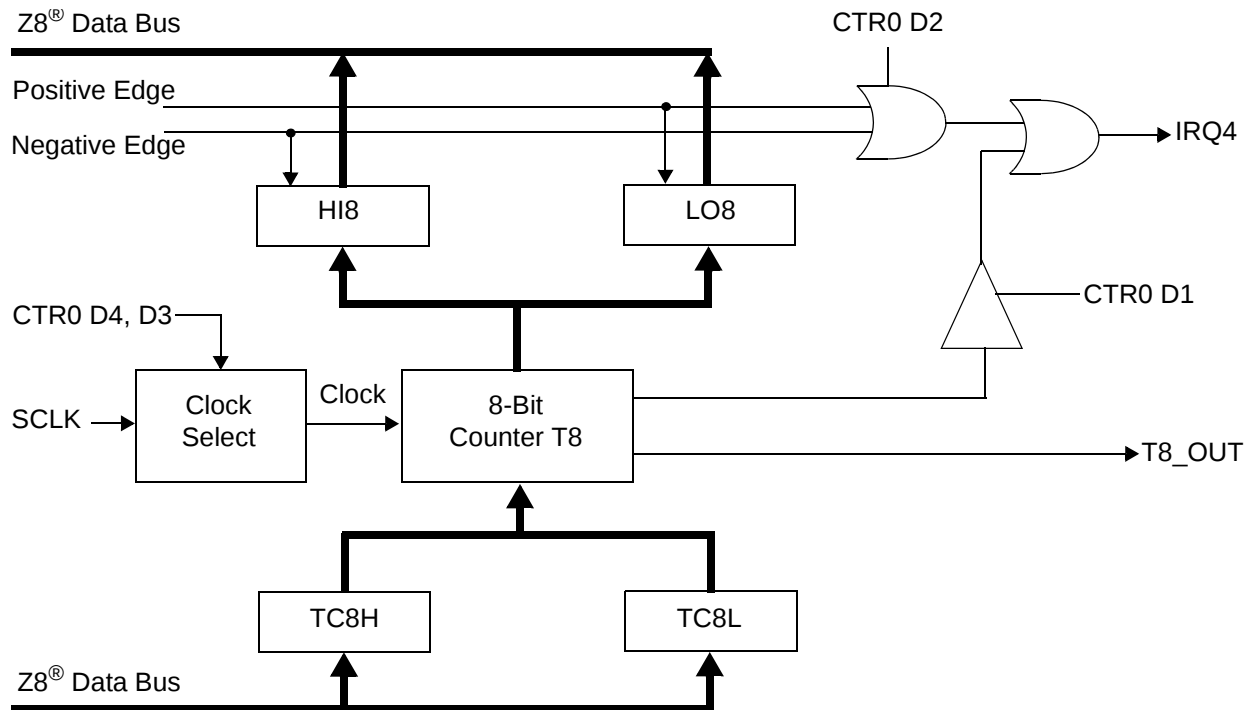


Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



Caution:

Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFE_H. Transition from 0 to FFFF_H is not a timeout condition.

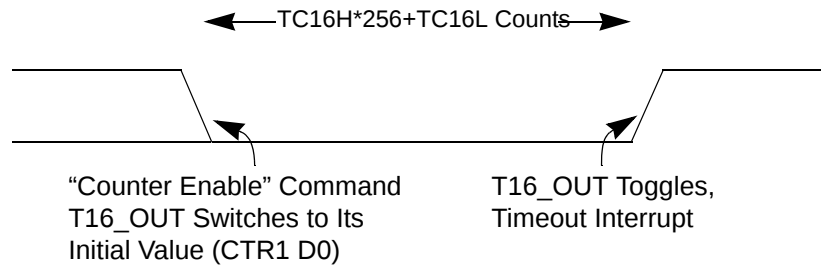


Figure 26. T16_OUT in Single-Pass Mode

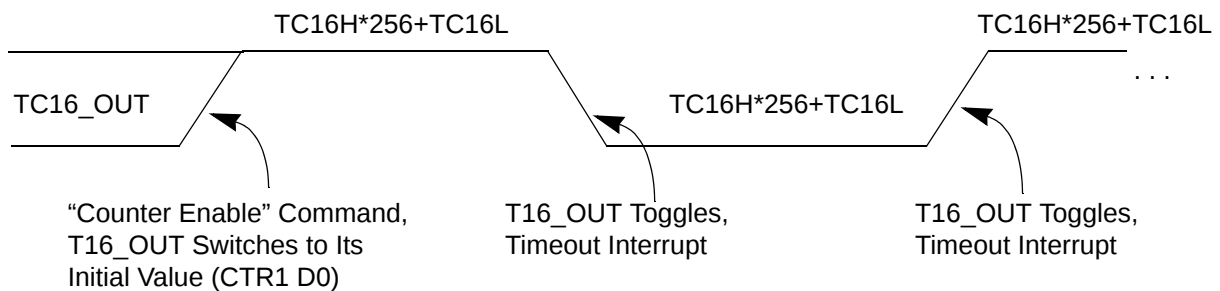


Figure 27. T16_OUT in Modulo-N Mode

T16 DEMODULATION Mode

The user must program TC16L and TC16H to FF_H. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFF_H and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from `FFFFh`. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

- **Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.

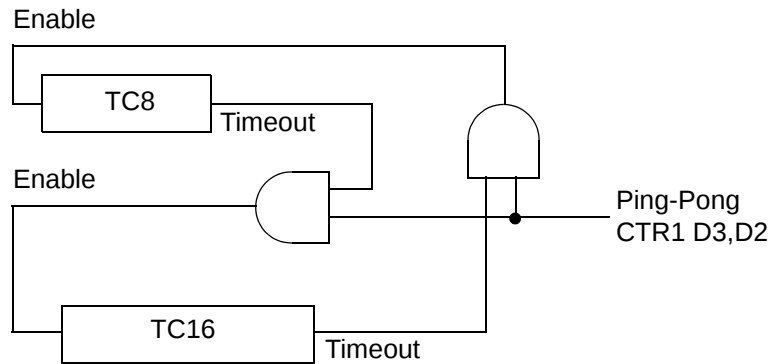


Figure 28. Ping-Pong Mode Diagram

Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.

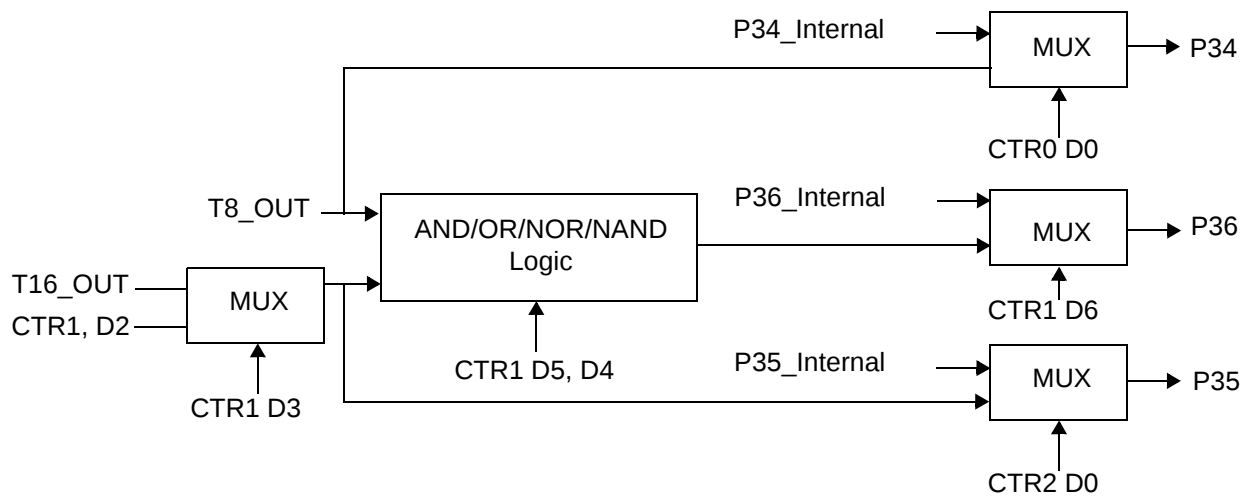
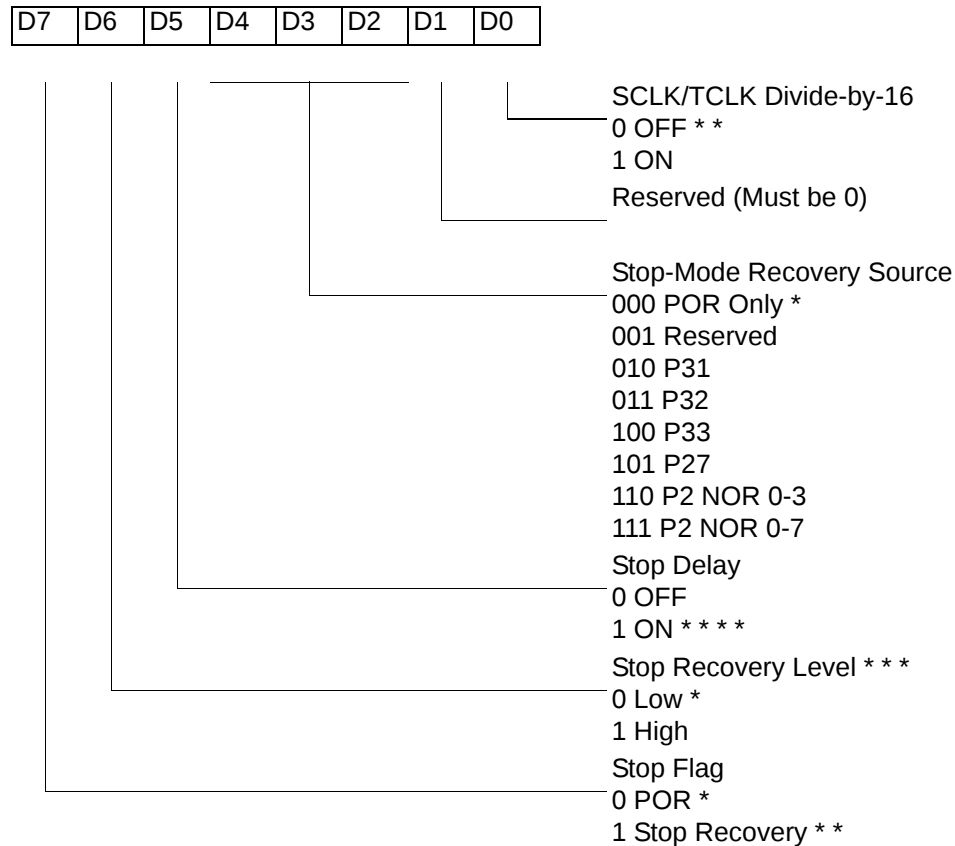


Figure 29. Output Circuit

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.

SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

** Default setting after Reset and Stop Mode Recovery

* * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

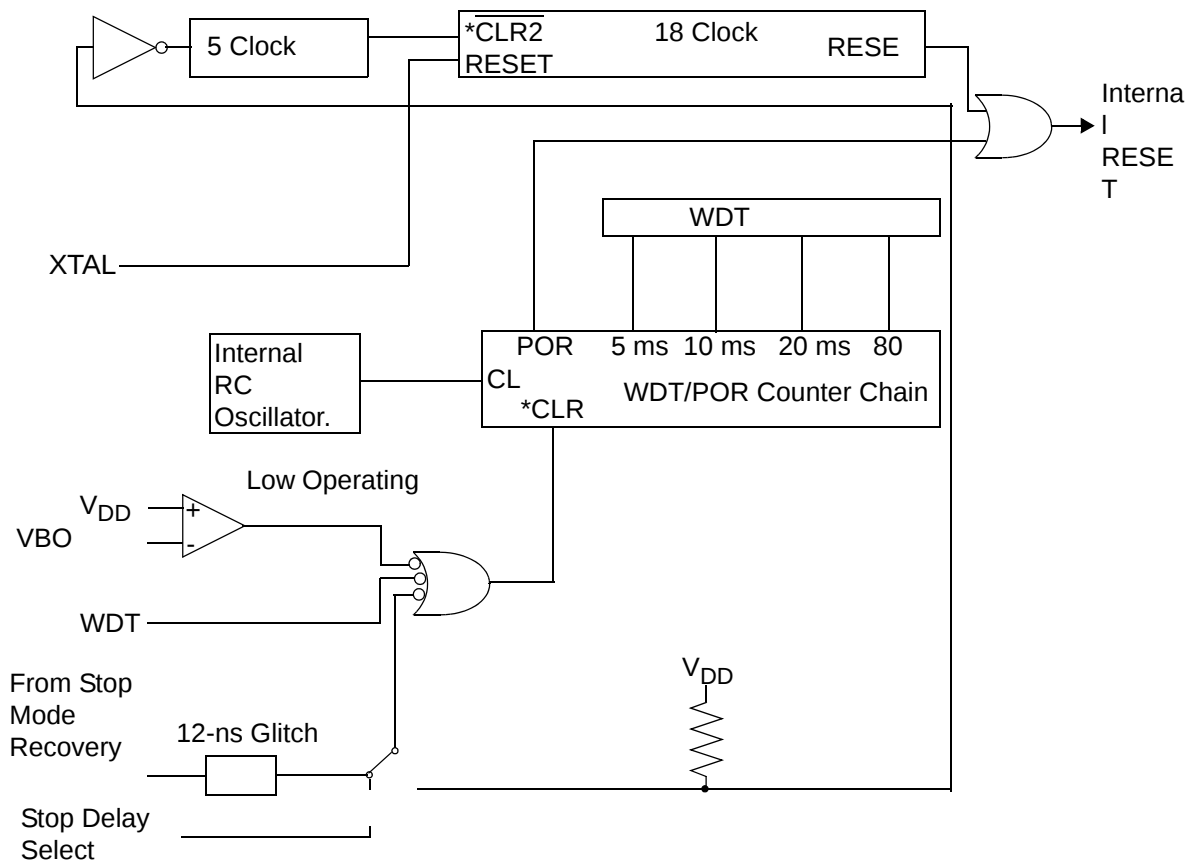
D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

Table 23. Watch-Dog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.

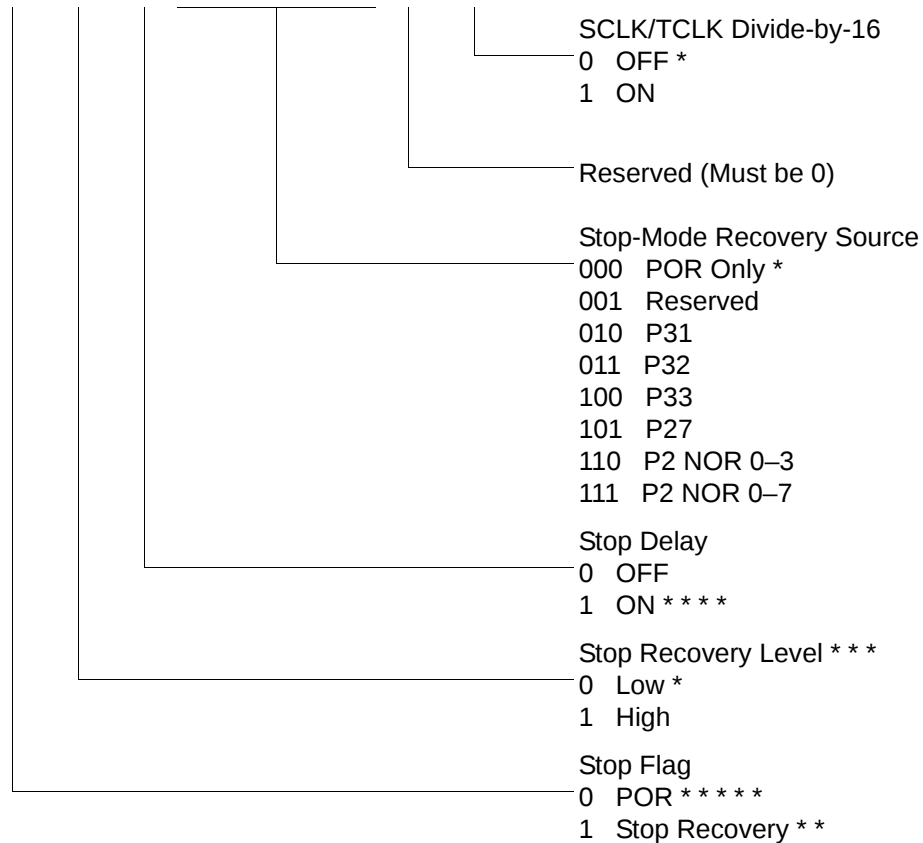


* CLR1 and $\overline{\text{CLR2}}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-

Figure 38. Resets and WDT

SMR(0F)0BH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



* Default setting after reset

** Set after Stop Mode Recovery

*** At the XOR gate input

**** Default setting after reset. Must be 1 if using a crystal or resonator clock source.

***** Default setting after Power On Reset. Not reset with a Stop Mode recovery.

Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)



R250 IRQ(FAH)

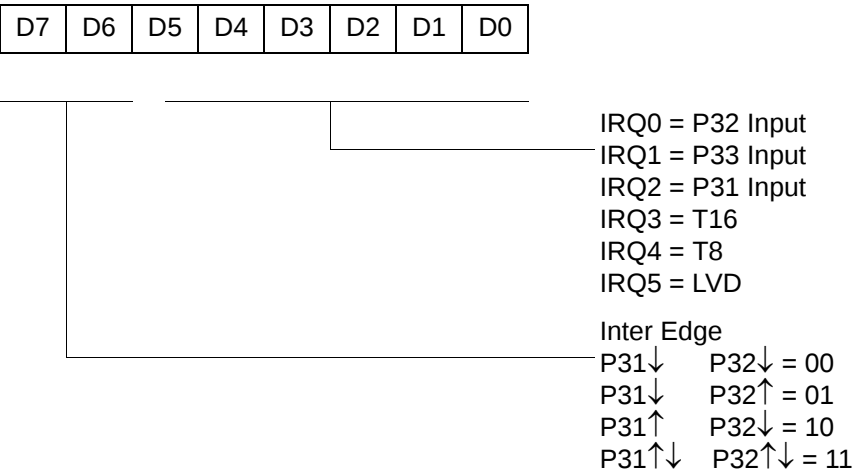


Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



* Default setting after reset
** Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)



R254 SPH(FEH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

General-Purpose Register

Figure 56. Stack Pointer High (FEH: Read/Write)

R255 SPL(FFH)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Stack Pointer Low
Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFH: Read/Write)

Package Information

Package information for all versions of ZGP323H is depicted in Figures 59 through Figure 68.

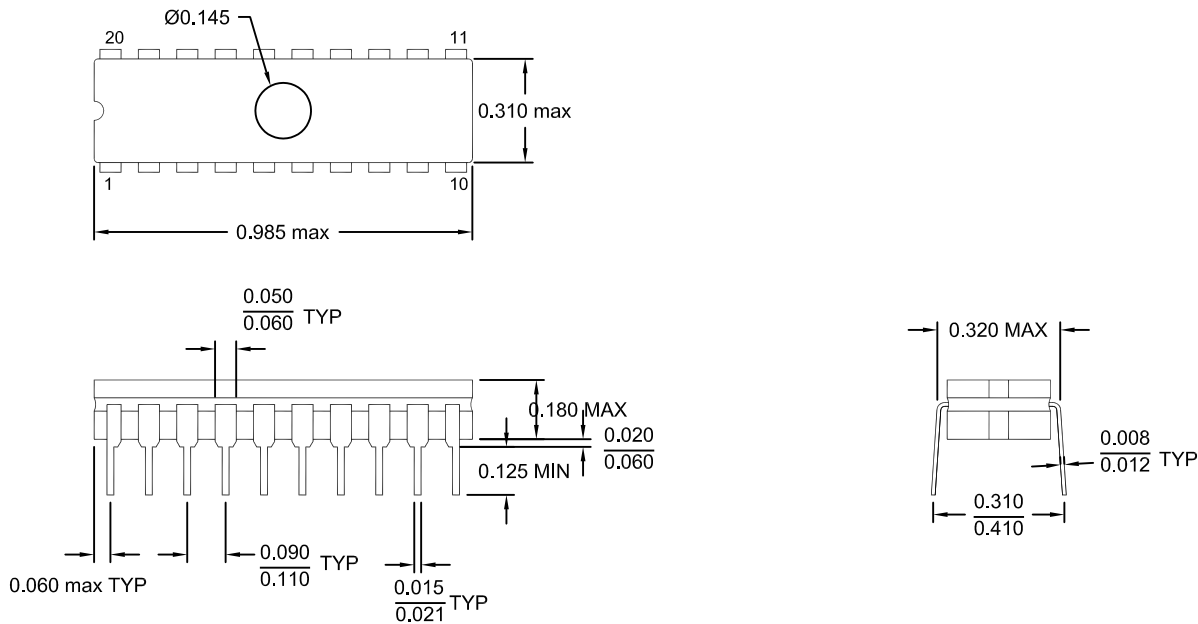


Figure 58. 20-Pin CDIP Package

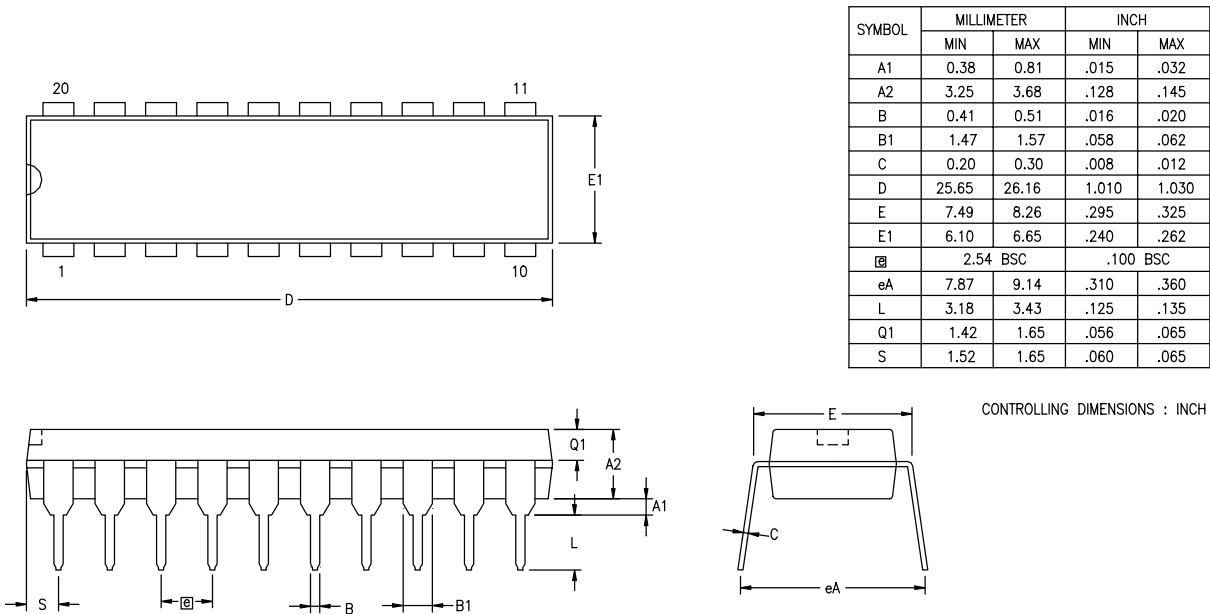


Figure 59. 20-Pin PDIP Package Diagram

- pin 4
- E
- EPROM
 - selectable options 64
- expanded register file 26
- expanded register file architecture 28
- expanded register file control registers 71
 - flag 80
 - interrupt mask register 79
 - interrupt priority register 78
 - interrupt request register 79
 - port 0 and 1 mode register 77
 - port 2 configuration register 75
 - port 3 mode register 76
 - port configuration register 75
 - register pointer 80
 - stack pointer high register 81
 - stack pointer low register 81
 - stop-mode recovery register 73
 - stop-mode recovery register 2 74
 - T16 control register 69
 - T8 and T16 common control functions register 67
 - T8/T16 control register 70
 - TC8 control register 66
 - watch-dog timer register 75
- F
- features
 - standby modes 1
- functional description
 - counter/timer functional blocks 40
 - CTR(D)01h register 35
 - CTR0(D)00h register 33
 - CTR2(D)02h register 37
 - CTR3(D)03h register 39
 - expanded register file 26
 - expanded register file architecture 28
 - HI16(D)09h register 32
 - HI8(D)0Bh register 32
 - L08(D)0Ah register 32
 - L0I6(D)08h register 32
 - program memory map 26
 - RAM 25
 - register description 65
 - register file 30
 - register pointer 29
 - register pointer detail 31
 - SMR2(F)0D1h register 40
 - stack 31
 - TC16H(D)07h register 32
 - TC16L(D)06h register 33
 - TC8H(D)05h register 33
 - TC8L(D)04h register 33
- G
- glitch filter circuitry 40
- H
- halt instruction, counter/timer 54
- I
- input circuit 40
- interrupt block diagram, counter/timer 51
- interrupt types, sources and vectors 52
- L
- low-voltage detection register 65
- M
- memory, program 25
- modulo-N mode
 - T16_OUT 47
 - T8_OUT 43
- O
- oscillator configuration 53
- output circuit, counter/timer 49
- P
- package information
 - 20-pin DIP package diagram 82
 - 20-pin SSOP package diagram 84
 - 28-pin DIP package diagram 86
 - 28-pin SOIC package diagram 85
 - 28-pin SSOP package diagram 87
 - 40-pin DIP package diagram 87
 - 48-pin SSOP package diagram 89
- pin configuration
 - 20-pin DIP/SOIC/SSOP 5

- T8_Capture_LO 32
- register file 30
 - expanded 26
- register pointer 29
 - detail 31
- reset pin function 25
- resets and WDT 63
- S
- SCLK circuit 58
- single-pass mode
 - T16_OUT 47
 - T8_OUT 43
- stack 31
- standard test conditions 10
- standby modes 1
- stop instruction, counter/timer 54
- stop mode recovery
 - 2 register 61
 - source 59
- stop mode recovery 2 61
- stop mode recovery register 57
- T
- T16 transmit mode 46
- T16_Capture_HI 32
- T8 transmit mode 40
- T8_Capture_HI 32
- test conditions, standard 10
- test load diagram 10
- timing diagram, AC 16
- transmit mode flowchart 41
- V
- VCC 5
- voltage
 - brown-out/standby 64
 - detection and flags 65
- voltage detection register 71
- W
- watch-dog timer
 - mode registerwatch-dog timer mode regis-
ter 62
 - time select 63
- X
- XTAL1 5
- XTAL1 pin function 18
- XTAL2 5
- XTAL2 pin function 18