



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hsh2004g



List of Figures

Figure 1. Functional Block Diagram	3
Figure 2. Counter/Timers Diagram	4
Figure 3. 20-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	5
Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration	6
Figure 5. 40-Pin PDIP/CDIP* Pin Configuration	7
Figure 6. 48-Pin SSOP Pin Configuration	8
Figure 7. Test Load Diagram	10
Figure 8. AC Timing Diagram	16
Figure 9. Port 0 Configuration	19
Figure 10. Port 1 Configuration	20
Figure 11. Port 2 Configuration	21
Figure 12. Port 3 Configuration	22
Figure 13. Port 3 Counter/Timer Output Configuration	24
Figure 14. Program Memory Map (32K OTP)	26
Figure 15. Expanded Register File Architecture	28
Figure 16. Register Pointer	29
Figure 17. Register Pointer—Detail	31
Figure 18. Glitch Filter Circuitry	40
Figure 19. Transmit Mode Flowchart	41
Figure 20. 8-Bit Counter/Timer Circuits	42
Figure 21. T8_OUT in Single-Pass Mode	43
Figure 22. T8_OUT in Modulo-N Mode	43
Figure 23. Demodulation Mode Count Capture Flowchart	44
Figure 24. Demodulation Mode Flowchart	45
Figure 25. 16-Bit Counter/Timer Circuits	46
Figure 26. T16_OUT in Single-Pass Mode	47
Figure 27. T16_OUT in Modulo-N Mode	47
Figure 28. Ping-Pong Mode Diagram	49
Figure 29. Output Circuit	49
Figure 30. Interrupt Block Diagram	51
Figure 31. Oscillator Configuration	53
Figure 32. Port Configuration Register (PCON) (Write Only)	55
Figure 33. STOP Mode Recovery Register	57



Figure 34. SCLK Circuit	58
Figure 35. Stop Mode Recovery Source	59
Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only) . .	61
Figure 37. Watch-Dog Timer Mode Register (Write Only).....	62
Figure 38. Resets and WDT	63
Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)	66
Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write) . . .	67
Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted) .	69
Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted).....	70
Figure 43. Voltage Detection Register	71
Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)	72
Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only)	73
Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)	74
Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only).	75
Figure 48. Port 2 Mode Register (F6H: Write Only).	75
Figure 49. Port 3 Mode Register (F7H: Write Only)	76
Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)	77
Figure 51. Interrupt Priority Register (F9H: Write Only)	78
Figure 52. Interrupt Request Register (FAH: Read/Write)	79
Figure 53. Interrupt Mask Register (FBH: Read/Write)	79
Figure 54. Flag Register (FCH: Read/Write)	80
Figure 55. Register Pointer (FDH: Read/Write)	80
Figure 56. Stack Pointer High (FEH: Read/Write)	81
Figure 57. Stack Pointer Low (FFH: Read/Write)	81
Figure 58. 20-Pin CDIP Package	82
Figure 59. 20-Pin PDIP Package Diagram	82
Figure 60. 20-Pin SOIC Package Diagram	83
Figure 61. 20-Pin SSOP Package Diagram	84
Figure 62. 28-Pin SOIC Package Diagram	85
Figure 63. 28-Pin CDIP Package Diagram	86
Figure 64. 28-Pin PDIP Package Diagram	86
Figure 65. 28-Pin SSOP Package Diagram.....	87
Figure 66. 40-Pin PDIP Package Diagram	87
Figure 67. 40-Pin CDIP Package Diagram	88



Table 10. GP323HE DC Characteristics (Continued)

Symbol	Parameter	V _{CC}	T _A = -40°C to +105°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	I _{OL} = 4.0mA	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V		
I _{IL}	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled	
R _{PU}	Pull-up Resistance	2.0V	200.0		700.0	KΩ	V _{IN} = 0V; Pullups selected by mask option	
		3.6V	50.0		300.0	KΩ		
		5.0V	25.0		175.0	KΩ		
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC}	
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I _{CC1}	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I _{CC2}	Standby Current (Stop Mode)	2.0V		1.6	12	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		3.6V		1.8	15	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		5.5V		1.9	18	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		2.0V		5	30	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		3.6V		8	40	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		5.5V		15	60	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V		
V _{HVD}	V _{CC} High Voltage Detection			2.7		V		

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V_{CC} and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

Table 11. GP323HA DC Characteristics

T_A = -40°C to +125°C								
Symbol	Parameter	V_{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	I _{OH} = -0.5mA	
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	I _{OL} = 4.0mA	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V		
I _{IL}	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled	
R _{PU}	Pull-up Resistance	2.0V	200		700	KΩ	V _{IN} = 0V; Pullups selected by mask option	
		3.6V	50		300	KΩ		
		5.0V	25		175	KΩ		
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC}	
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I _{CC1}	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I _{CC2}	Standby Current (Stop Mode)	2.0V		1.6	15	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		3.6V		1.8	20	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		5.5V		1.9	25	μA	V _{IN} = 0 V, V _{CC} WDT not Running	3
		2.0V		5	30	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		3.6V		8	40	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
		5.5V		15	60	μA	V _{IN} = 0 V, V _{CC} WDT is Running	3
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V		



AC Characteristics

Figure 8 and Table 13 describe the Alternating Current (AC) characteristics.

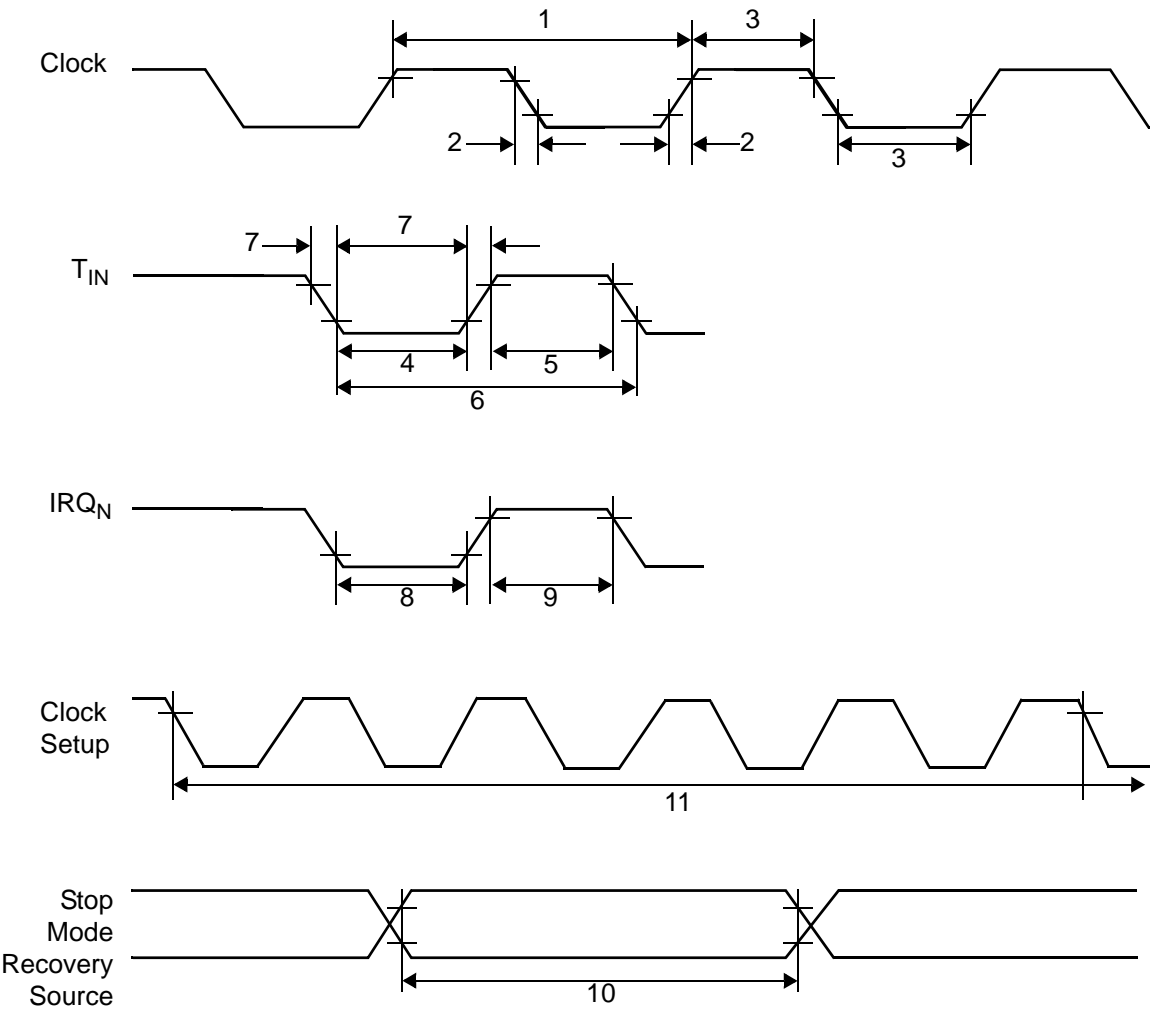


Figure 8. AC Timing Diagram

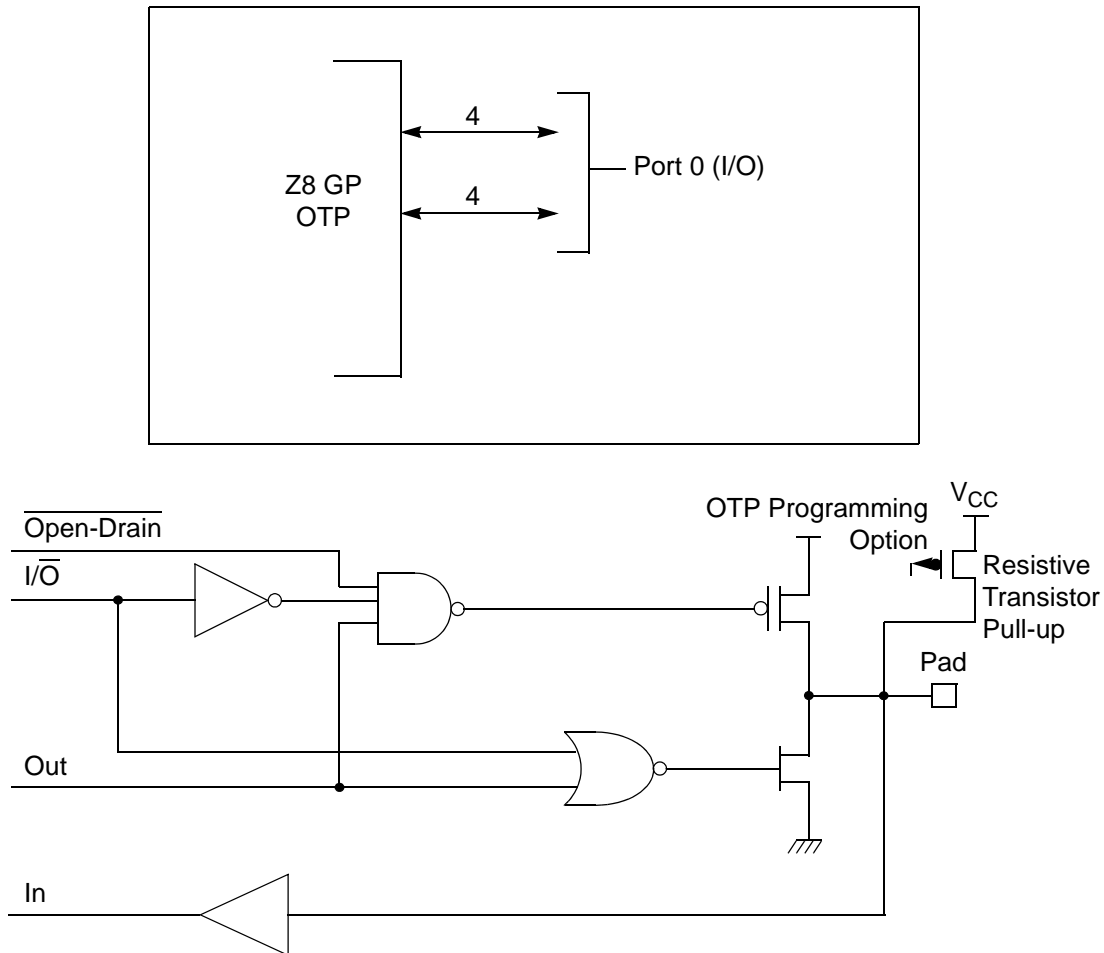


Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.

► **Note:** The Port 1 direction is reset to its default state following an SMR.



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

- **Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).

Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position	Description
T8_Capture_HI	[7:0]	R/W Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position	Description
T8_Capture_LO	[7:0]	R/W Captured Data - No Effect

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position	Description
T16_Capture_HI	[7:0]	R/W Captured Data - No Effect

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position	Description
T16_Data_HI	[7:0]	R/W Data



Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position	Description
T16_Data_LO	[7:0]	R/W Data

Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position	Description
T8_Level_HI	[7:0]	R/W Data

Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position	Description
T8_Level_LO	[7:0]	R/W Data

CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

Table 15. CTR0(D)00H Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-----	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5-----	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8_Clock	---43---	R/W	0 0**	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_Mask	----2--	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt

► **Note:** The letter *h* denotes hexadecimal values.

Transition from 0 to FF_h is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.

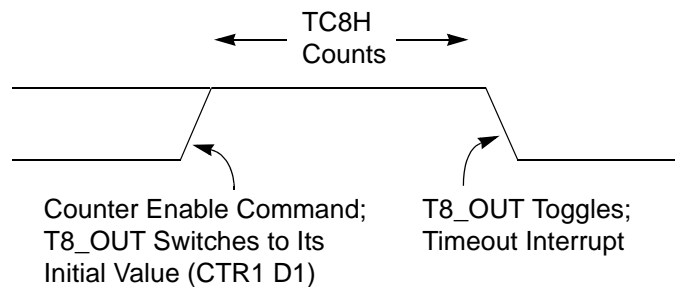


Figure 21. T8_OUT in Single-Pass Mode

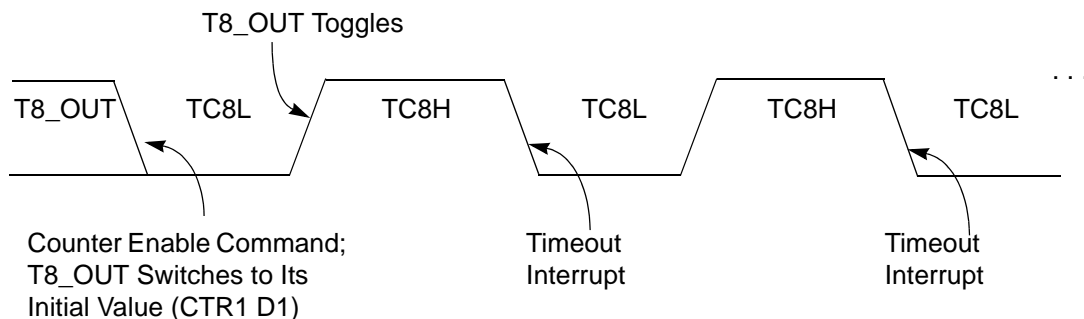


Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FF_h. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).

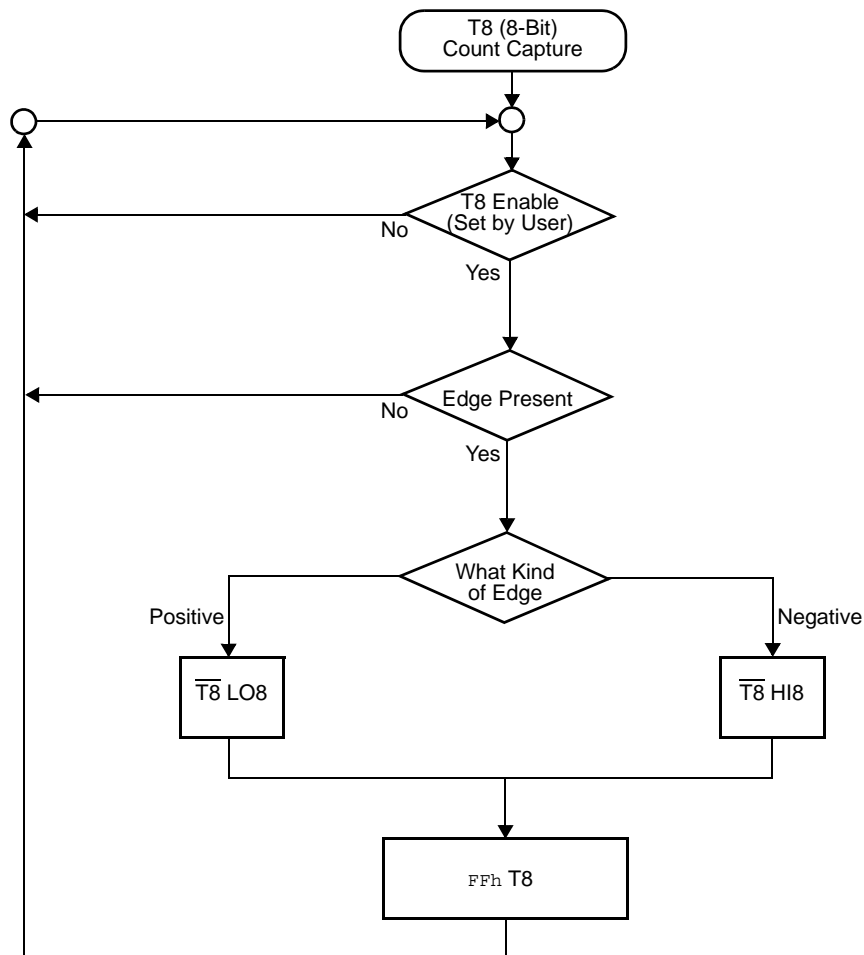


Figure 23. Demodulation Mode Count Capture Flowchart

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from `FFFFh`. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

- **Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal or ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.

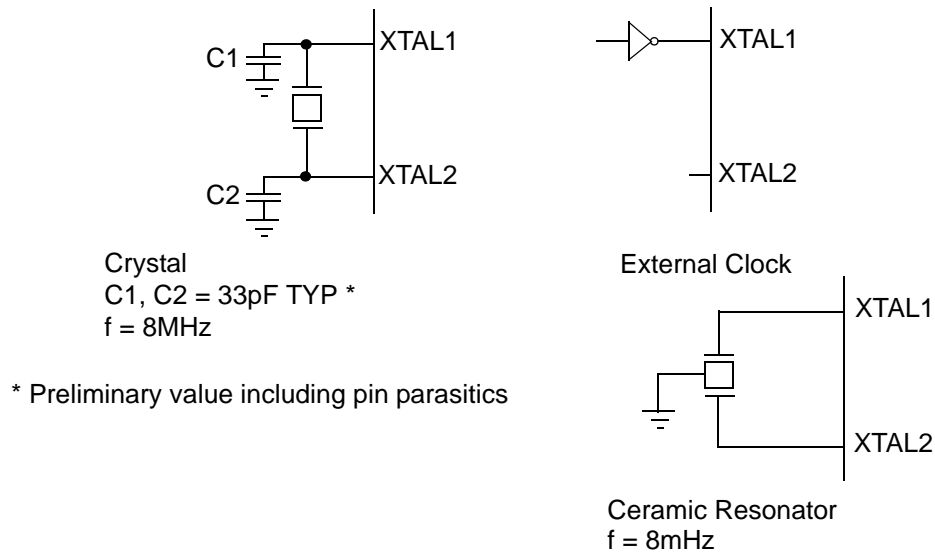


Figure 31. Oscillator Configuration

Table 22. Stop Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

- **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 61 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 T_{pC} .

- **Note:** This bit must be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

CTR1(0D)01H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

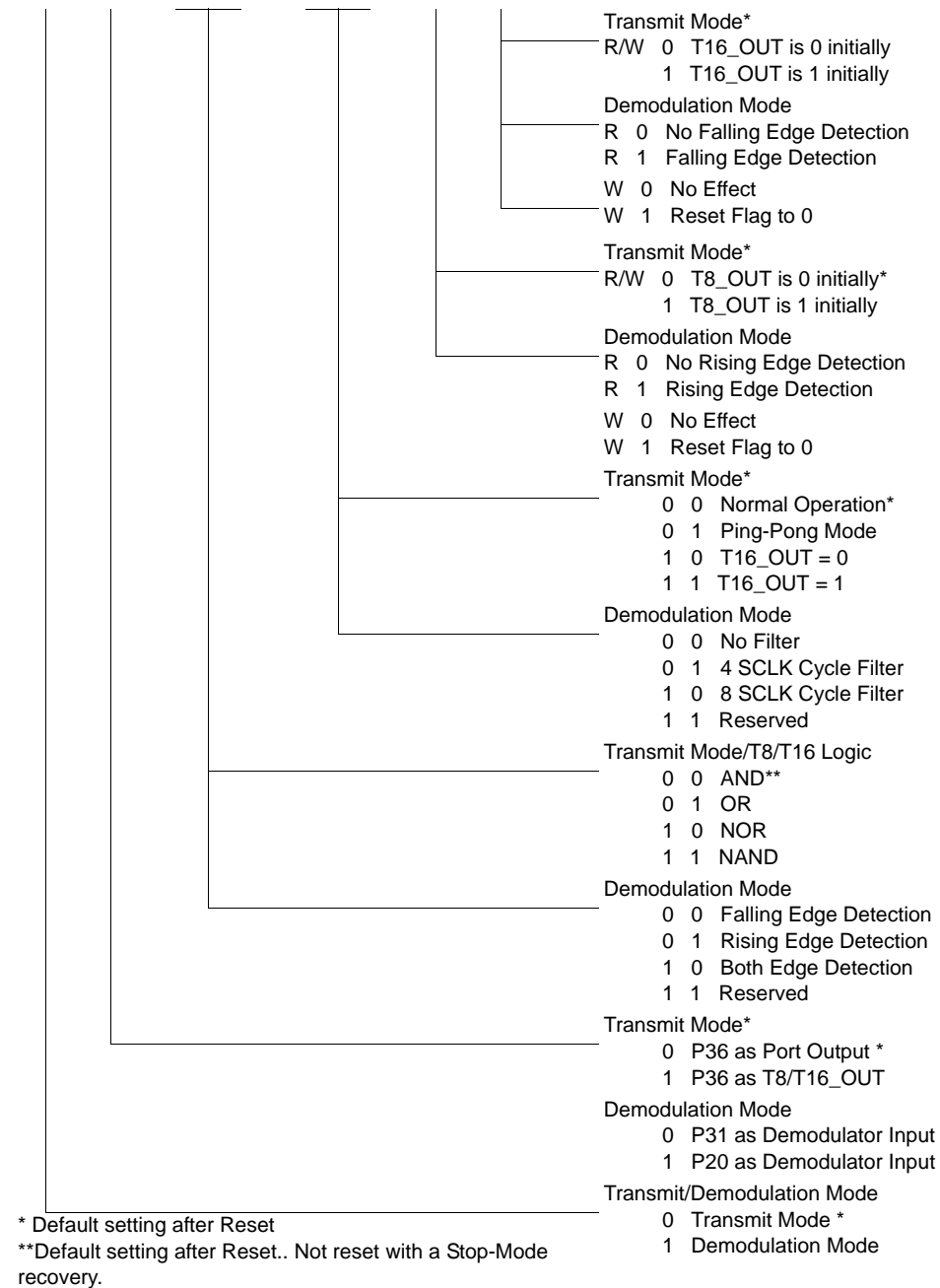
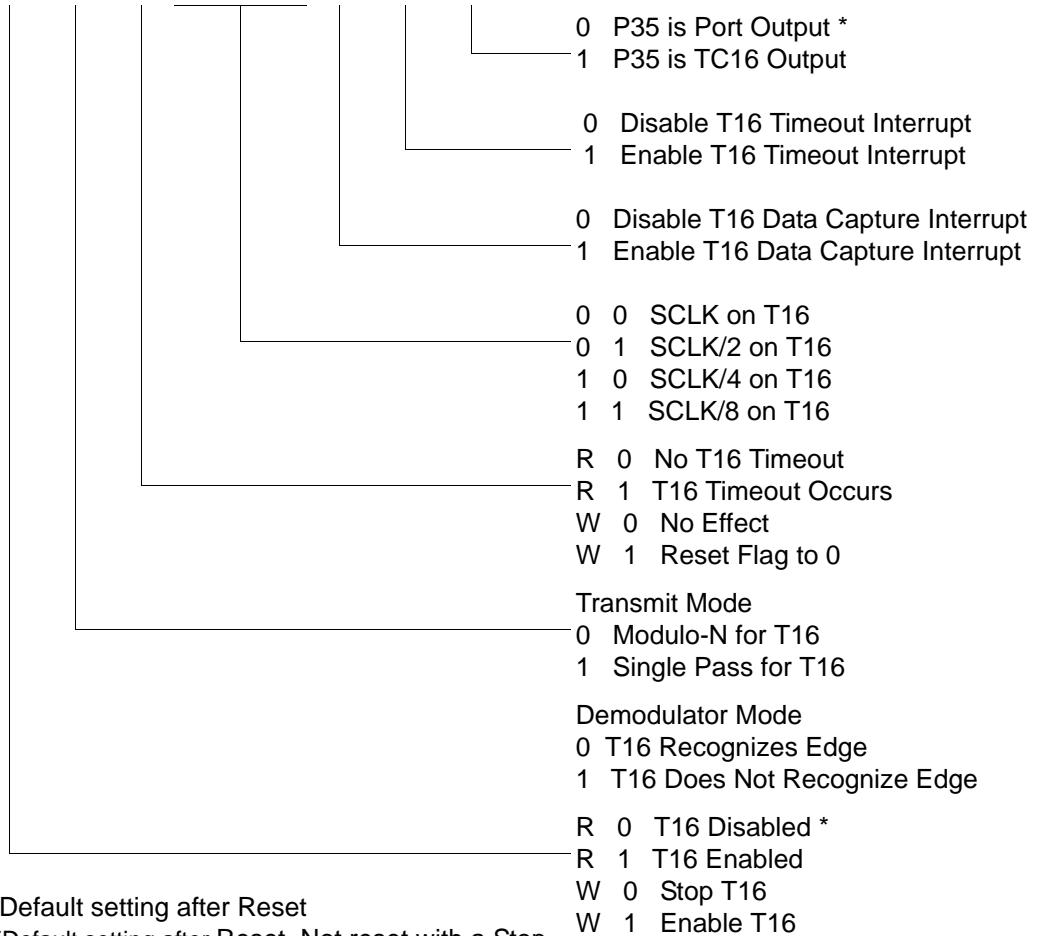


Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)

CTR2(0D)02H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



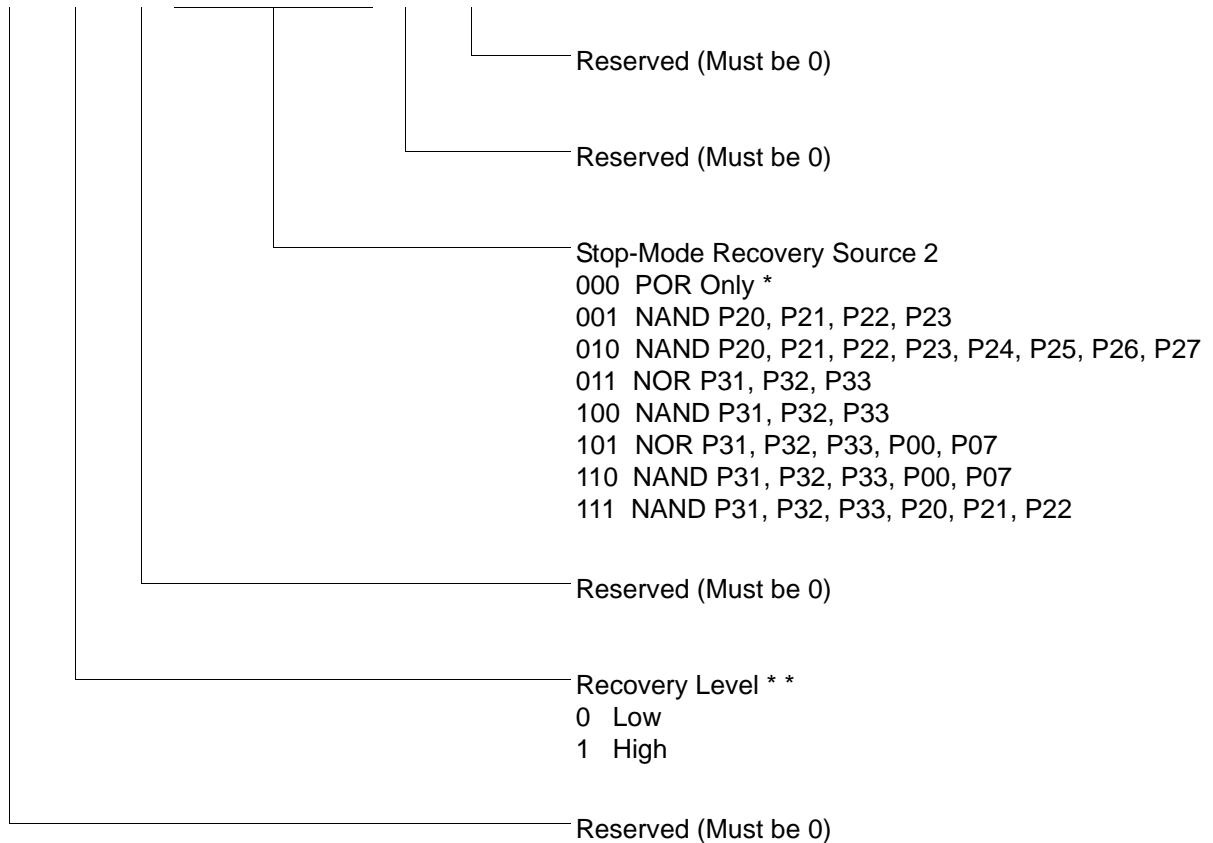
* Default setting after Reset

**Default setting after Reset. Not reset with a Stop-Mode recovery.

Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)

SMR2(0F)0DH

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

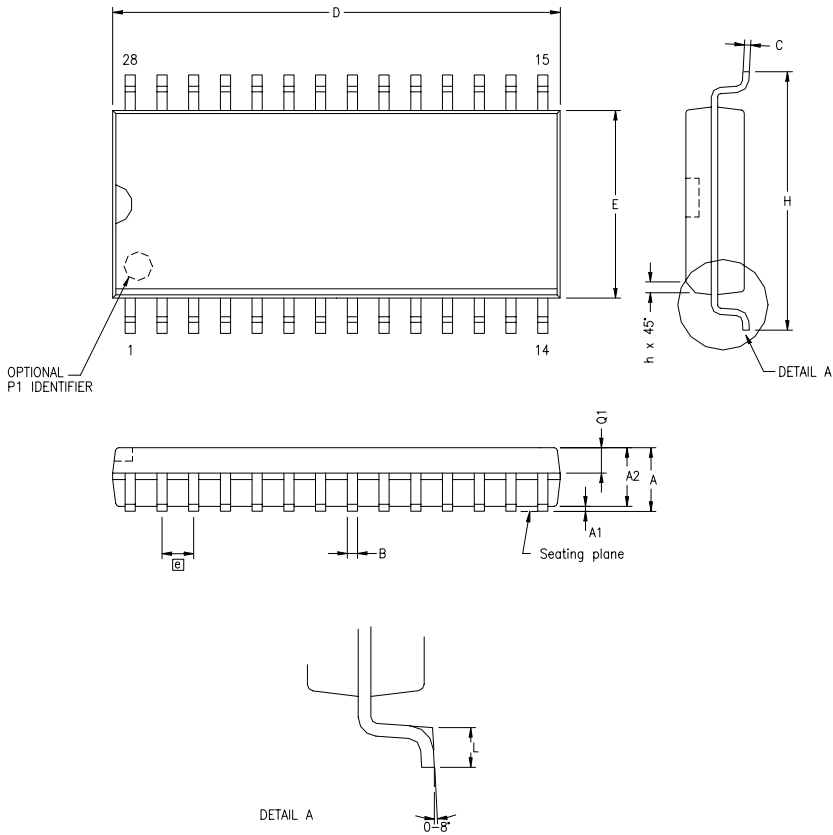


Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset. Not reset with a Stop Mode recovery.

* * At the XOR gate input

Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
@	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 62. 28-Pin SOIC Package Diagram



16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4816C	48-pin SSOP 16K OTP	ZGP323HSS2816C	28-pin SOIC 16K OTP
ZGP323HSP4016C	40-pin PDIP 16K OTP	ZGP323HSH2016C	20-pin SSOP 16K OTP
ZGP323HSH2816C	28-pin SSOP 16K OTP	ZGP323HSP2016C	20-pin PDIP 16K OTP
ZGP323HSP2816C	28-pin PDIP 16K OTP	ZGP323HSS2016C	20-pin SOIC 16K OTP

16KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4816C	48-pin SSOP 16K OTP	ZGP323HES2816C	28-pin SOIC 16K OTP
ZGP323HEP4016C	40-pin PDIP 16K OTP	ZGP323HEH2016C	20-pin SSOP 16K OTP
ZGP323HEH2816C	28-pin SSOP 16K OTP	ZGP323HEP2016C	20-pin PDIP 16K OTP
ZGP323HEP2816C	28-pin PDIP 16K OTP	ZGP323HES2016C	20-pin SOIC 16K OTP

16KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323HAH4816C	48-pin SSOP 16K OTP	ZGP323HAS2816C	28-pin SOIC 16K OTP
ZGP323HAP4016C	40-pin PDIP 16K OTP	ZGP323HAH2016C	20-pin SSOP 16K OTP
ZGP323HAH2816C	28-pin SSOP 16K OTP	ZGP323HAP2016C	20-pin PDIP 16K OTP
ZGP323HAP2816C	28-pin PDIP 16K OTP	ZGP323HAS2016C	20-pin SOIC 16K OTP

Replace C with G for Lead-Free Packaging



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

H = High Voltage

T = Temperature

S = Standard 0° to +70°C

E = Extended -40° to +105°C

A = Automotive -40° to +125°C

P = Package Type:

K = CDIP

P = PDIP

H = SSOP

S = SOIC

= Number of Pins

CC = Memory Size

M = Molding Compound

C = Standard Plastic Packaging Molding Compound

G = Green Plastic Molding Compound

E = Standard Cer Dip flow