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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hsh2804g

List of Figures

Development Features

Table 2 lists the features of ZiLOG®'s ZGP323H members.

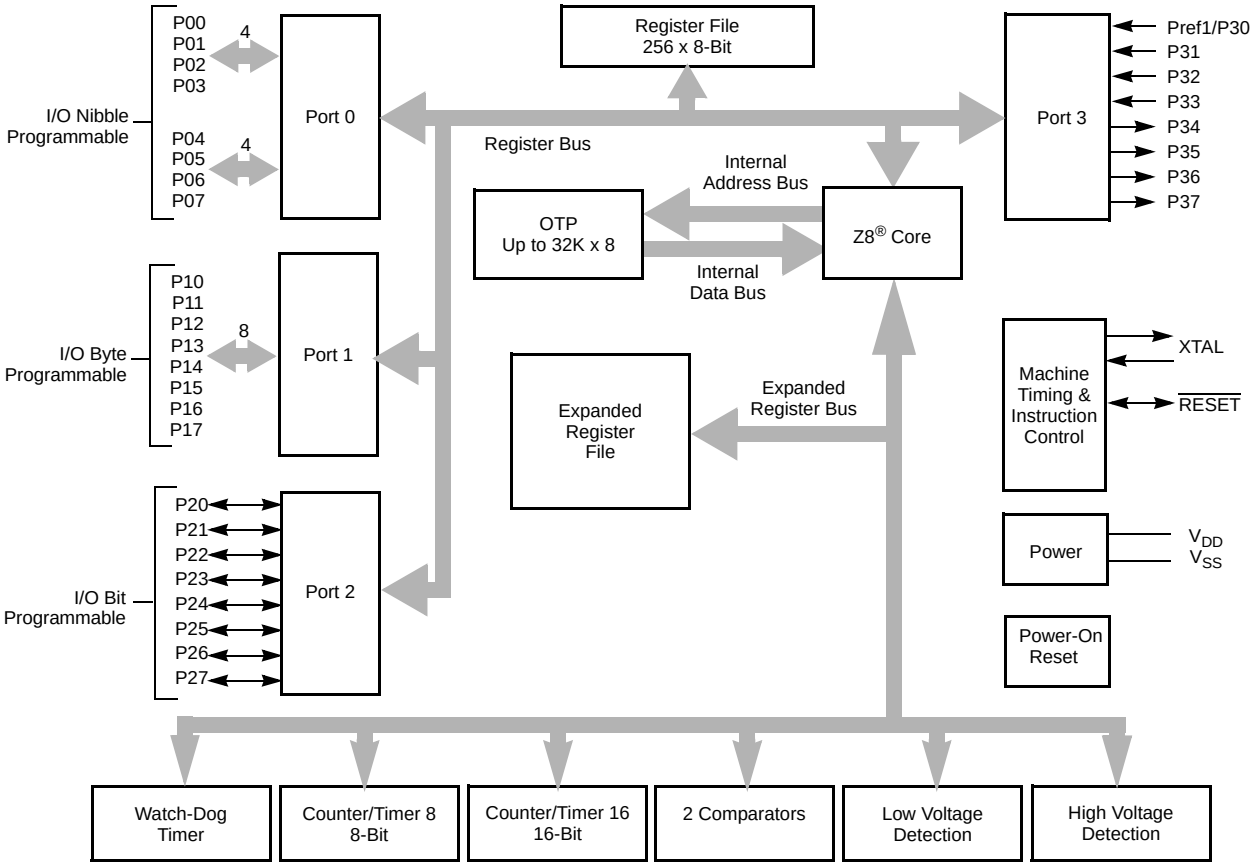
Table 2. Features

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323H OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–5.5V

- Low power consumption–18mW (typical)
- T = Temperature
  S = Standard 0° to +70°C
  E = Extended -40° to +105°C
  A = Automotive -40° to +125°C
- Three standby modes:
  - STOP— (typical 1.8µA)
  - HALT— (typical 0.8mA)
  - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors

Table 3. Power Connections

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram

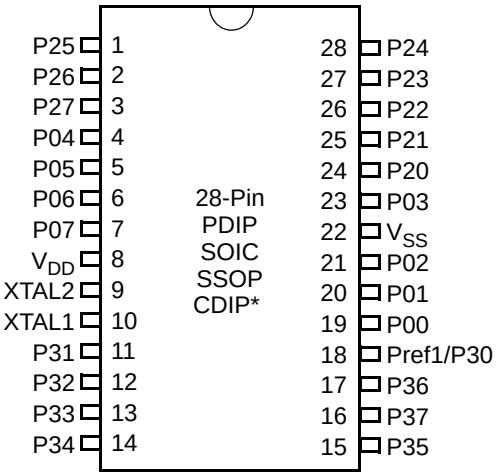


Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Configuration

Table 5. 28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V_{DD}		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V_{CC} if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V_{SS}		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

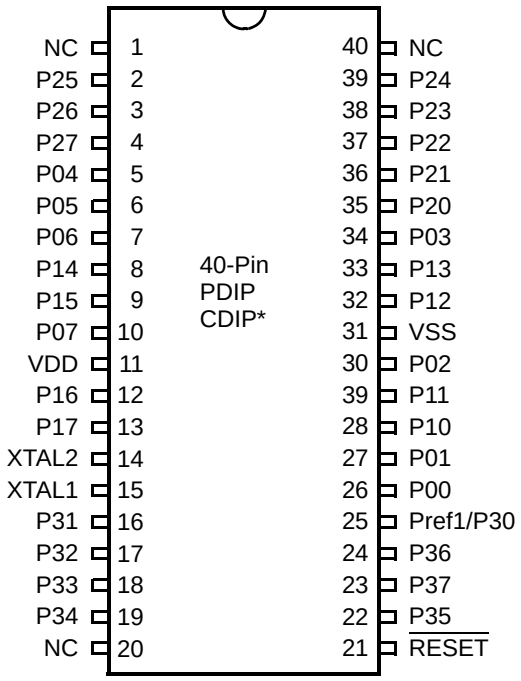


Figure 5. 40-Pin PDIP/CDIP* Pin Configuration

Note: *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

Capacitance

Table 8 lists the capacitances.

Table 8. Capacitance

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: T_A = 25° C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND	

DC Characteristics

Table 9. GP323HS DC Characteristics

			T_A=0°C to +70°C					
Symbol	**Parameter**	**V_{CC}**	**Min**	**Typ(7)**	**Max**	**Units**	**Conditions**	**Notes**
V_{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-5.5	0.8 V_{CC}		V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-5.5	V_{SS}–0.3		0.4	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-5.5	0.7 V_{CC}		V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0-5.5	V_{SS}–0.3		0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0-5.5	V_{CC}–0.4			V	I_{OH} = –0.5mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V_{CC}–0.8			V	I_{OH} = –7mA	
V_{OL1}	Output Low Voltage	2.0-5.5			0.4	V	I_{OL} = 4.0mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I_{OL} = 10mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-5.5	0		V_{CC} 1.75	V		
I_{IL}	Input Leakage	2.0-5.5	–1		1	µA	V_{IN} = 0V, V_{CC} Pull-ups disabled	
R_{PU}	Pull-up Resistance	2.0V	225		675	KΩ	V_{IN} = 0V; Pullups selected by mask option	
		3.6V	75		275	KΩ		
		5.0V	40		160	KΩ		

Table 9. GP323HS DC Characteristics (Continued)

			T_A=0°C to +70°C					
Symbol	**Parameter**	**V_{CC}**	**Min**	**Typ(7)**	**Max**	**Units**	**Conditions**	**Notes**
I_{OL}	Output Leakage	2.0-5.5	–1		1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I_{CC1}	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I_{CC2}	Standby Current (Stop Mode)	2.0V		1.6	8	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		3.6V		1.8	10	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		5.5V		1.9	12	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		2.0V		5	20	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		3.6V		8	30	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		5.5V		15	45	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
I_{LV}	Standby Current (Low Voltage)			1.2	6	µA	Measured at 1.3V	4
V_{BO}	V_{CC} Low Voltage Protection			1.9	2.0	V	8MHz maximum Ext. CLK Freq.	
V_{LVD}	V_{CC} Low Voltage Detection			2.4		V		
V_{HVD}	Vcc High Voltage Detection			2.7		V		

Notes:
1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 µF), physically close to VCC and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

Table 10. GP323HE DC Characteristics

			T_A= -40°C to +105°C					
Symbol	**Parameter**	**V_{CC}**	**Min**	**Typ(7)**	**Max**	**Units**	**Conditions**	**Notes**
V_{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-5.5	0.8 V_{CC}		V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-5.5	V_{SS}–0.3		0.4	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-5.5	0.7 V_{CC}		V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0-5.5	V_{SS}–0.3		0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0-5.5	V_{CC}–0.4			V	I_{OH} = –0.5mA	

Table 10. GP323HE DC Characteristics (Continued)

			T_A= -40°C to +105°C					
Symbol	**Parameter**	**V_{CC}**	**Min**	**Typ(7)**	**Max**	**Units**	**Conditions**	**Notes**
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V_{CC}–0.8			V	I_{OH} = –7mA	
V_{OL1}	Output Low Voltage	2.0-5.5			0.4	V	I_{OL} = 4.0mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I_{OL} = 10mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-5.5	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-5.5	–1		1	µA	V_{IN} = 0V, V_{CC} Pull-ups disabled	
R_{PU}	Pull-up Resistance	2.0V	200.0		700.0	KΩ	V_{IN} = 0V; Pullups selected by mask option	
		3.6V	50.0		300.0	KΩ		
		5.0V	25.0		175.0	KΩ		
I_{OL}	Output Leakage	2.0-5.5	–1		1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I_{CC1}	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I_{CC2}	Standby Current (Stop Mode)	2.0V		1.6	12	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		3.6V		1.8	15	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		5.5V		1.9	18	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		2.0V		5	30	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		3.6V		8	40	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		5.5V		15	60	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
I_{LV}	Standby Current (Low Voltage)			1.2	6	µA	Measured at 1.3V	4
V_{BO}	V_{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V_{LVD}	V_{CC} Low Voltage Detection			2.4		V		
V_{HVD}	Vcc High Voltage Detection			2.7		V		

Notes:

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V_{CC} falls below V_{BO} limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 µF), physically close to VCC and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

Table 11. GP323HA DC Characteristics

			T_A= -40°C to +125°C					
Symbol	**Parameter**	**V_{CC}**	**Min**	**Typ(7)**	**Max**	**Units**	**Conditions**	**Notes**
V_{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V_{CH}	Clock Input High Voltage	2.0-5.5	0.8 V_{CC}		V_{CC}+0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0-5.5	V_{SS}–0.3		0.4	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0-5.5	0.7 V_{CC}		V_{CC}+0.3	V		
V_{IL}	Input Low Voltage	2.0-5.5	V_{SS}–0.3		0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.0-5.5	V_{CC}–0.4			V	I_{OH} = –0.5mA	
V_{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V_{CC}–0.8			V	I_{OH} = –7mA	
V_{OL1}	Output Low Voltage	2.0-5.5			0.4	V	I_{OL} = 4.0mA	
V_{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I_{OL} = 10mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V_{REF}	Comparator Reference Voltage	2.0-5.5	0		V_{DD} -1.75	V		
I_{IL}	Input Leakage	2.0-5.5	–1		1	µA	V_{IN} = 0V, V_{CC} Pull-ups disabled	
R_{PU}	Pull-up Resistance	2.0V	200		700	KΩ	V_{IN} = 0V; Pullups selected by mask option	
		3.6V	50		300	KΩ		
		5.0V	25		175	KΩ		
I_{OL}	Output Leakage	2.0-5.5	–1		1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I_{CC1}	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V_{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I_{CC2}	Standby Current (Stop Mode)	2.0V		1.6	15	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		3.6V		1.8	20	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		5.5V		1.9	25	µA	V_{IN} = 0 V, V_{CC} WDT not Running	3
		2.0V		5	30	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		3.6V		8	40	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
		5.5V		15	60	µA	V_{IN} = 0 V, V_{CC} WDT is Running	3
I_{LV}	Standby Current (Low Voltage)			1.2	6	µA	Measured at 1.3V	4
V_{BO}	V_{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V_{LVD}	V_{CC} Low Voltage Detection			2.4		V		

Table 13. AC Characteristics

				T_A=0°C to +70°C (S) –40°C to +105°C (E) –40°C to +125°C (A) 8.0MHz				Watch-Dog Timer Mode Register (D1, D0)
No	**Symbol**	**Parameter**	**V_{CC}**	**Minimum**	**Maximum**	**Units**	**Notes**	
1	TpC	Input Clock Period	2.0–5.5	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–5.5		25	ns	1	
3	TwC	Input Clock Width	2.0–5.5	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 5.5	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–5.5	3TpC			1	
6	TpTin	Timer Input Period	2.0–5.5	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–5.5		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 5.5	100 70		ns	1, 2	
9	TwIH	Interrupt Request Input High Time	2.0–5.5	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width Spec	2.0–5.5	12 5TpC		ns	3 4	
11	Tost	Oscillator Start-Up Time	2.0–5.5		5TpC		4	
12	Twdt	Watch-Dog Timer Delay Time	2.0–5.5 2.0–5.5 2.0–5.5 2.0–5.5	5 10 20 80		ms ms ms ms		0, 0 0, 1 1, 0 1, 1
13	T_{POR}	Power-On Reset	2.0–5.5	2.5	10	ms		

Notes:
1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. SMR – D5 = 1.
4. SMR – D5 = 0.

Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

Table 16. CTR1(0D)01H T8 and T16 Common Functions

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/	-6------	R/W		Transmit Mode
Demodulator_Input			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0*	P31
			1	P20
T8/T16_Logic/	--54----	R/W		Transmit Mode
Edge _Detect			00**	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

T8/T16_Logic/Edge _Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

Initial_T8_Out/Rising_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Note: Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

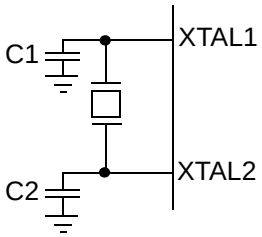
CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 17 lists and briefly describes the fields for this register.

Clock

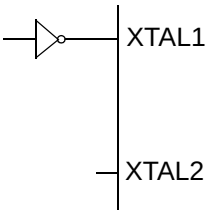
The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal or ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω. The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.

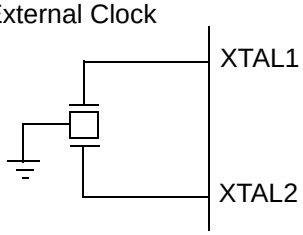


Crystal
C1, C2 = 33pF TYP *
f = 8MHz

* Preliminary value including pin parasitics



External Clock



Ceramic Resonator
f = 8mHz

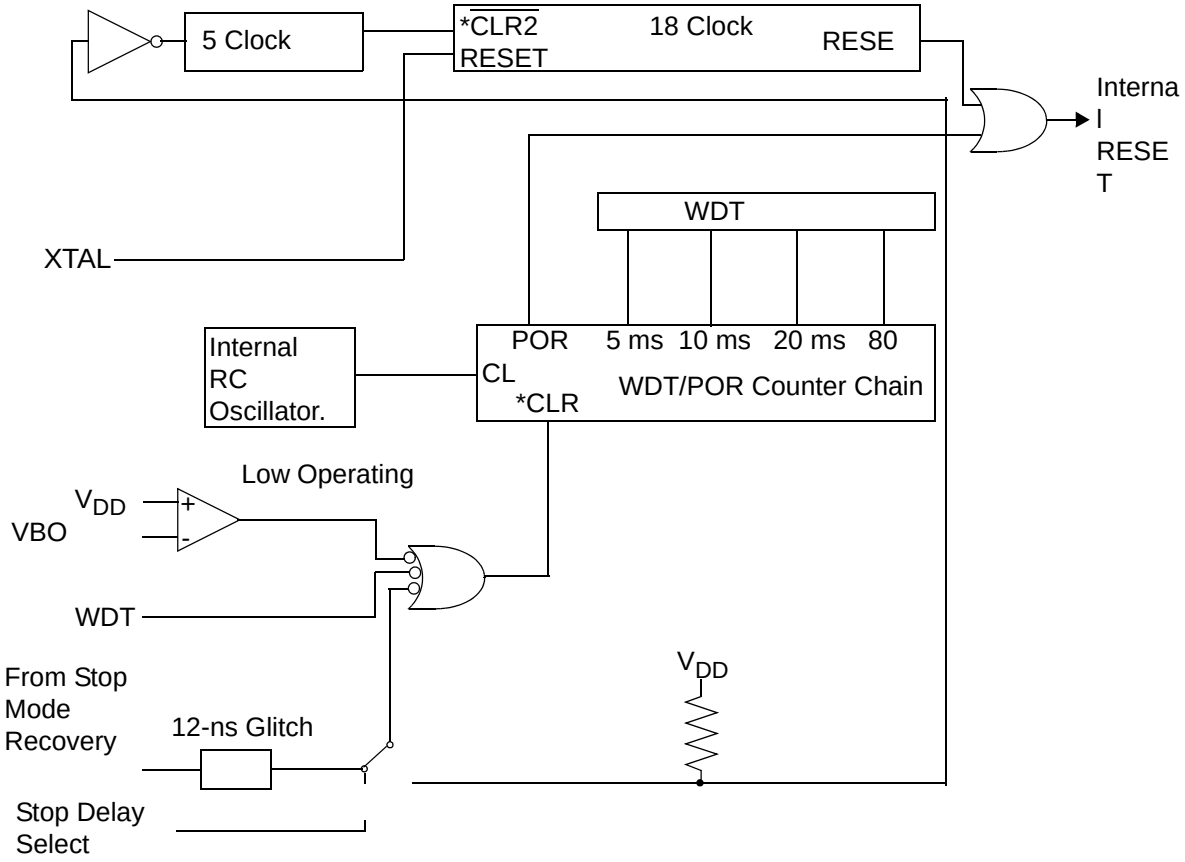
Figure 31. Oscillator Configuration

Table 23. Watch-Dog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

WDTMR During Halt (D2)

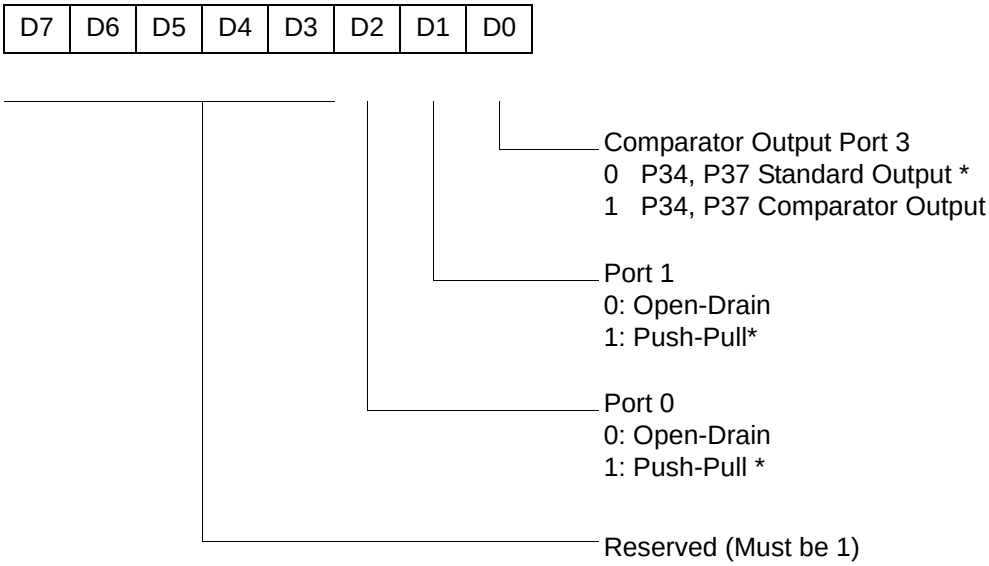
This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.



* CLR1 and $\overline{CLR2}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-

Figure 38. Resets and WDT

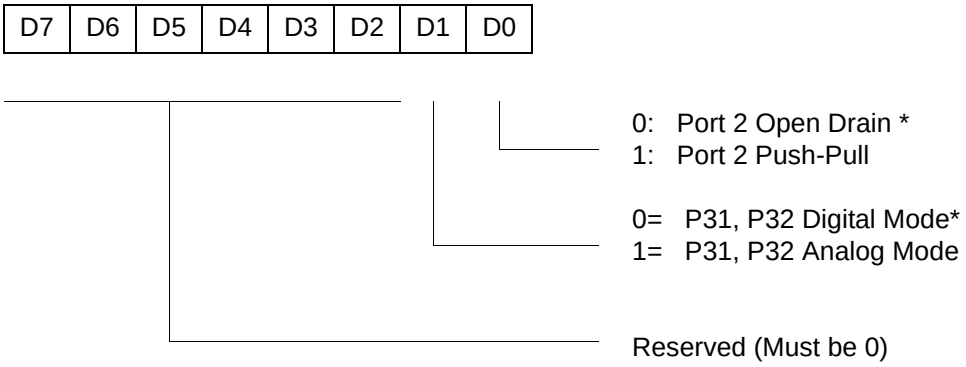
PCON(0F)00H



* Default setting after reset

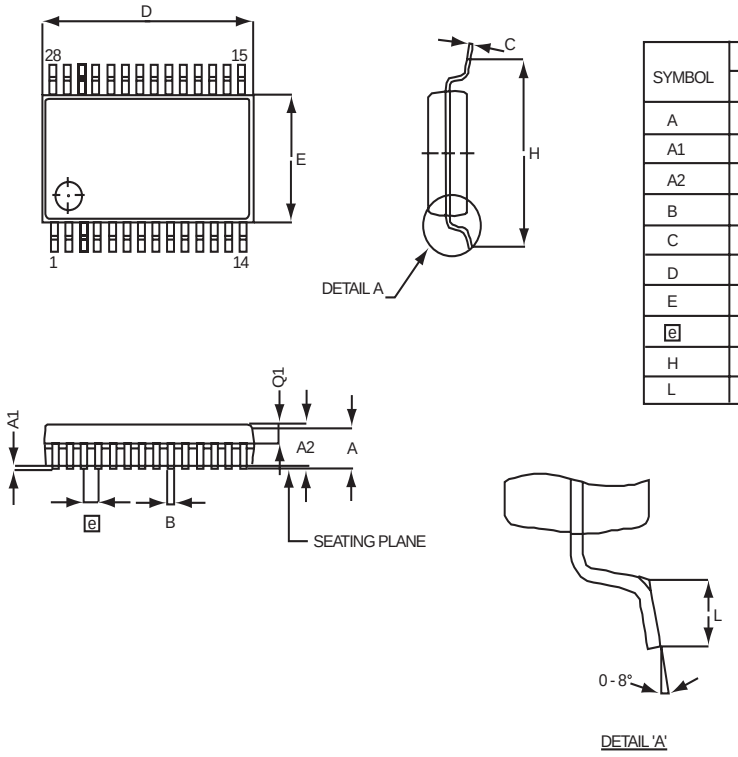
Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)

R247 P3M(F7H)



* Default setting after reset. Not reset with a Stop Mode recovery.

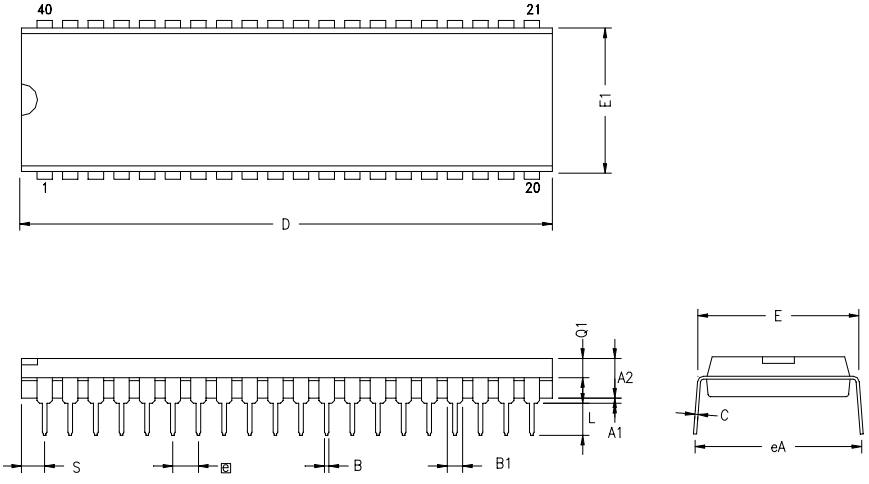
Figure 49. Port 3 Mode Register (F7H: Write Only)



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.86	1.99	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.78	0.066	0.068	0.070
B	0.25		0.38	0.010		0.015
C	0.09	–	0.20	0.004	0.006	0.008
D	10.07	10.20	10.33	0.397	0.402	0.407
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.63	0.75	0.95	0.025	0.030	0.037

CONTROLLING DIMENSIONS: MM
LEADS ARE COPLANAR WITHIN .004 INCHES.

Figure 65. 28-Pin SSOP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 66. 40-Pin PDIP Package Diagram

8KB Standard Temperature: 0° to +70°C			
Part Number	**Description**	**Part Number**	**Description**
ZGP323HSH4808C	48-pin SSOP 8K OTP	ZGP323HSS2808C	28-pin SOIC 8K OTP
ZGP323HSP4008C	40-pin PDIP 8K OTP	ZGP323HSH2008C	20-pin SSOP 8K OTP
ZGP323HSH2808C	28-pin SSOP 8K OTP	ZGP323HSP2008C	20-pin PDIP 8K OTP
ZGP323HSP2808C	28-pin PDIP 8K OTP	ZGP323HSS2008C	20-pin SOIC 8K OTP

8KB Extended Temperature: -40° to +105°C			
Part Number	**Description**	**Part Number**	**Description**
ZGP323HEH4808C	48-pin SSOP 8K OTP	ZGP323HES2808C	28-pin SOIC 8K OTP
ZGP323HEP4008C	40-pin PDIP 8K OTP	ZGP323HEH2008C	20-pin SSOP 8K OTP
ZGP323HEH2808C	28-pin SSOP 8K OTP	ZGP323HEP2008C	20-pin PDIP 8K OTP
ZGP323HEP2808C	28-pin PDIP 8K OTP	ZGP323HES2008C	20-pin SOIC 8K OTP

8KB Automotive Temperature: -40° to +125°C			
Part Number	**Description**	**Part Number**	**Description**
ZGP323HAH4808C	48-pin SSOP 8K OTP	ZGP323HAS2808C	28-pin SOIC 8K OTP
ZGP323HAP4008C	40-pin PDIP 8K OTP	ZGP323HAH2008C	20-pin SSOP 8K OTP
ZGP323HAH2808C	28-pin SSOP 8K OTP	ZGP323HAP2008C	20-pin PDIP 8K OTP
ZGP323HAP2808C	28-pin PDIP 8K OTP	ZGP323HAS2008C	20-pin SOIC 8K OTP
Replace C with G for Lead-Free Packaging			