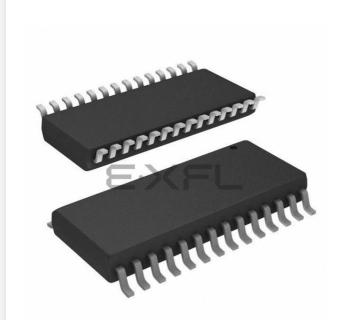
Zilog - ZGP323HSH2808C Datasheet





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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	·
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	·
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	·
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	·
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hsh2808c

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Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

Table 1.	Revision	History	of this	Document
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Date	Revision Level	Section	Description	Page #	
December 2004	02	Changed low power consumption, STOP and HALT mode current values, deleted mask option note, clarified temperature ranges in Tables 6 and 8 and 10. Added new Tables 9 and 10. Also added Characterization data to Table 11 and changed Program/Erase Endurance value in Table 12.		11,12,	
		Removed Preliminar	y designation	All	
March 2005	03	Minor change to Table 9 Electrical Characteristics. Added 20, 28 and 40- pin CDIP parts in the Ordering Section.			

ZGP323H Product Specification



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Absolute Maximum Ratings

Stresses greater than those listed in Table 8 might cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	125	° C	1
Storage temperature	-65	+150	° C	
Voltage on any pin with respect to V_{SS}	-0.3	7.0	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	7.0	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
Maximum current into V_{DD} or out of V_{SS}		75	mA	
Notos:				

Notes:

1. See Ordering Information.

2. This voltage applies to all pins except the following: V_{DD}, P32, P33 and RESET.

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 7).

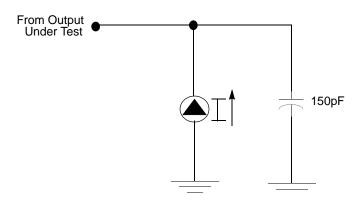


Figure 7. Test Load Diagram



Capacitance

Table 8 lists the capacitances.

Table 8. Capacitance

Parameter	Maximum			
Input capacitance	12pF			
Output capacitance	12pF			
I/O capacitance	12pF			
Note: $T_A = 25^{\circ}$ C, $V_{CC} = GND = 0$ V, f = 1.0 MHz, unmeasured pins returned to GND				

DC Characteristics

Table 9. GP323HS DC Characteristics

			T _A =0°C to	o +70°C				
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions N	lotes
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5 5	i
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	$I_{OH} = -0.5 \text{mA}$	
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	I _{OL} = 4.0mA	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{CC} 1.75	V		
Ι _{ΙL}	Input Leakage	2.0-5.5	-1		1	μA	V _{IN} = 0V, V _{CC} Pull-ups disabled	
R _{PU}	Pull-up Resistance	2.0V	225		675	KΩ	V _{IN} = 0V; Pullups selected by mask	
		3.6V	75		275	KΩ	option	
		5.0V	40		160	KΩ		



Table 11. GP323HA DC Characteristics

			T _A = -40°C	C to +12	5°C			
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} 0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	I _{OH} = -0.5mA	
V _{OH2}	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V _{CC} -0.8			V	I _{OH} = -7mA	
V _{OL1}	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$	
V _{OL2}	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I _{OL} = 10mA	
V _{OFFSET}	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V _{REF}	Comparator Reference Voltage	2.0-5.5	0		V _{DD} -1.75	V		
Ι _{ΙL}	Input Leakage	2.0-5.5	-1		1	μΑ	V _{IN} = 0V, V _{CC} Pull-ups disabled	
R _{PU}	Pull-up Resistance	2.0V	200		700	KΩ	V _{IN} = 0V; Pullups selected by mask	(
		3.6V	50		300	KΩ	option	
		5.0V	25		175	KΩ	_	
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0V, V_{CC}$	
I _{CC}	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1,2
	0	5.5V		10	15	mA	at 8.0 MHz	1, 2
I _{CC1}	Standby Current	2.0V		0.5	1.6	mA m A	$V_{IN} = 0V$, Clock at 8.0MHz	1, 2, 6
	(HALT Mode)	3.6V 5.5V		0.8 1.3	2.0 3.2	mA mA	$V_{IN} = 0V$, Clock at 8.0MHz $V_{IN} = 0V$, Clock at 8.0MHz	1, 2, 6 1, 2, 6
1	Standby Current (Stop	2.0V		1.6	15	μΑ	$V_{IN} = 0 V$, V_{CC} WDT not Running	3
I _{CC2}	Mode)	2.6V 3.6V		1.8	20	μA μA	$V_{IN} = 0 V, V_{CC} WDT not Running$ $V_{IN} = 0 V, V_{CC} WDT not Running$	3
	wode)	5.5V		1.9	25	μA	$V_{IN} = 0 V$, V_{CC} WDT not Running	3
		2.0V		5	30	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		3.6V		8	40	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		5.5V		15	60	μA	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage Detection			2.4		V	•	



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				–40°C to –40°C to	o +70°C (S) +105°C (E) +125°C (A) MHz			Watch-Dog Timer Mode Register
No	Symbol	Parameter	V _{CC}	Minimum	Maximum	Units	Notes	(D1, D0)
1	ТрС	Input Clock Period	2.0–5.5	121	DC	ns	1	
2	TrC,TfC	Clock Input Rise and Fall Times	2.0–5.5		25	ns	1	
3	TwC	Input Clock Width	2.0–5.5	37		ns	1	
4	TwTinL	Timer Input Low Width	2.0 5.5	100 70		ns	1	
5	TwTinH	Timer Input High Width	2.0–5.5	3ТрС			1	
6	TpTin	Timer Input Period	2.0–5.5	8TpC			1	
7	TrTin,TfTin	Timer Input Rise and Fall Timers	2.0–5.5		100	ns	1	
8	TwIL	Interrupt Request Low Time	2.0 5.5	100 70		ns	1, 2	
9	TwlH	Interrupt Request Input High Time	2.0–5.5	5TpC			1, 2	
10	Twsm	Stop-Mode Recovery Width	2.0–5.5	12		ns	3	
		Spec		5TpC			4	
11	Tost	Oscillator Start-Up Time	2.0–5.5		5TpC		4	
12	Twdt	Watch-Dog Timer Delay Time	2.0–5.5 2.0–5.5 2.0–5.5 2.0–5.5	5 10 20 80		ms ms ms ms		0, 0 0, 1 1, 0 1, 1
13	T _{POR}	Power-On Reset	2.0–5.5	2.5	10	ms		

Table 13. AC Characteristics

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0. 2. Interrupt request through Port 3 (P33–P31).

3. SMR – D5 = 1.

4. SMR - D5 = 0.







Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field Bit Position			Description		
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect		

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description	
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect	

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position		Description
T16_Data_HI	[7:0]	R/W	Data





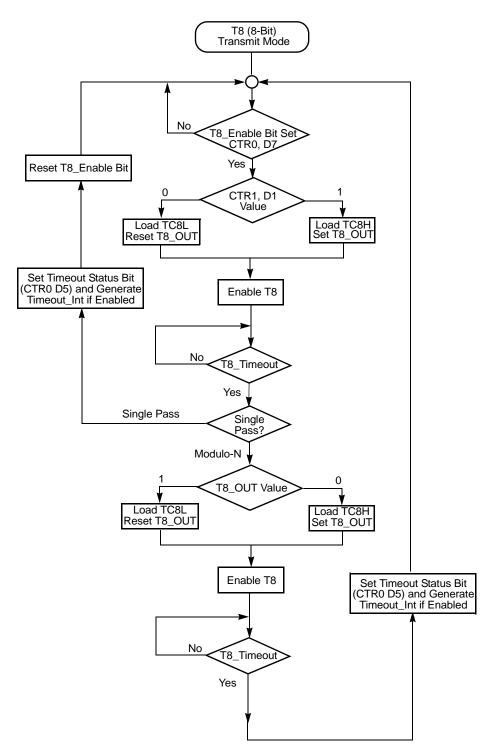


Figure 19. Transmit Mode Flowchart



Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.





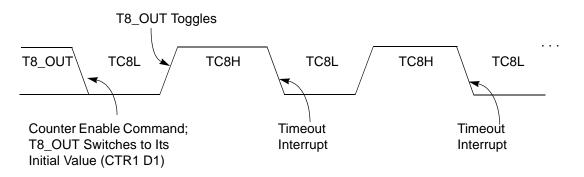


Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

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Caution: Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFFH. Transition from 0 to FFFFH is not a timeout condition.







Figure 27. T16_OUT in Modulo-N Mode

T16 DEMODULATION Mode

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).



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During PING-PONG Mode

The enable bits of T8 and T16 (CTR0, D7; CTR2, D7) are set and cleared alternately by hardware. The timeout bits (CTR0, D5; CTR2, D5) are set every time the counter/timers reach the terminal count.

Interrupts

The ZGP323H features six different interrupts (Table 19). The interrupts are maskable and prioritized (Figure 30). The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers (Table 19) and one for low voltage detection. The Interrupt Mask Register (globally or individually) enables or disables the six interrupt requests.

The source for IRQ is determined by bit 1 of the Port 3 mode register (P3M). When in digital mode, Pin P33 is the source. When in analog mode the output of the Stop mode recovery source logic is used as the source for the interrupt. See Figure 35, Stop Mode Recovery Source, on page 59.





Low-Voltage Detection Register—LVD(D)0Ch

Note: Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position			Description
LVD	76543			Reserved No Effect
	2	R	1 0*	HVD flag set HVD flag reset
	1-	R	1 0*	LVD flag set LVD flag reset
	0	R/W	1 0*	Enable VD Disable VD
*Default	after POR			

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Voltage Detection and Flags

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the V_{CC} voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the V_{CC} level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if V_{CC} is higher than V_{HVD}. The LVD flag (bit 1 of the LVD register) is set only if V_{CC} is lower than the V_{LVD}. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

Notes: If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.





CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0	
								Reserved No effect when written Always reads 11111 Sync Mode 0* Disable Sync Mode** 1 Enable Sync Mode T ₈ Enable R 0* T ₈ Disabled R 1 T ₈ Enabled W0 Stop T ₈
								W1 Enable T_8 T_{16} Enable $R 0^* T_{16}$ Disabled $R 1 T_{16}$ Enabled $W 0$ Stop T_{16} $W 1$ Enable T_{16}

* Default setting after reset. ** Default setting after reset. Not reset with a Stop Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)



R250 IRQ(FAH)





Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



* Default setting after reset

* * Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)



R252 Flags(FCH)

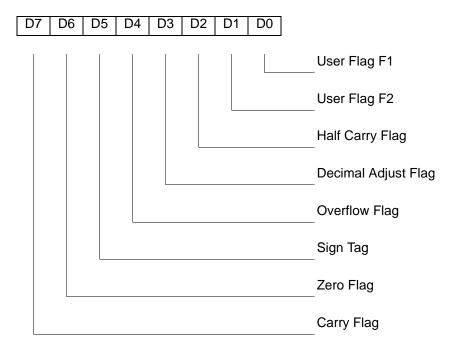
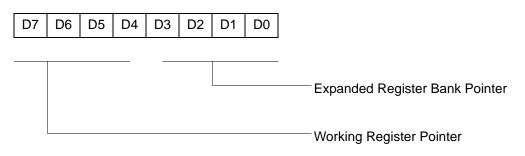


Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)

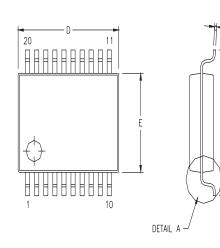


Default setting after reset = 0000 0000

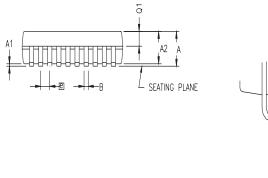
Figure 55. Register Pointer (FDH: Read/Write)







CVANDOL	MILLIMETER			INCH		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
В	0.25	0.30	0.38	0.010	0.012	0.015
С	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e		0.65 BSC		0.0256 BSC		
Н	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032



DETAIL A

Н

CONTROLLING DIMENSIONS : MM LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 61. 20-Pin SSOP Package Diagram





8KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4808C	48-pin SSOP 8K OTP	ZGP323HSS2808C	28-pin SOIC 8K OTP
ZGP323HSP4008C	40-pin PDIP 8K OTP	ZGP323HSH2008C	20-pin SSOP 8K OTP
ZGP323HSH2808C	28-pin SSOP 8K OTP	ZGP323HSP2008C	20-pin PDIP 8K OTP
ZGP323HSP2808C	28-pin PDIP 8K OTP	ZGP323HSS2008C	20-pin SOIC 8K OTP

8KB Extended Temperature: -40° to +105°C

-			
Part Number	Description	Part Number	Description
ZGP323HEH4808C	48-pin SSOP 8K OTP	ZGP323HES2808C	28-pin SOIC 8K OTP
ZGP323HEP4008C	40-pin PDIP 8K OTP	ZGP323HEH2008C	20-pin SSOP 8K OTP
ZGP323HEH2808C	28-pin SSOP 8K OTP	ZGP323HEP2008C	20-pin PDIP 8K OTP
ZGP323HEP2808C	28-pin PDIP 8K OTP	ZGP323HES2008C	20-pin SOIC 8K OTP

8KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323HAH4808C	48-pin SSOP 8K OTP	ZGP323HAS2808C	28-pin SOIC 8K OTP
ZGP323HAP4008C	40-pin PDIP 8K OTP	ZGP323HAH2008C	20-pin SSOP 8K OTP
ZGP323HAH2808C	28-pin SSOP 8K OTP	ZGP323HAP2008C	20-pin PDIP 8K OTP
ZGP323HAP2808C	28-pin PDIP 8K OTP	ZGP323HAS2008C	20-pin SOIC 8K OTP
Replace C with G for	r Lead-Free Packaging		

ZGP323H Z8[®] OTP Microcontroller with IR Timers



pin 4 Ε **EPROM** selectable options 64 expanded register file 26 expanded register file architecture 28 expanded register file control registers 71 flag 80 interrupt mask register 79 interrupt priority register 78 interrupt request register 79 port 0 and 1 mode register 77 port 2 configuration register 75 port 3 mode register 76 port configuration register 75 register pointer 80 stack pointer high register 81 stack pointer low register 81 stop-mode recovery register 73 stop-mode recovery register 2 74 T16 control register 69 T8 and T16 common control functions register 67 T8/T16 control register 70 TC8 control register 66 watch-dog timer register 75 F features standby modes 1 functional description counter/timer functional blocks 40 CTR(D)01h register 35 CTR0(D)00h register 33 CTR2(D)02h register 37 CTR3(D)03h register 39 expanded register file 26 expanded register file architecture 28 HI16(D)09h register 32 HI8(D)0Bh register 32 L08(D)0Ah register 32 L0I6(D)08h register 32

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