Zilog - ZGP323HSH2808G Datasheet





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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hsh2808g

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	ſ		$\overline{\mathbf{\nabla}}$				
NC		1	-		40	þ	NC
P25		2			39	Þ	P24
P26		3			38		P23
P27		4			37	Þ	P22
P04		5			36	Þ	P21
P05	q	6			35		P20
P06	Ц	7			34	Þ	P03
P14	С	8	40-Pir	۱	33	Þ	P13
P15		9			32		P12
P07	Ц	10	CDIP		31	Þ	VSS
VDD		11			30		P02
P16		12			39		P11
P17	С	13			28		P10
XTAL2		14			27		P01
XTAL1	С	15			26		P00
P31		16			25		Pref1/P30
P32	С	17			24		P36
P33	q	18			23		P37
P34	С	19			22	þ	P35
NC	Ц	20			21	Þ	RESET
	_						

Figure 5. 40-Pin PDIP/CDIP* Pin Configuration

Note: *Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.



40-Pin PDIP #	48-Pin SSOP #	Symbol
33	40	P13
8	9	P14
9	10	P15
12	15	P16
13	16	P17
35	42	P20
36	43	P21
37	44	P22
38	45	P23
39	46	P24
2	2	P25
3	3	P26
4	4	P27
16	19	P31
17	20	P32
18	21	P33
19	22	P34
22	26	P35
24	28	P36
23	27	P37
20	23	NC
40	47	NC
1	1	NC
21	25	RESET
15	18	XTAL1
14	17	XTAL2
11	12, 13	V _{DD}
31	24, 37, 38	V _{SS}
25	29	Pref1/P30
	48	NC
	6	NC
	14	NC
	30	NC
	36	NC

Table 6. 40- and 48-Pin Configuration (Continued)





Figure 9. Port 0 Configuration

Port 1 (P17–P10)

Port 1 (see Figure 10) Port 1 can be configured for standard port input or output mode. After POR, Port 1 is configured as an input port. The output drivers are either push-pull or open-drain and are controlled by bit D1 in the PCON register.



Note: The Port 1 direction is reset to its default state following an SMR.



CTR1(0D)01H" on page 35). Other edge detect and IRQ modes are described in Table 14.

Note: Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	Т8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Table 14. Port 3 Pin Function Summary

>

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.





Expanded Reg. Bank 0/Group 15" Register Pointer [7] [5] [4] [3] [2] [10] Working Register Group Pointer Bank Pointer FF FP Bank Pointer FF FP Bank Pointer FF FF FF FF Bank Pointer FF FF	Z8 [®] Standard Control Registers					Cond	itior	۱
Register Pointer FF SPL FE U <thu< th=""> <thu< th=""> U U</thu<></thu<>			Expanded Reg. Bank 0/Group 15	** D7 D6 D	5 D4	D3	D2[D1 D0
Register Pointer Image: Construction of the second of					1	ii		
Register Pointer T D								
Register Pointer U <			FD RP		0	0	0	
7 6 5 4 3 2 1 0		Register Pointer	FC FLAGS					
Working Register Group Pointer Expanded Register Bank Pointer FA IRQ 0 <td< td=""><td>7</td><td>7 6 5 4 3 2 1 0</td><td>FB IMB</td><td></td><td></td><td></td><td></td><td></td></td<>	7	7 6 5 4 3 2 1 0	FB IMB					
Working Register Expanded Register F3 F3 <td></td> <td></td> <td>FA IBO</td> <td></td> <td>0</td> <td>0</td> <td>0</td> <td></td>			FA IBO		0	0	0	
Ordop Pollies Dirth Antes PB PD1M 1 0 <t< td=""><td>Working Regist</td><td>ter Expanded Regist</td><td>er F9 IPR</td><td></td><td></td><td></td><td></td><td></td></t<>	Working Regist	ter Expanded Regist	er F9 IPR					
F7 P3M 0	Group Pointer	Dank i ontei	F8 P01M	1 1 0	0	1	1	1 1
F6 P2M 1			+ F7 P3M		0	0	0	0 0
F5 Reserved I			F6 P2M	1 1 1	1	1	1	1 1
F4 Reserved F3 Reserved F3 Reserved F4 Reserved F5 Reserved F6 F6 F6 F7 F7 F8 F8 F8 F7 F8 F8 F8 F9 F8 <td></td> <td></td> <td>F5 Reserved</td> <td></td> <td></td> <td>$\frac{1}{1}$</td> <td>ii l</td> <td></td>			F5 Reserved			$\frac{1}{1}$	ii l	
Fig Reserved U			F4 Reserved			11	U	
File (Bank 0)** File (Bank 0)** File (Bank 0)** File Reserved U			F3 Reserved		U U	U	U	
Findersterning (bank 0)** Findersterning (bank 0)**			F2 Reserved		U U	U	Ŭ	
F0 Reserved U	FF	Register File (Bank 0)	F1 Reserved		U U	Ŭ	U	υυ
Image: Second State Sta	Fo		F0 Reserved		U U	Ŭ	U	
Figure 1 Expanded Reg. Bank F/Group 0** (F) 0F WD 1MR (F) 0F WD 1MR (F) 0F Reserved (F) 0F Reserved (F) 0R Reserved						1-1	~	
Image: constraint of the second state stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the stop mode Recovery Image: constraint of the stop-Mode Recovery Image: constraint of the			Expanded Reg. Bank F/Group 0*	*				
(F) 0E Reserved 0			(F) 0F WDTMR	U U O	0	1	1	0 1
F) OD SMR2 0			(F) 0E Reserved			Π		
7F F			* (F) 0D SMR2	0 0 0	0	0	0	0 0
7F (F) 0B SMR U 0 1 0 0 0 U 0 (F) 0B Reserved (F) 0B Reserved (F) 0B Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved (F) 0F Reserved </td <td>_</td> <td></td> <td>(F) 0C Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	_		(F) 0C Reserved					
(F) 0A Reserved (F) 09 Reserved (F) 06 Reserved (F) 06 Reserved (F) 07 Reserved (F) 06 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 09 Reserved (F) 07 Reserved (F) 00 Reserved (F) 00 Reserved (D) 00 C LVD (D) 0 0 0 0 0 0 0 0	7F	· ↓	↑ (F) 0B SMR	U 0 1	0	0	0	U 0
(F) 09 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved		_	(F) 0A Reserved			Π		
(F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 07 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 08 Reserved (F) 07 Reserved (F) 00 PCON (F) 01 Reserved (O) 01 P1 U (O) 00 P0 U U = Unknown (D) 00 C T16L * 18 not reset with a Stop-Mode Recovery * 111 Bits 5,4,3,2 not reset with a Stop-Mode Recovery * 111 Bits 5,4,3,2,2 not reset with a			(F) 09 Reserved					
0F (F) 07 Reserved (F) 06 Reserved (F) 06 Reserved (F) 05 Reserved (F) 07 Reserved (F) 04 Reserved (F) 07 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 01 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 04 Reserved (F) 04 Reserved			(F) 08 Reserved					
0F (F) 06 Reserved (F) 05 Reserved (F) 04 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 02 Reserved (F) 04 Reserved (F) 03 Reserved (F) 04 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 03 P3 0 (F) 01 Reserved (F) 00 PCON (F) 01 Reserved (F) 01 Reserved (F) 01 Reserved (F) 02 Reserved (F) 01 Reserved (F) 00 PCON (F) 01 Reserved (F) 01 P1 (F) 01 Reserved (D) 02 P2 (F) 00 PCON (F) 03 B Hil8 (F) 00 0 0 0 0 0 0 0 (D) 04 LO8 (F) 00 0 0 0 0 0 (F) 03 B LO16 (F) 00 0 0 0 0 0 (F) 04 C LD8 (F) 00 0 0 0 0 0 (D) 05 TC8H (F) 00 0 0 0 0 0 (F) 03 C TR3 (F) 0 0 0 0 0 0 (F) 04 TC8L (F) 0 0 0 0 0 0 (F) 04 C C R2<			(F) 07 Reserved					
0F 0F <td< td=""><td></td><td></td><td>(F) 06 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 06 Reserved					
0F 00 <td< td=""><td></td><td></td><td>(F) 05 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 05 Reserved					
00 Image: constraint of the set with a Stop-Mode Recovery 1 <td>0F</td> <td><u> </u>₩/</td> <td>(F) 04 Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	0F	<u> </u> ₩/	(F) 04 Reserved					
Expanded Reg. Bank 0/Group (0) (F) 02 Reserved 1	00		(F) 03 Reserved					
Expanded Reg. Bank 0/Group (0) (0) 03 P3 0 (0) 02 P2 U (0) 01 P1 U (0) 01 P1 U (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** Di 03 CTR3 0 ** (D) 04 TC8L 0 0 0 ** (D) 03 CTR3 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 04 TC8L 0 0 0 ** (D) 02 CTR2 0 ** (D) 01 CTR1 0 ** (D) 00 CTR0 0		\backslash	(F) 02 Reserved					
Expanded Reg. Bank 0/Group (0) (0) 03 P3 0 U (0) 02 P2 U * (0) 01 P1 U (0) 00 P0 U (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ↑ Is not reset with a Stop-Mode Recovery ** His 5 Is not reset with a Stop-Mode Recovery ** (D) 04 TC8L 0 <			(F) 01 Reserved					
(0) 03 P3 0 U (0) 02 P2 U * (0) 01 P1 U (0) 00 P0 U * (0) 00 P0 U U = Unknown * Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ^* (D) 05 TC8H 0	Expa	anded Reg. Bank 0/Group (0)	(F) 00 PCON	1 1 1	1	1	1	1 0
(0) 03 P3 0			Expanded Reg. Bank D/Group 0					
(b) 02 P2 U * (0) 01 P1 U (0) 00 P0 U U = Unknown * * All addresses are in hexadecimal * ↑ Bit 5 Is not reset with a Stop-Mode Recovery ** (D) 04 ** (D) 05 ** (D) 06 ** (D) 07 ** (D) 08 ** (D) 08 ** (D) 07 ** (D) 08 ** (D) 07 ** (D) 06 ** (D) 06 ** (D) 07 ** (D) 06 ** (D) 07 ** (D) 08 ** (D) 08 ** (D) 04 ** (D) 05 ** (D) 04 ** (D) 03 ** (D) 02 ** (D) 01 ** (D) 01 ** (D) 01 ** (D) 01 ** (D) 02 ** (D) 01 (D) 0	(0) 03 P3	U U		UUI	υ	U	U	υn
* (0) 01 P1 U (0) 01 P1 U (0) 00 P0 U * (D) 00 A LO8 0<	(0) 02 P2	U	* (D) 0B HI8	0 0 0	0	0	0	0 0
(b) 01 1 1 0	* (0) 01 P1	U	* (D) 0A 08	0 0 0	0	0	0	0 0
(0) 00 P0 U U = Unknown (D) 08 LO16 0	(0) 011 1	<u> </u>	* (D) 09 HI16	0 0 0	0	0	0	0 0
U = Unknown * (D) 07 TC16H 0 <td>(0) 00 P0</td> <td>U</td> <td>* (D) 08 LO16</td> <td>0 0 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td>	(0) 00 P0	U	* (D) 08 LO16	0 0 0	0	0	0	0 0
* Is not reset with a Stop-Mode Recovery ** All addresses are in hexadecimal ^* All addresses are in hexadecimal ^* Is not reset with a Stop-Mode Recovery, except Bit 0 ^* Bit 5 Is not reset with a Stop-Mode Recovery ^* Bit 5 Is not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Bit 5 Js not reset with a Stop-Mode Recovery ^* Diss 5,4,3,2 not reset with a Stop-Mode Recovery ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery ^* CD 00 CTR1 0 0 ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery ^* CD 00 CTR0 ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery			* (D) 07 TC16H	0 0 0	0	0	0	0 0
*** All addresses are in hexadecimal * (D) 05 TC8H 0 <t< td=""><td>* Is not reset with a Ston-Mor</td><td>de Recoverv</td><td>* (D) 06 TC16L</td><td>0 0 0</td><td>0</td><td>0</td><td>0</td><td>0 0</td></t<>	* Is not reset with a Ston-Mor	de Recoverv	* (D) 06 TC16L	0 0 0	0	0	0	0 0
⁺ Is not reset with a Stop-Mode Recovery, except Bit 0 ⁺ 1bit 5 Is not reset with a Stop-Mode Recovery ⁺ (D) 04 TC8L ⁻ 0 0 0 0 0 0 0 0 0 0 0 ⁺ (D) 03 CTR3 ⁻ 0 0 0 0 1 1 1 1 1 ⁺ 1 ⁺ (D) 02 CTR2 ⁻ 0 0 0 0 0 0 0 0 0 ⁻ 1 1 1 1 ⁺	** All addresses are in beyade	ecimal	* (D) 05 TC8H	0 0 0	0	0	0	0 0
	↑ Is not reset with a Stop-Mo	de Recovery, except Bit 0	* (D) 04 TC8L	0 0 0	0	0	0	0 0
[↑] ↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery [↑] ↑↑↑ [↑] ↑↑↑ [↑] ↑↑↑ [↑] ↑↑↑↑ [↑] ↑↑↑ [↑] ↑↑ [↑] ↑ [↑]	↑↑ Bit 5 Is not reset with a Sto	p-Mode Recovery	1↑ (D) 03 CTR3	0 0 0	1	1	1	1 1
^{↑↑↑↑} Bits 5 and 4 not reset with a Stop-Mode Recovery ^{↑↑↑↑↑} (D) 01 CTR1 (D) 01 CTR1 (D) 0 0 0 0 0 0 0 0 (D) 01 CTR1 (D) 00 CTR0 (D)	↑↑↑ Bits 5,4,3.2 not reset with	a Stop-Mode Recoverv	↑↑↑ (D) 02 CTR2	0 0 0	0	0	0	0 0
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery ↑↑↑↑↑↓ (D) 00 CTR0 0 0 0 0 0 0 0 0 0 0	↑↑↑↑ Bits 5 and 4 not reset with	a Stop-Mode Recovery	↑↑↑↑ (D) 01 CTR1	0 0 0	0	0	0	0 0
	↑↑↑↑↑ Bits 5,4,3,2,1 not reset wit	th a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	0 0 0	0	0	0	0 0

Figure 15. Expanded Register File Architecture



The counter/timers are mapped into ERF group D. Access is easily performed using the following:

LD	RP, #0Dh	;	Select ERF D
for access to bank D			
		;	(working
register group 0)			
LD	R0,#xx	;	load CTR0
LD	1, #xx	;	load CTR1
LD	R1, 2	;	CTR2→CTR1
LD	RP, #0Dh	;	Select ERF D
for access to bank D			
		;	(working
register group 0)			
LD	RP, #7Dh	;	Select
expanded register bank	D and working	;	register
group 7 of bank 0 for a	ccess.		
LD	71h, 2		
; CTRL2 \rightarrow register 71h			
LD	R1, 2		
; CTRL2 \rightarrow register 71h			

Register File

>

The register file (bank 0) consists of 4 I/O port registers, 237 general-purpose registers, 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), and two expanded registers groups in Banks D (see Table 15) and F. Instructions can access registers directly or indirectly through an 8-bit address field, thereby allowing a short, 4-bit register address to use the Register Pointer (Figure 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.





Timers

T8_Capture_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T8_Capture_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field Bit Position			Description
T8_Capture_L0	[7:0]	R/W	Captured Data - No Effect

T16_Capture_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	[7:0]	R/W	Captured Data - No Effect

T16_Capture_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/ Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field Bit Position			Description
T16_Data_HI	[7:0]	R/W	Data



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Table 15.CTR0(D)00H Counter/Timer8 Control Register (Continued)

Field	Bit Position		Value	Description
Counter_INT_Mask	1-	R/W	0** 1	Disable Time-Out Interrupt Enable Time-Out Interrupt
P34_Out	0	R/W	0* 1	P34 as Port Output T8 Output on P34

Note:

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

T8 Enable

This field enables T8 when set (written) to 1.

Single/Modulo-N

When set to 0 (Modulo-N), the counter reloads the initial value when the terminal count is reached. When set to 1 (single-pass), the counter stops when the terminal count is reached.

Timeout

This bit is set when T8 times out (terminal count reached). To reset this bit, write a 1 to its location.



Caution: Writing a 1 is the only way to reset the Terminal Count status condition. Reset this bit before using/enabling the counter/timers.

The first clock of T8 might not have complete clock width and can occur any time when enabled.

Note: Take care when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers.

T8 Clock

This bit defines the frequency of the input signal to T8.



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When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.



Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising, Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T _{IN}	4,5	External (P31), Rising, Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	Т8	8,9	Internal
IRQ5	LVD	10,11	Internal

Table 19. Interrupt Types, Sources, and Vectors

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All ZGP323H interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 20.

IRQ		Interrupt Edge		
D7	D6	IRQ2 (P31)	IRQ0 (P32)	
0	0	F	F	
0	1	F	R	
1	0	R	F	
1	1	R/F	R/F	
Note: F = Falling Edge; R = Rising Edge				

Table 20. IRQ Register



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SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset

* * Default setting after Reset and Stop Mode Recovery

* * * At the XOR gate input

* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.







Figure 35. Stop Mode Recovery Source



Table 22. Stop Mode Recovery Source

SMR:432			Operation	
D4	D3	D2	Description of Action	
0	0	0	POR and/or external reset recovery	
0	0	1	Reserved	
0	1	0	P31 transition	
0	1	1	P32 transition	
1	0	0	P33 transition	
1	0	1	P27 transition	
1	1	0	Logical NOR of P20 through P23	
1	1	1	Logical NOR of P20 through P27	

Note: Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 61 for other recover sources.

Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the T_{POR} delay after Stop Mode Recovery. The default configuration of this bit is 1. If the "fast" wake up is selected, the Stop Mode Recovery source must be kept active for at least 5 TpC.

Note: This bit must be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.

Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).







Notes: Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.



LVD(0D)0CH



* Default setting after reset.

Figure 43. Voltage Detection Register

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.



MILLIMETER

MAX

2.65

0.30

2.44

0.46

0.30

12.95

7.60

10.65

0.40

1.00

1.07

1.27 BSC



INCH

мах

.104

.012

.096

.018

.012

.510

.299

.419

.016

.039

.042

.050 BSC

MIN

.094

.004

.088

.014

.009

.496

.291

.394

.012

.024

.038



Figure 60. 20-Pin SOIC Package Diagram

PS023803-0305



Ordering Information

32KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4832C	48-pin SSOP 32K OTP	ZGP323HSS2832C	28-pin SOIC 32K OTP
ZGP323HSP4032C	40-pin PDIP 32K OTP	ZGP323HSH2032C	20-pin SSOP 32K OTP
ZGP323HSK2832E	28-pin CDIP 32K OTP	ZGP323HSK2032E	20-pin CDIP 32K OTP
ZGP323HSK4032E	40-pin CDIP 32K OTP	ZGP323HSP2032C	20-pin PDIP 32K OTP
ZGP323HSH2832C	28-pin SSOP 32K OTP	ZGP323HSS2032C	20-pin SOIC 32K OTP
ZGP323HSP2832C	28-pin PDIP 32K OTP		

32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4832C	48-pin SSOP 32K OTP	ZGP323HES2832C	28-pin SOIC 32K OTP
ZGP323HEP4032C	40-pin PDIP 32K OTP	ZGP323HEH2032C	20-pin SSOP 32K OTP
ZGP323HEH2832C	28-pin SSOP 32K OTP	ZGP323HEP2032C	20-pin PDIP 32K OTP
ZGP323HEP2832C	28-pin PDIP 32K OTP	ZGP323HES2032C	20-pin SOIC 32K OTP

32KB Automotive Temperature: -40° to +125°C				
Part Number	Description	Part Number	Description	
ZGP323HAH4832C	48-pin SSOP 32K OTP	ZGP323HAS2832C	28-pin SOIC 32K OTP	
ZGP323HAP4032C	40-pin PDIP 32K OTP	ZGP323HAH2032C	20-pin SSOP 32K OTP	
ZGP323HAH2832C	28-pin SSOP 32K OTP	ZGP323HAP2032C	20-pin PDIP 32K OTP	
ZGP323HAP2832C	28-pin PDIP 32K OTP	ZGP323HAS2032C	20-pin SOIC 32K OTP	
Replace C with G fo	r Lead-Free Packaging			

ZGP323H Z8[®] OTP Microcontroller with IR Timers



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X XTAL1 5 XTAL1 pin function 18 XTAL2 5 XTAL2 pin function 18