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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | HLVD, POR, WDT |
| Number of I/O | 32 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-BSSOP (0.295", 7.50mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zgp323hsh4816c |

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**ZiLOG Worldwide Headquarters**
532 Race Street
San Jose, CA  95126-3432
Telephone: 408.558.8500
Fax: 408.558.8300
www.zilog.com



## Document Disclaimer

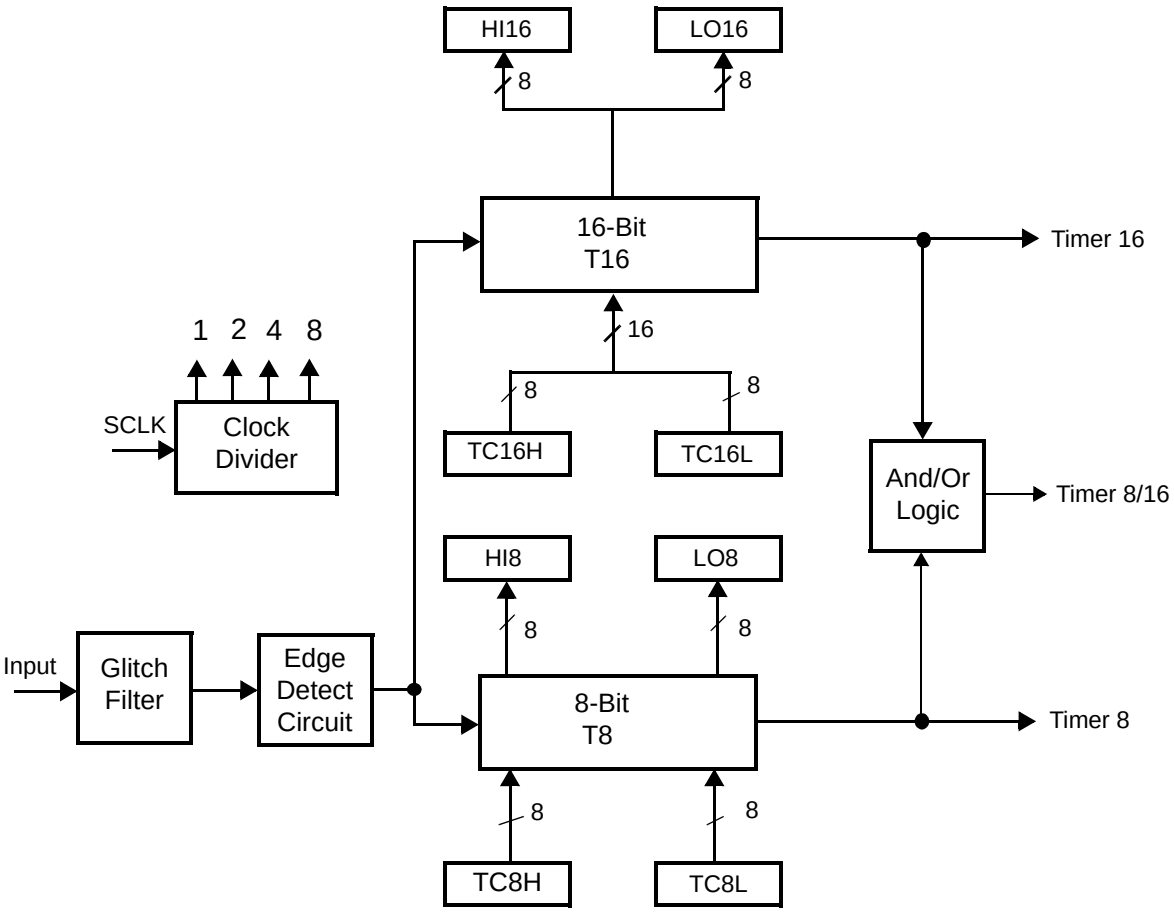



**Figure 2. Counter/Timers Diagram**

## Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.

CTR1(0D)01H" on page 35). Other edge detect and IRQ modes are described in Table 14.

**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

**Table 14. Port 3 Pin Function Summary**

| Pin | I/O | Counter/Timers | Comparator | Interrupt |
|---|---|---|---|---|
| Pref1/P30 | IN | | RF1 | |
| P31 | IN | IN | AN1 | IRQ2 |
| P32 | IN | | AN2 | IRQ0 |
| P33 | IN | | RF2 | IRQ1 |
| P34 | OUT | T8 | AO1 | |
| P35 | OUT | T16 | | |
| P36 | OUT | T8/16 | | |
| P37 | OUT | | AO2 | |
| P20 | I/O | IN | | |

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

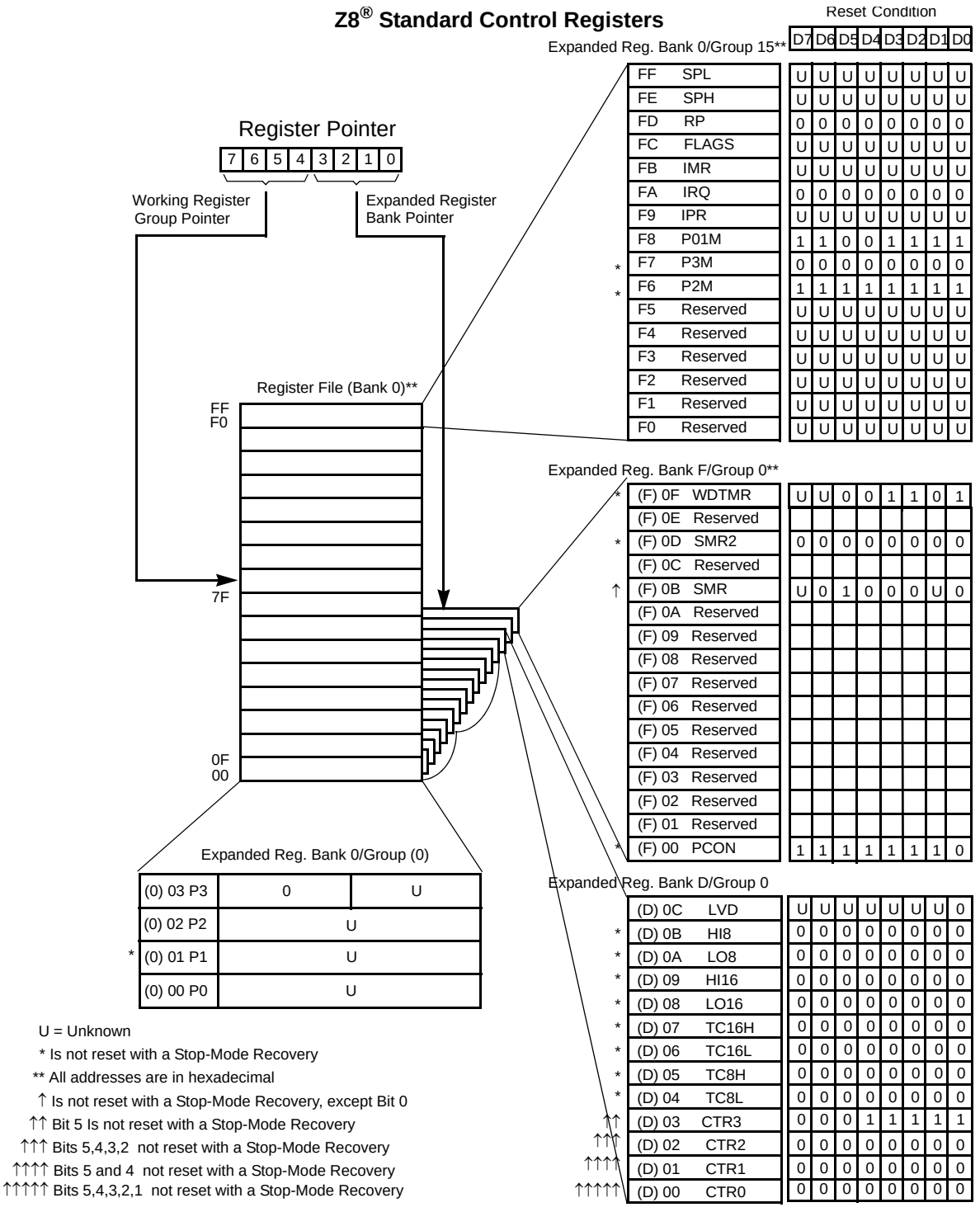



**Figure 15. Expanded Register File Architecture**

**Table 16. CTR1(0D)01H T8 and T16 Common Functions (Continued)**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Transmit_Submode/ Glitch_Filter | ----32-- | R/W | | Transmit Mode |
| | | | 00* | Normal Operation |
| | | | 01 | Ping-Pong Mode |
| | | | 10 | T16_Out = 0 |
| | | | 11 | T16_Out = 1 |
| | | | | Demodulation Mode |
| | | | 00* | No Filter |
| | | | 01 | 4 SCLK Cycle |
| | | | 10 | 8 SCLK Cycle |
| | | | 11 | Reserved |
| Initial_T8_Out/ Rising Edge | ------1- | | | Transmit Mode |
| | | R/W | 0* | T8_OUT is 0 Initially |
| | | | 1 | T8_OUT is 1 Initially |
| | | | | Demodulation Mode |
| | | R | 0* | No Rising Edge |
| | | | 1 | Rising Edge Detected |
| | | W | 0 | No Effect |
| | | | 1 | Reset Flag to 0 |
| Initial_T16_Out/ Falling_Edge | -------0 | | | Transmit Mode |
| | | R/W | 0* | T16_OUT is 0 Initially |
| | | | 1 | T16_OUT is 1 Initially |
| | | | | Demodulation Mode |
| | | R | 0* | No Falling Edge |
| | | | 1 | Falling Edge Detected |
| | | W | 0 | No Effect |
| | | | 1 | Reset Flag to 0 |

**Note:**
*Default at Power-On Reset
*Default at Power-On Reset. Not reset with Stop Mode recovery.

### Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

### P36_Out/Demodulator_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

### T8/T16_Logic/Edge _Detect

In TRANSMIT Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In DEMODULATION Mode, this field defines which edge should be detected by the edge detector.

### Transmit_Submode/Glitch Filter

In Transmit Mode, this field defines whether T8 and T16 are in the PING-PONG mode or in independent normal operation mode. Setting this field to “NORMAL OPERATION Mode” terminates the “PING-PONG Mode” operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 forces T16 to output a 1.

In DEMODULATION Mode, this field defines the width of the glitch that must be filtered out.

### Initial_T8_Out/Rising_Edge

In TRANSMIT Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When the counter is not enabled and this bit is set to 1 or 0, T8_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In DEMODULATION Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset the mode, a 1 should be written to this location.

### Initial_T16 Out/Falling _Edge

In TRANSMIT Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or PING-PONG Mode (CTR1, D3; D2). When the counter is not enabled and this bit is set, T16_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D0.

In DEMODULATION Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

**Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/16_OUT.

### CTR2 Counter/Timer 16 Control Register—CTR2(D)02H

Table 17 lists and briefly describes the fields for this register.

In Demodulation Mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode on page 47.

### Time_Out

This bit is set when T16 times out (terminal count reached). To reset the bit, write a 1 to this location.

### T16_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

### Capture_INT_Mask

This bit is set to allow an interrupt when data is captured into LO16 and HI16.

### Counter_INT_Mask

Set this bit to allow an interrupt when T16 times out.

### P35_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

### CTR3 T8/T16 Control Register—CTR3(D)03H

Table 18 lists and briefly describes the fields for this register. This register allows the $T_8$ and $T_{16}$ counters to be synchronized.

**Table 18. CTR3 (D)03H: T8/T16 Control Register**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| $T_{16}$ Enable | 7------- | R | 0* | Counter Disabled |
| | | R | 1 | Counter Enabled |
| | | W | 0 | Stop Counter |
| | | W | 1 | Enable Counter |
| $T_8$ Enable | -6------ | R | 0* | Counter Disabled |
| | | R | 1 | Counter Enabled |
| | | W | 0 | Stop Counter |
| | | W | 1 | Enable Counter |
| Sync Mode | --5----- | R/W | 0** | Disable Sync Mode |
| | | | 1 | Enable Sync Mode |

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFH (see Figure 23 and Figure 24).

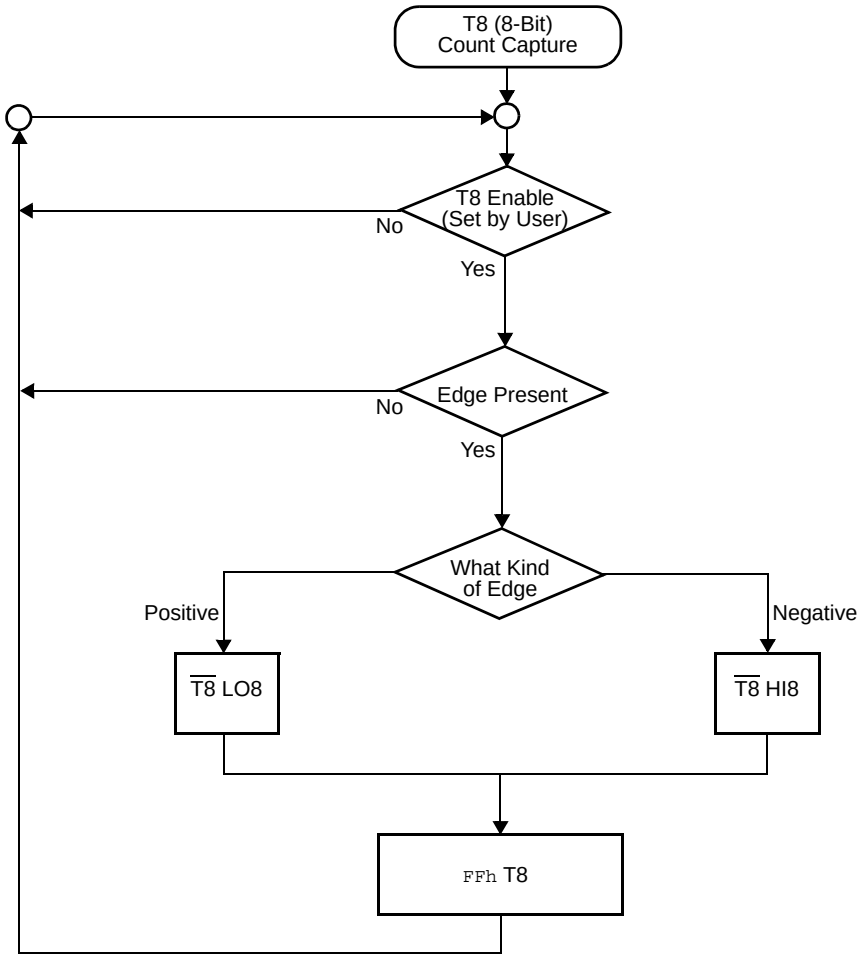



**Figure 23. Demodulation Mode Count Capture Flowchart**

**Table 19. Interrupt Types, Sources, and Vectors**

| Name | Source | Vector Location | Comments |
|---|---|---|---|
| IRQ0 | P32 | 0,1 | External (P32), Rising, Falling Edge Triggered |
| IRQ1 | P33 | 2,3 | External (P33), Falling Edge Triggered |
| IRQ2 | P31, $T_{IN}$ | 4,5 | External (P31), Rising, Falling Edge Triggered |
| IRQ3 | T16 | 6,7 | Internal |
| IRQ4 | T8 | 8,9 | Internal |
| IRQ5 | LVD | 10,11 | Internal |

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle activates when an interrupt request is granted. As a result, all subsequent interrupts are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All ZGP323H interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered. These interrupts are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 20.

**Table 20. IRQ Register**

| IRQ | | Interrupt Edge | |
|---|---|---|---|
| **D7** | **D6** | **IRQ2 (P31)** | **IRQ0 (P32)** |
| 0 | 0 | F | F |
| 0 | 1 | F | R |
| 1 | 0 | R | F |
| 1 | 1 | R/F | R/F |

**Note:** F = Falling Edge; R = Rising Edge

### Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

### Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

### Low-Voltage Detection Register—LVD(D)0Ch

**Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

| Field | Bit Position | | | Description |
|---|---|---|---|---|
| LVD | 76543--- | | | Reserved<br>No Effect |
| | -----2-- | R | 1<br>0* | HVD flag set<br>HVD flag reset |
| | ------1- | R | 1<br>0* | LVD flag set<br>LVD flag reset |
| | -------0 | R/W | 1<br>0* | Enable VD<br>Disable VD |

***Default after POR

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

### Voltage Detection and Flags

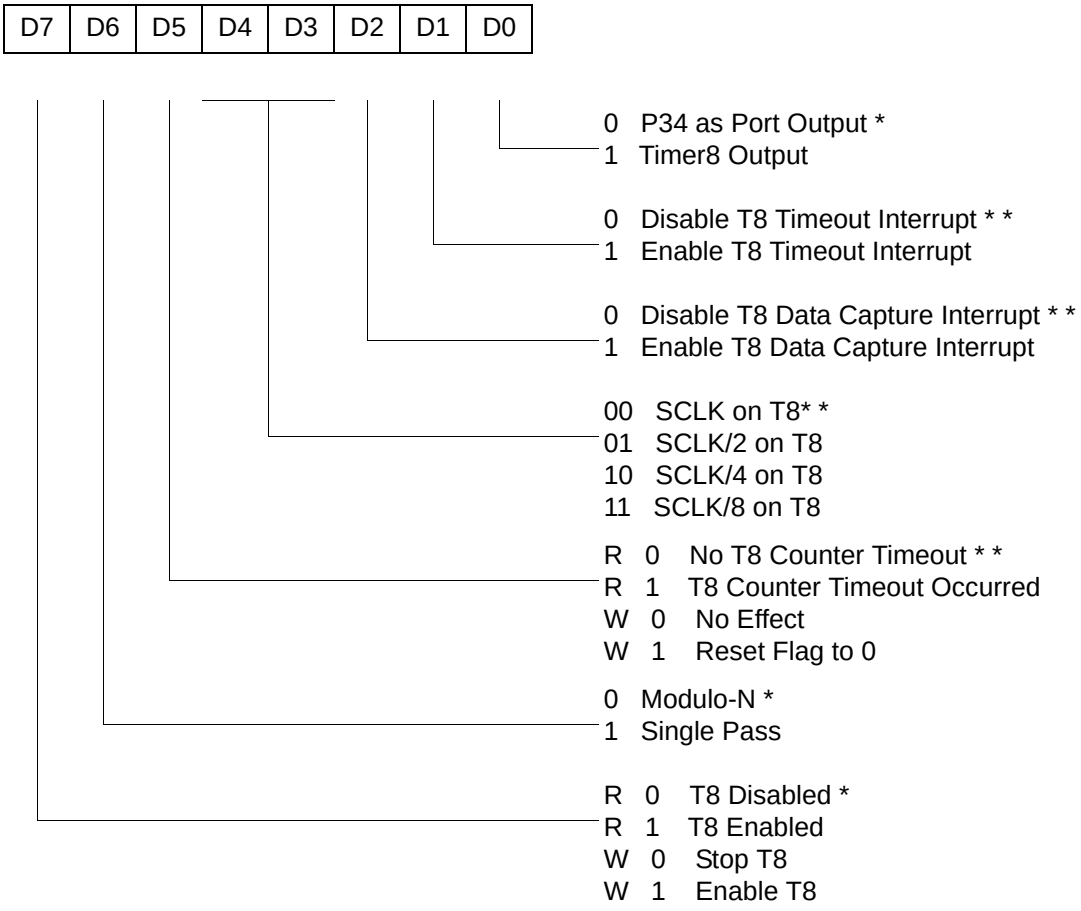
The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the $V_{CC}$ voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the the $V_{CC}$ level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if $V_{CC}$ is higher than $V_{HVD.}$ The LVD flag (bit 1 of the LVD register) is set only if $V_{CC}$ is lower than the $V_{LVD}$. When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

**Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

# Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H




* Default setting after reset.
* * Default setting after Reset.. Not reset with a Stop-Mode recovery.

**Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)**

CTR2(0D)02H

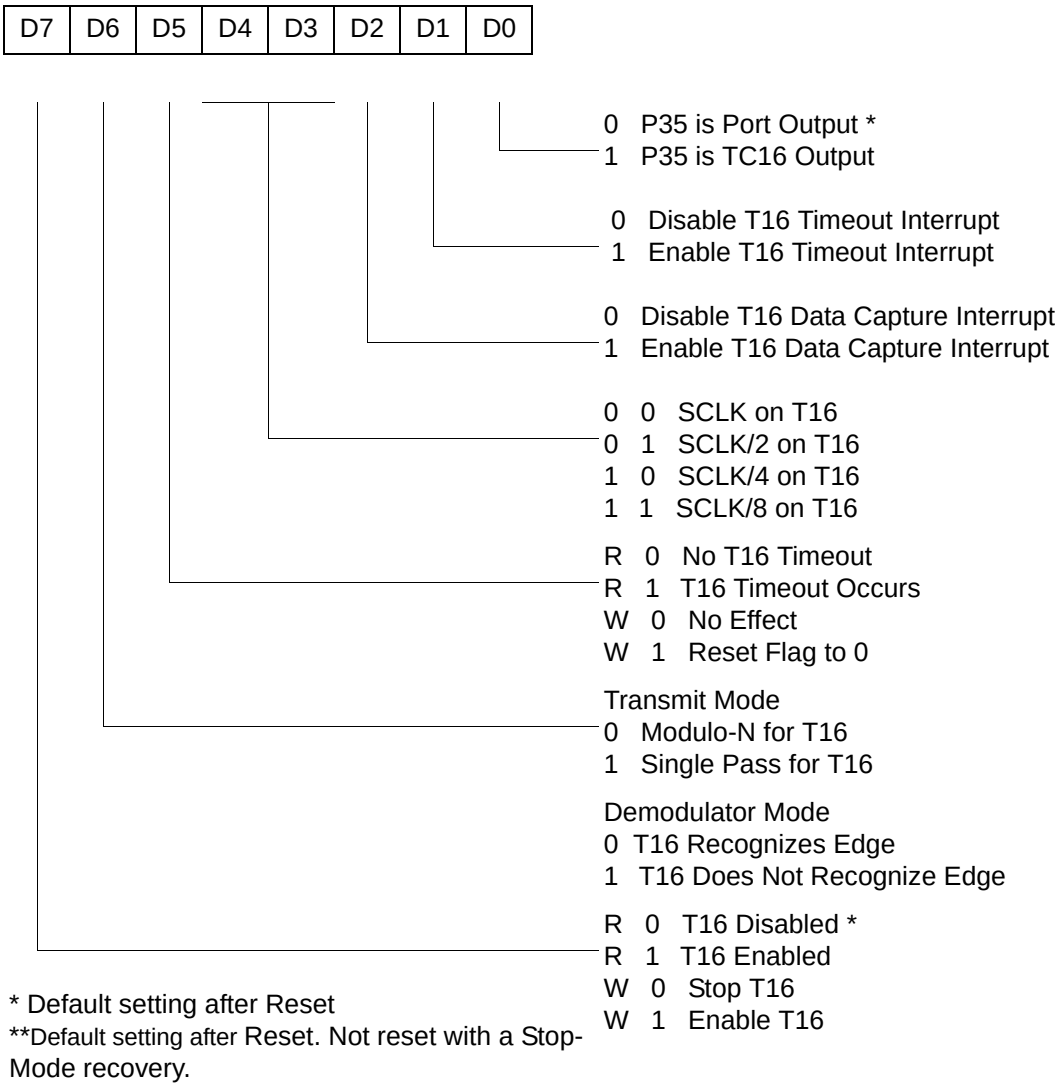



**Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)**

R254 SPH(FEH)

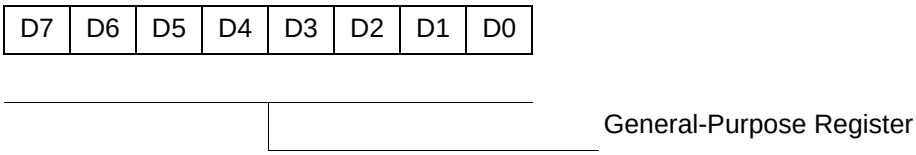



**Figure 56. Stack Pointer High (FEH: Read/Write)**

R255 SPL(FFH)

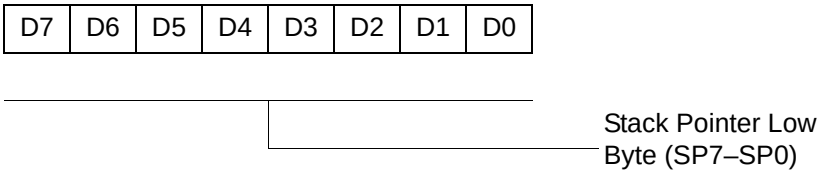
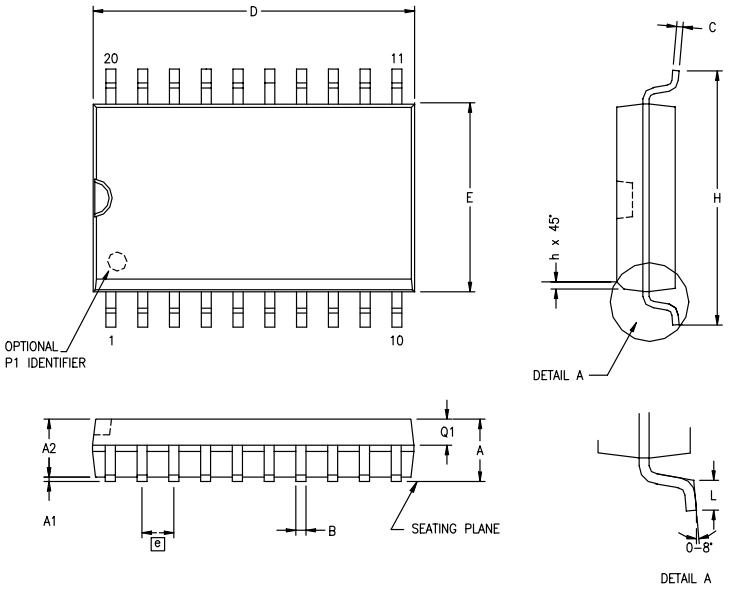



**Figure 57. Stack Pointer Low (FFH: Read/Write)**

# Package Information

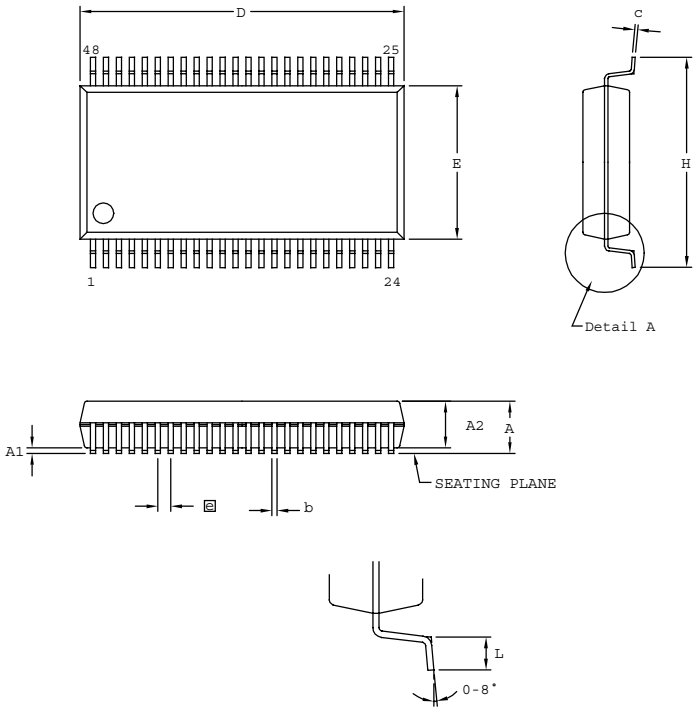
Package information for all versions of ZGP323H is depicted in Figures 59 through Figure 68.




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.40 | 2.65 | .094 | .104 |
| A1 | 0.10 | 0.30 | .004 | .012 |
| A2 | 2.24 | 2.44 | .088 | .096 |
| B | 0.36 | 0.46 | .014 | .018 |
| C | 0.23 | 0.30 | .009 | .012 |
| D | 12.60 | 12.95 | **.496** | .510 |
| E | 7.40 | 7.60 | .291 | .299 |
| e | 1.27 BSC | | .050 BSC | |
| H | 10.00 | 10.65 | .394 | .419 |
| h | 0.30 | 0.40 | .012 | .016 |
| L | 0.60 | 1.00 | .024 | .039 |
| Q1 | 0.97 | 1.07 | .038 | .042 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

**Figure 60. 20-Pin SOIC Package Diagram**




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.79 | 0.095 | 0.110 |
| A1 | 0.23 | 0.38 | 0.009 | 0.015 |
| A2 | 2.18 | 2.39 | 0.086 | 0.094 |
| b | 0.20 | 0.34 | 0.008 | 0.0135 |
| c | 0.13 | 0.25 | 0.005 | 0.010 |
| D | 15.75 | 16.00 | 0.620 | 0.630 |
| E | 7.39 | 7.59 | 0.291 | 0.299 |
| e | 0.635 BSC | | 0.025 BSC | |
| H | 10.16 | 10.41 | 0.400 | 0.410 |
| L | 0.51 | 1.016 | 0.020 | 0.040 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

**Figure 68. 48-Pin SSOP Package Design**

**Note:** Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.

| 8KB Standard Temperature: 0° to +70°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HSH4808C | 48-pin SSOP 8K OTP | ZGP323HSS2808C | 28-pin SOIC 8K OTP |
| ZGP323HSP4008C | 40-pin PDIP 8K OTP | ZGP323HSH2008C | 20-pin SSOP 8K OTP |
| ZGP323HSH2808C | 28-pin SSOP 8K OTP | ZGP323HSP2008C | 20-pin PDIP 8K OTP |
| ZGP323HSP2808C | 28-pin PDIP 8K OTP | ZGP323HSS2008C | 20-pin SOIC 8K OTP |

| 8KB Extended Temperature: -40° to +105°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HEH4808C | 48-pin SSOP 8K OTP | ZGP323HES2808C | 28-pin SOIC 8K OTP |
| ZGP323HEP4008C | 40-pin PDIP 8K OTP | ZGP323HEH2008C | 20-pin SSOP 8K OTP |
| ZGP323HEH2808C | 28-pin SSOP 8K OTP | ZGP323HEP2008C | 20-pin PDIP 8K OTP |
| ZGP323HEP2808C | 28-pin PDIP 8K OTP | ZGP323HES2008C | 20-pin SOIC 8K OTP |

| 8KB Automotive Temperature: -40° to +125°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HAH4808C | 48-pin SSOP 8K OTP | ZGP323HAS2808C | 28-pin SOIC 8K OTP |
| ZGP323HAP4008C | 40-pin PDIP 8K OTP | ZGP323HAH2008C | 20-pin SSOP 8K OTP |
| ZGP323HAH2808C | 28-pin SSOP 8K OTP | ZGP323HAP2008C | 20-pin PDIP 8K OTP |
| ZGP323HAP2808C | 28-pin PDIP 8K OTP | ZGP323HAS2008C | 20-pin SOIC 8K OTP |
| Replace C with G for Lead-Free Packaging | | | |

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

**Codes**

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

H = High Voltage

T = Temparature
- S = Standard 0° to +70°C
- E = Extended -40° to +105°C
- A = Automotive -40° to +125°C

P = Package Type:
- K = CDIP
- P = PDIP
- H = SSOP
- S = SOIC

## = Number of Pins

CC = Memory Size

M = Molding Compound

C = Standard Plastic Packaging Molding Compound
G = Green Plastic Molding Compound
E = Standard Cer Dip flow