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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323hsh4816c00tr">https://www.e-xfl.com/product-detail/zilog/zgp323hsh4816c00tr</a>



## Revision History

Each instance in Table 1 reflects a change to this document from its previous revision. To see more detail, click the appropriate link in the table.

**Table 1. Revision History of this Document**

<b>Date</b>	<b>Revision Level</b>	<b>Section</b>	<b>Description</b>	<b>Page #</b>
December 2004	02		Changed low power consumption, STOP and HALT mode current values, deleted mask option note, clarified temperature ranges in Tables 6 and 8 and 10. Added new Tables 9 and 10. Also added Characterization data to Table 11 and changed Program/Erase Endurance value in Table 12.	1,2,10 11,12, 13,14, 15
			Removed Preliminary designation	All
March 2005	03		Minor change to Table 9 Electrical Characteristics. Added 20, 28 and 40-pin CDIP parts in the Ordering Section.	11,90



Figure 68. 48-Pin SSOP Package Design ..... 89



## Development Features

Table 2 lists the features of ZiLOG<sup>®</sup>'s ZGP323H members.

**Table 2. Features**

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323H OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–5.5V

- Low power consumption—18mW (typical)
- T = Temperature  
S = Standard 0° to +70°C  
E = Extended -40° to +105°C  
A = Automotive -40° to +125°C
- Three standby modes:
  - STOP— (typical 1.8µA)
  - HALT— (typical 0.8mA)
  - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors

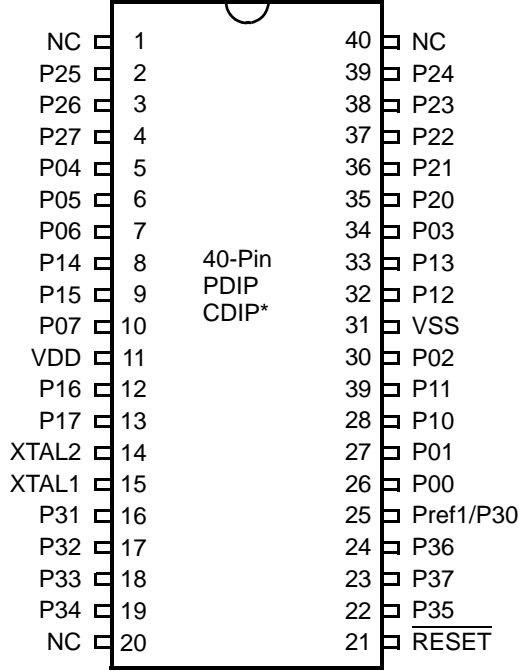


Figure 5. 40-Pin PDIP/CDIP\* Pin Configuration

► **Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.

**Table 9. GP323HS DC Characteristics (Continued)**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> =0°C to +70°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
I <sub>OL</sub>	Output Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>CC</sub>	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I <sub>CC1</sub>	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
I <sub>CC2</sub>	Standby Current (Stop Mode)	2.0V		1.6	8	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		3.6V		1.8	10	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		5.5V		1.9	12	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		2.0V		5	20	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		3.6V		8	30	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		5.5V		15	45	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
I <sub>LV</sub>	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage Protection			1.9	2.0	V	8MHz maximum Ext. CLK Freq.	
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage Detection			2.4		V		
V <sub>HVD</sub>	V <sub>CC</sub> High Voltage Detection			2.7		V		

**Notes:**

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF.
3. Oscillator stopped.
4. Oscillator stops when V<sub>CC</sub> falls below V<sub>BO</sub> limit.
5. It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to V<sub>CC</sub> and V<sub>SS</sub> pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.
6. Comparator and Timers are on. Interrupt disabled.
7. Typical values shown are at 25 degrees C.

**Table 10. GP323HE DC Characteristics**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = -40°C to +105°C			Units	Conditions	Notes
			Min	Typ(7)	Max			
V <sub>CC</sub>	Supply Voltage		2.0		5.5	V	See Note 5	5
V <sub>CH</sub>	Clock Input High Voltage	2.0-5.5	0.8 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.4	V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	2.0-5.5	0.7 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V		
V <sub>IL</sub>	Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.2 V <sub>CC</sub>	V		
V <sub>OH1</sub>	Output High Voltage	2.0-5.5	V <sub>CC</sub> -0.4			V	I <sub>OH</sub> = -0.5mA	

Table 11. GP323HA DC Characteristics

T <sub>A</sub> = -40°C to +125°C								
Symbol	Parameter	V <sub>CC</sub>	Min	Typ(7)	Max	Units	Conditions	Notes
V <sub>CC</sub>	Supply Voltage		2.0		5.5	V	See Note 5	5
V <sub>CH</sub>	Clock Input High Voltage	2.0-5.5	0.8 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.4	V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	2.0-5.5	0.7 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V		
V <sub>IL</sub>	Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.2 V <sub>CC</sub>	V		
V <sub>OH1</sub>	Output High Voltage	2.0-5.5	V <sub>CC</sub> -0.4			V	I <sub>OH</sub> = -0.5mA	
V <sub>OH2</sub>	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V <sub>CC</sub> -0.8			V	I <sub>OH</sub> = -7mA	
V <sub>OL1</sub>	Output Low Voltage	2.0-5.5			0.4	V	I <sub>OL</sub> = 4.0mA	
V <sub>OL2</sub>	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I <sub>OL</sub> = 10mA	
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V <sub>REF</sub>	Comparator Reference Voltage	2.0-5.5	0		V <sub>DD</sub> -1.75	V		
I <sub>IL</sub>	Input Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub> Pull-ups disabled	
R <sub>PU</sub>	Pull-up Resistance	2.0V	200		700	KΩ	V <sub>IN</sub> = 0V; Pullups selected by mask option	
		3.6V	50		300	KΩ		
		5.0V	25		175	KΩ		
I <sub>OL</sub>	Output Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub>	
I <sub>CC</sub>	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I <sub>CC1</sub>	Standby Current (HALT Mode)	2.0V		0.5	1.6	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		3.6V		0.8	2.0	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
I <sub>CC2</sub>	Standby Current (Stop Mode)	2.0V		1.6	15	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		3.6V		1.8	20	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		5.5V		1.9	25	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT not Running	3
		2.0V		5	30	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		3.6V		8	40	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
		5.5V		15	60	μA	V <sub>IN</sub> = 0 V, V <sub>CC</sub> WDT is Running	3
I <sub>LV</sub>	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage Detection			2.4		V		

## Pin Functions

### XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

### XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonant to the on-chip oscillator output.

### Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

- **Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

The Port 0 direction is reset to its default state following an SMR.





**Table 16. CTR1(0D)01H T8 and T16 Common Functions (Continued)**

Field	Bit Position		Value	Description
Transmit_Submode/ Glitch_Filter	----32--	R/W	00*	Transmit Mode
			01	Normal Operation
		R	10	Ping-Pong Mode
			11	T16_Out = 0
		W	00*	T16_Out = 1
			01	Demodulation Mode
		R	10	No Filter
			11	4 SCLK Cycle
		W	00*	8 SCLK Cycle
			01	Reserved
Initial_T8_Out/ Rising Edge	-----1-	R/W	0*	Transmit Mode
			1	T8_OUT is 0 Initially
		R	0*	T8_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Rising Edge
			1	Rising Edge Detected
		R	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/ Falling_Edge	-----0	R/W	0*	Transmit Mode
			1	T16_OUT is 0 Initially
		R	0*	T16_OUT is 1 Initially
			1	Demodulation Mode
		W	0	No Falling Edge
			1	Falling Edge Detected
		R	0	No Effect
			1	Reset Flag to 0

**Note:**

\*Default at Power-On Reset

\*Default at Power-On Reset. Not reset with Stop Mode recovery.

**Mode**

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

**P36\_Out/Demodulator\_Input**

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).

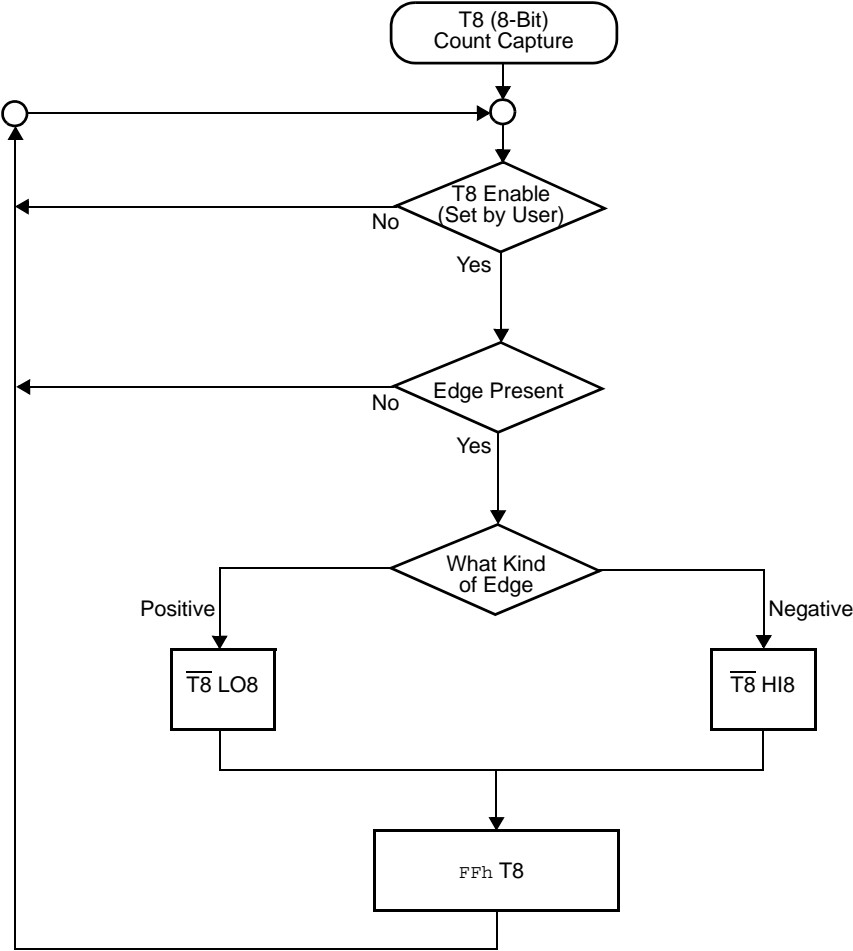


Figure 23. Demodulation Mode Count Capture Flowchart

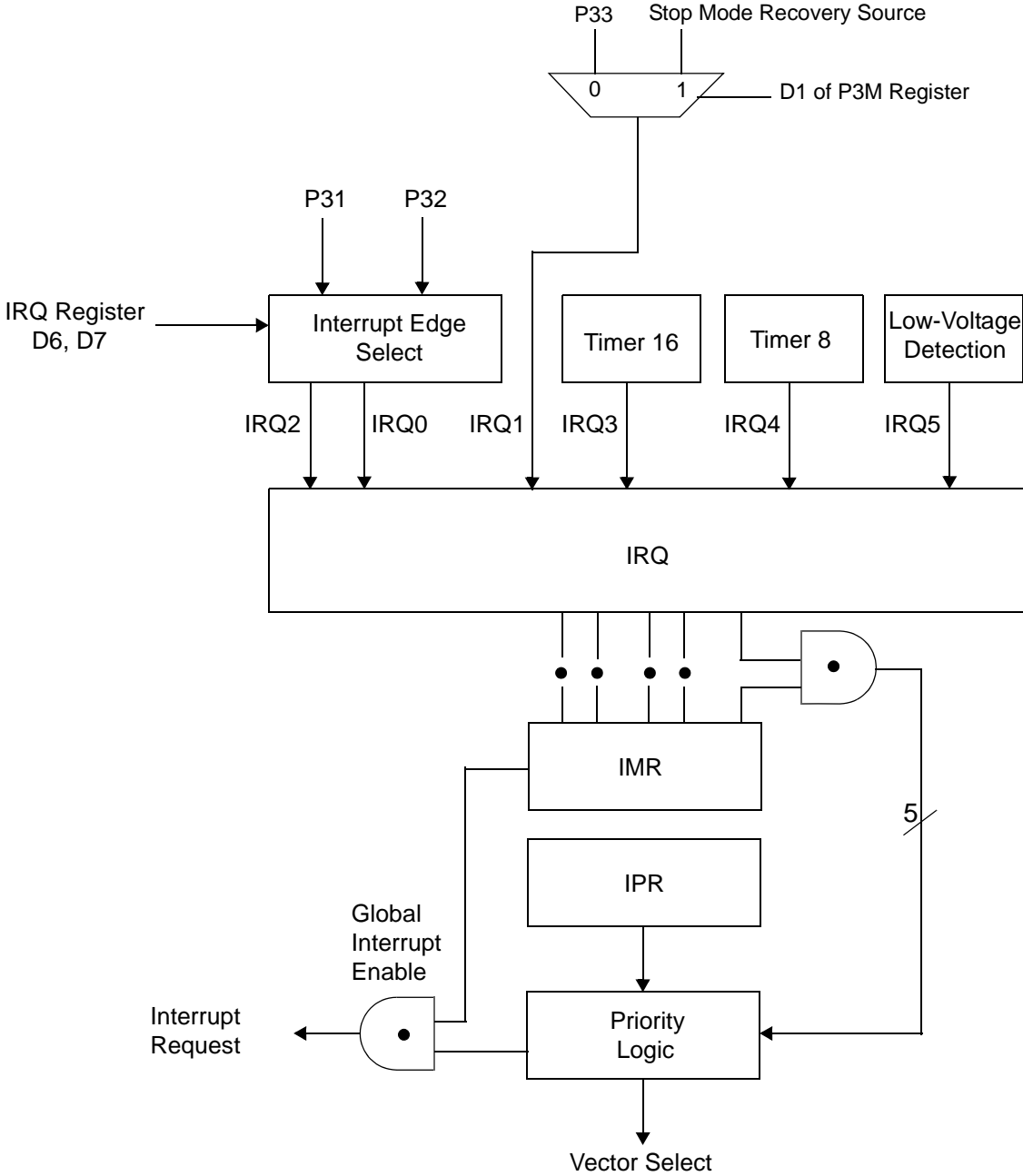
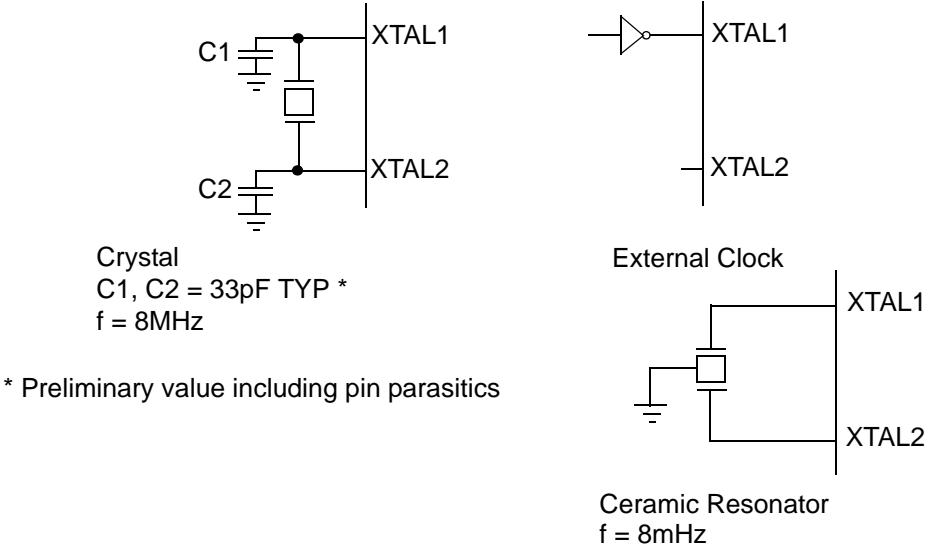


Figure 30. Interrupt Block Diagram

**Clock**

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal or ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω. The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.



**Figure 31. Oscillator Configuration**



### Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

### Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bit D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

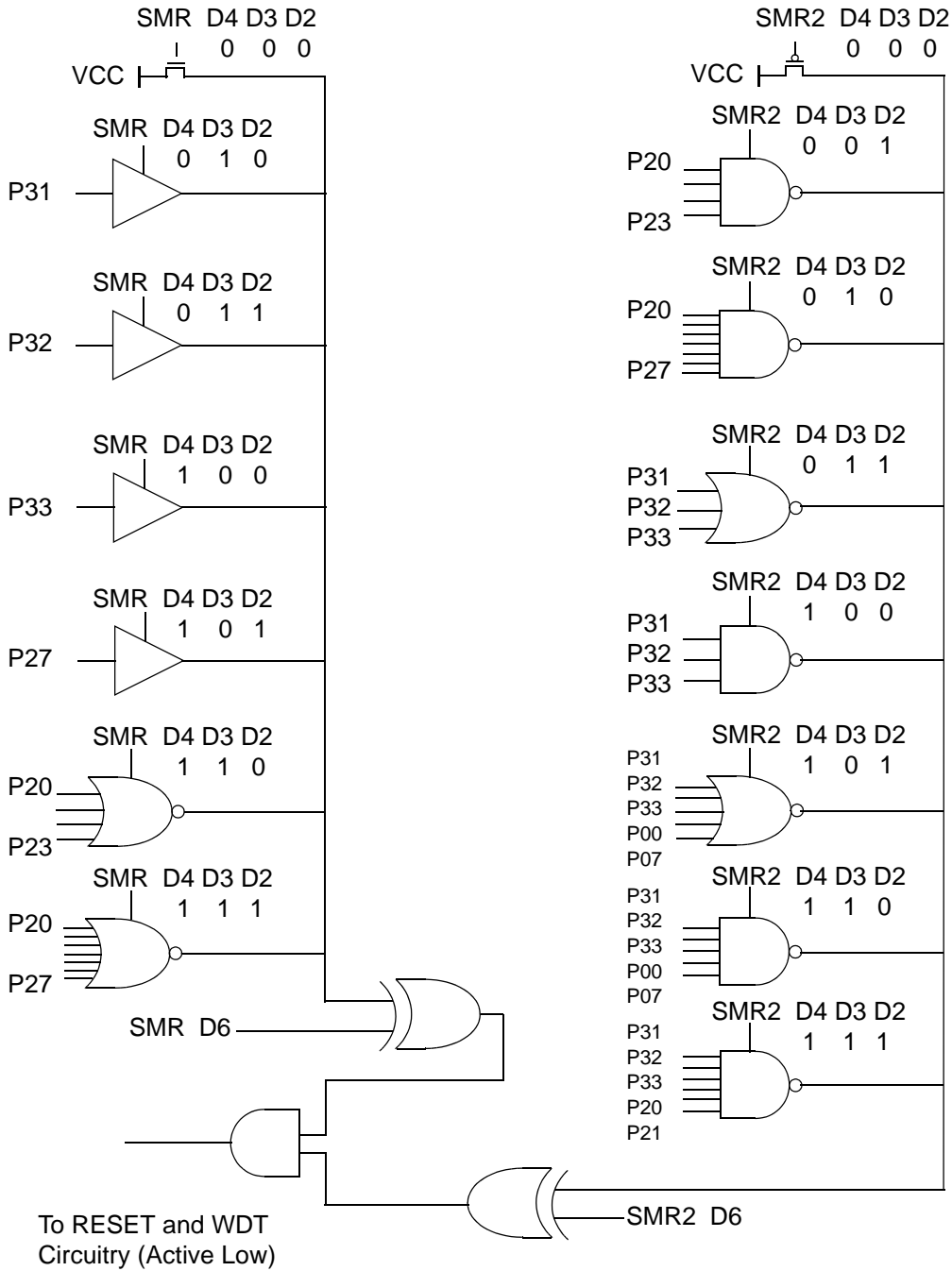


Figure 35. Stop Mode Recovery Source



CTR1(0D)01H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

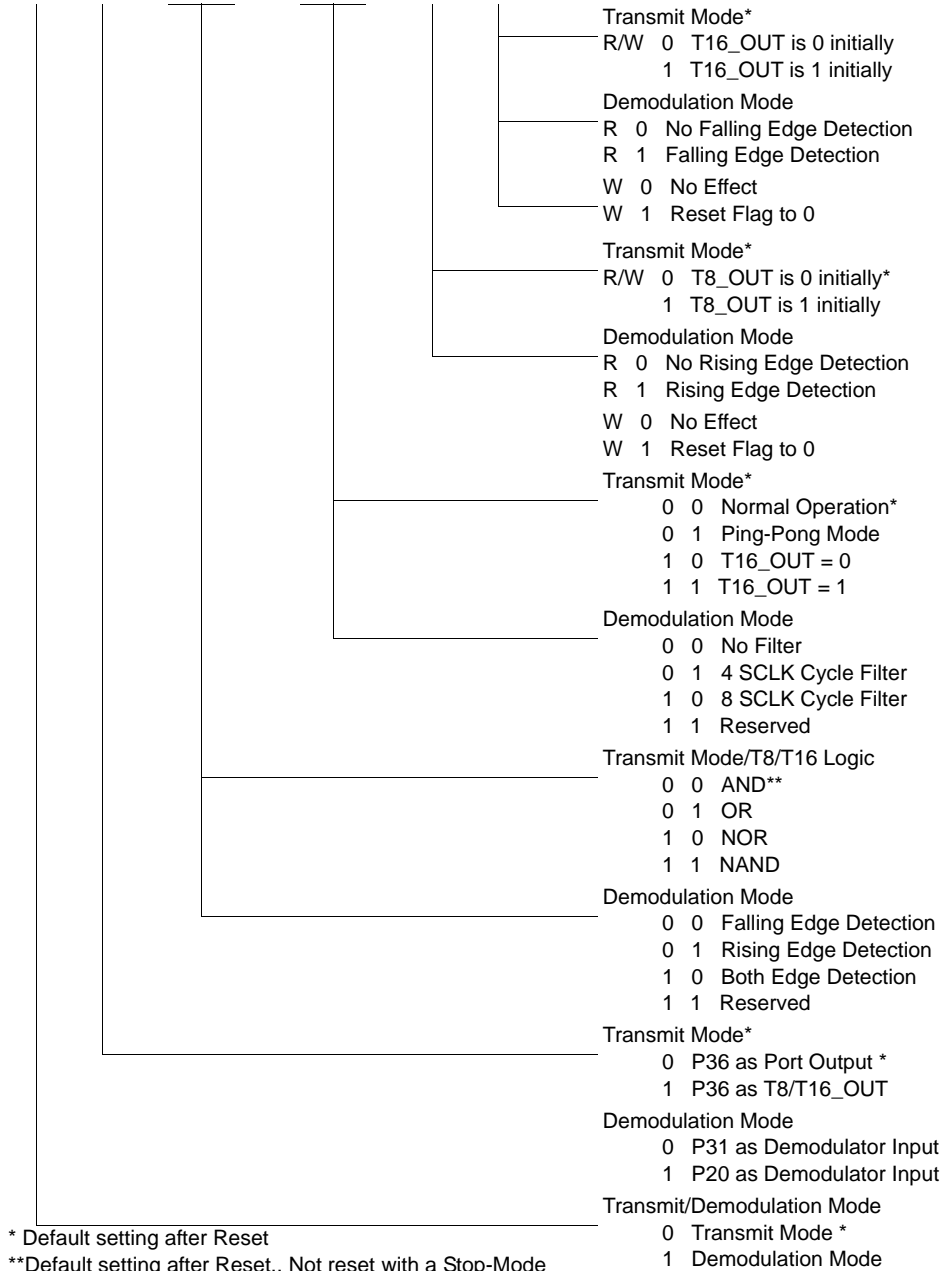
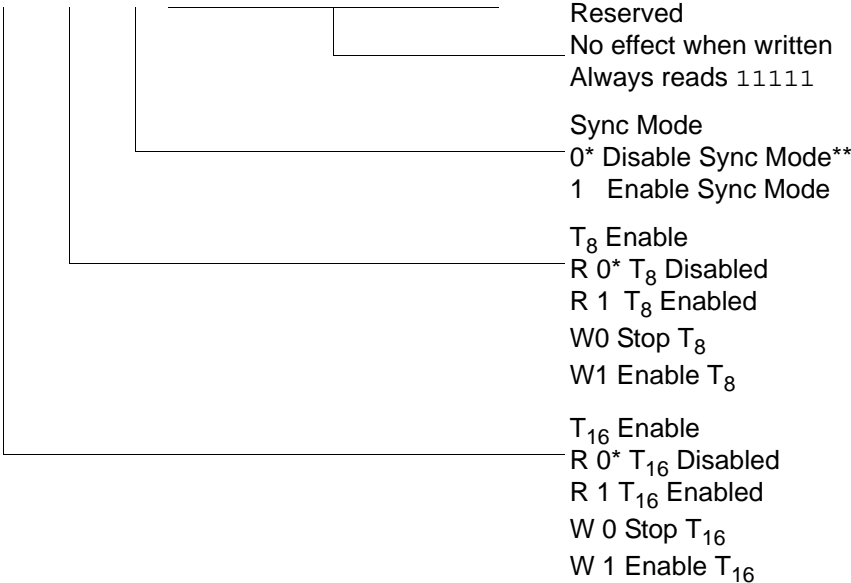


Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)



CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



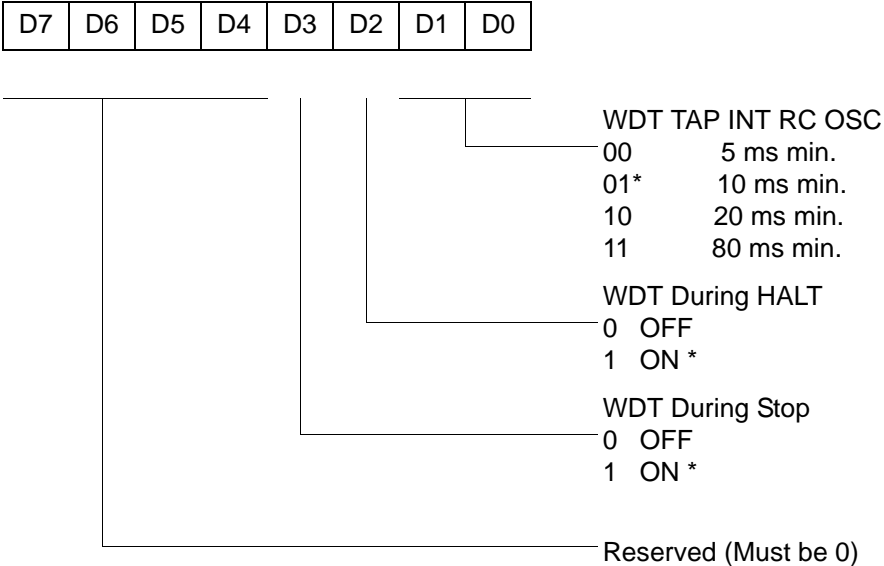
\* Default setting after reset.  
\*\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)





WDTMR(0F)0FH

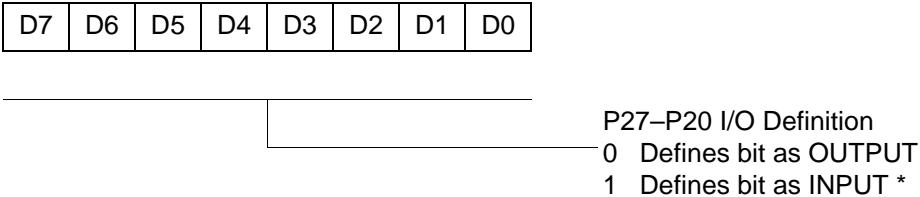


\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only)

### Standard Control Registers

R246 P2M(F6H)



\* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 48. Port 2 Mode Register (F6H: Write Only)

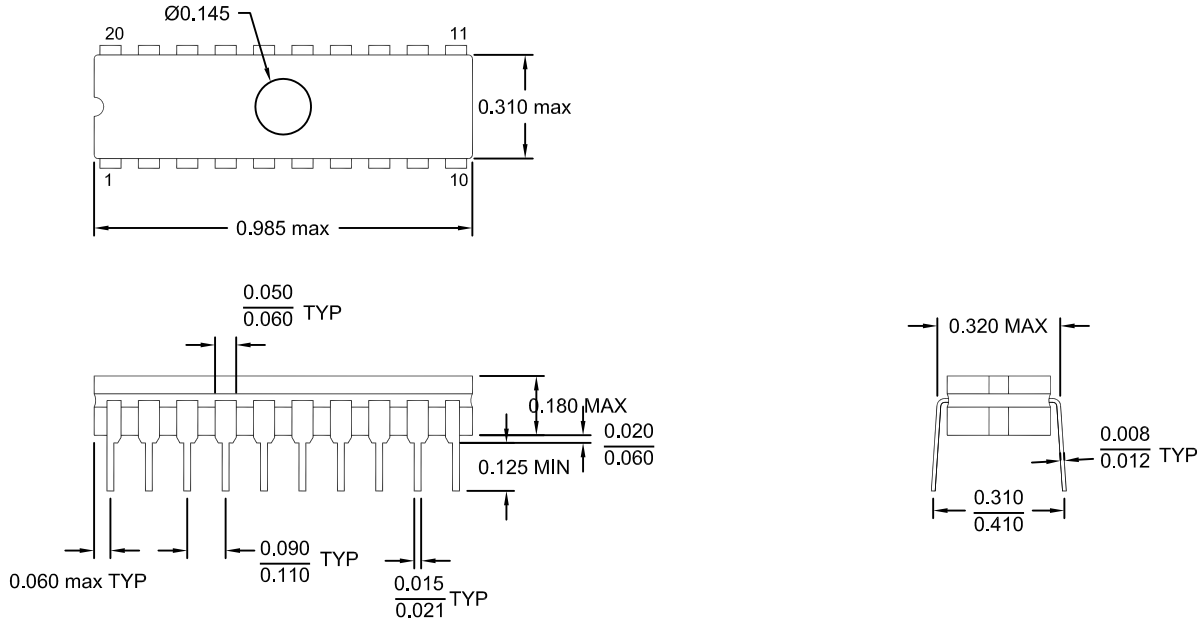


Figure 58. 20-Pin CDIP Package

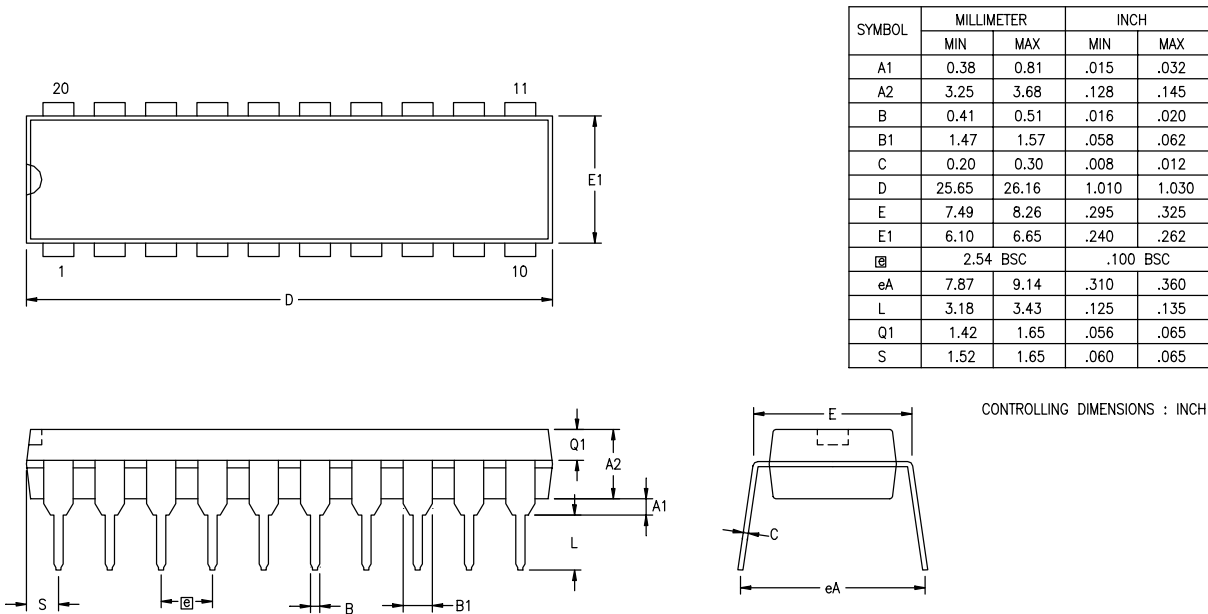


Figure 59. 20-Pin PDIP Package Diagram

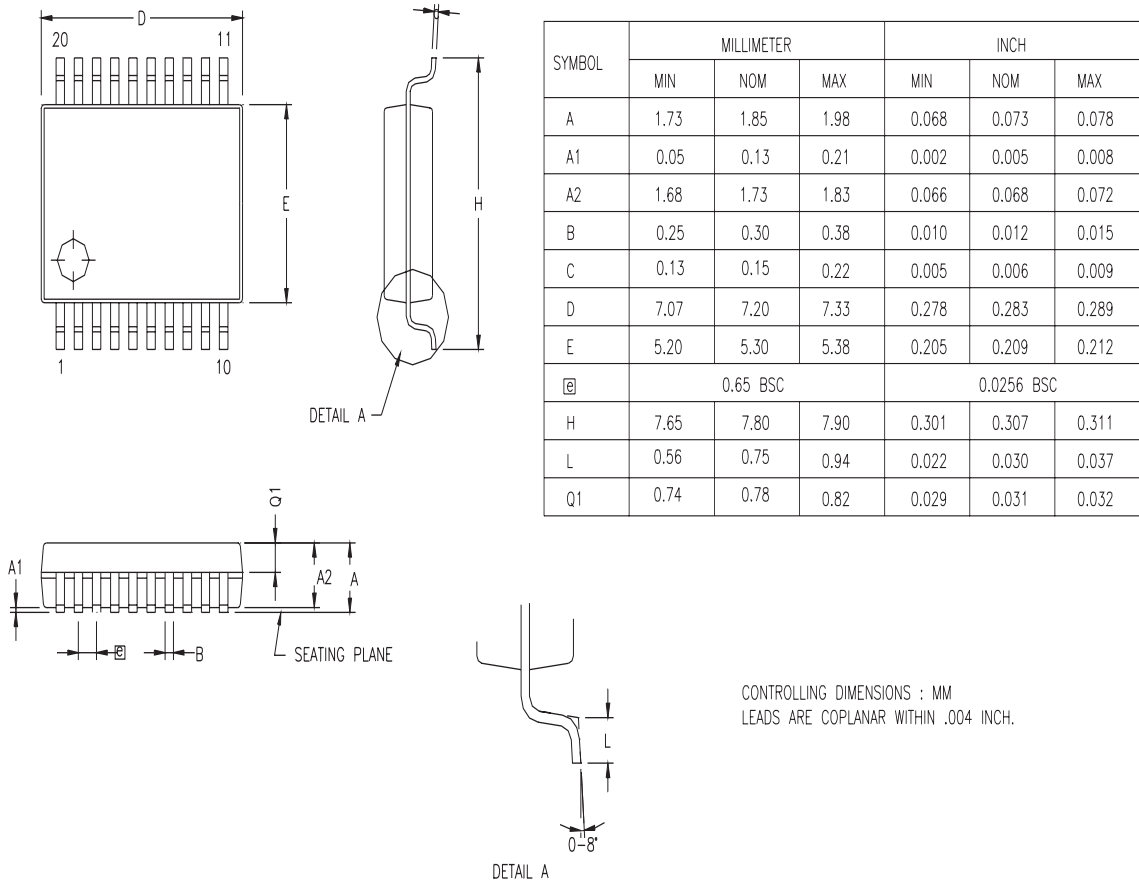


Figure 61. 20-Pin SSOP Package Diagram




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**8KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323HSH4808C	48-pin SSOP 8K OTP	ZGP323HSS2808C	28-pin SOIC 8K OTP
ZGP323HSP4008C	40-pin PDIP 8K OTP	ZGP323HSH2008C	20-pin SSOP 8K OTP
ZGP323HSH2808C	28-pin SSOP 8K OTP	ZGP323HSP2008C	20-pin PDIP 8K OTP
ZGP323HSP2808C	28-pin PDIP 8K OTP	ZGP323HSS2008C	20-pin SOIC 8K OTP

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**8KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323HEH4808C	48-pin SSOP 8K OTP	ZGP323HES2808C	28-pin SOIC 8K OTP
ZGP323HEP4008C	40-pin PDIP 8K OTP	ZGP323HEH2008C	20-pin SSOP 8K OTP
ZGP323HEH2808C	28-pin SSOP 8K OTP	ZGP323HEP2008C	20-pin PDIP 8K OTP
ZGP323HEP2808C	28-pin PDIP 8K OTP	ZGP323HES2008C	20-pin SOIC 8K OTP

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**8KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323HAH4808C	48-pin SSOP 8K OTP	ZGP323HAS2808C	28-pin SOIC 8K OTP
ZGP323HAP4008C	40-pin PDIP 8K OTP	ZGP323HAH2008C	20-pin SSOP 8K OTP
ZGP323HAH2808C	28-pin SSOP 8K OTP	ZGP323HAP2008C	20-pin PDIP 8K OTP
ZGP323HAP2808C	28-pin PDIP 8K OTP	ZGP323HAS2008C	20-pin SOIC 8K OTP

Replace C with G for Lead-Free Packaging

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