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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hsh4832g



- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

General Description

The ZGP323H is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The ZGP323H architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

► **Note:** All signals with an overline, " $\overline{}$ ", are active Low. For example, $\overline{B/W}$, in which WORD is active Low, and $\overline{B/W}$, in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 3.

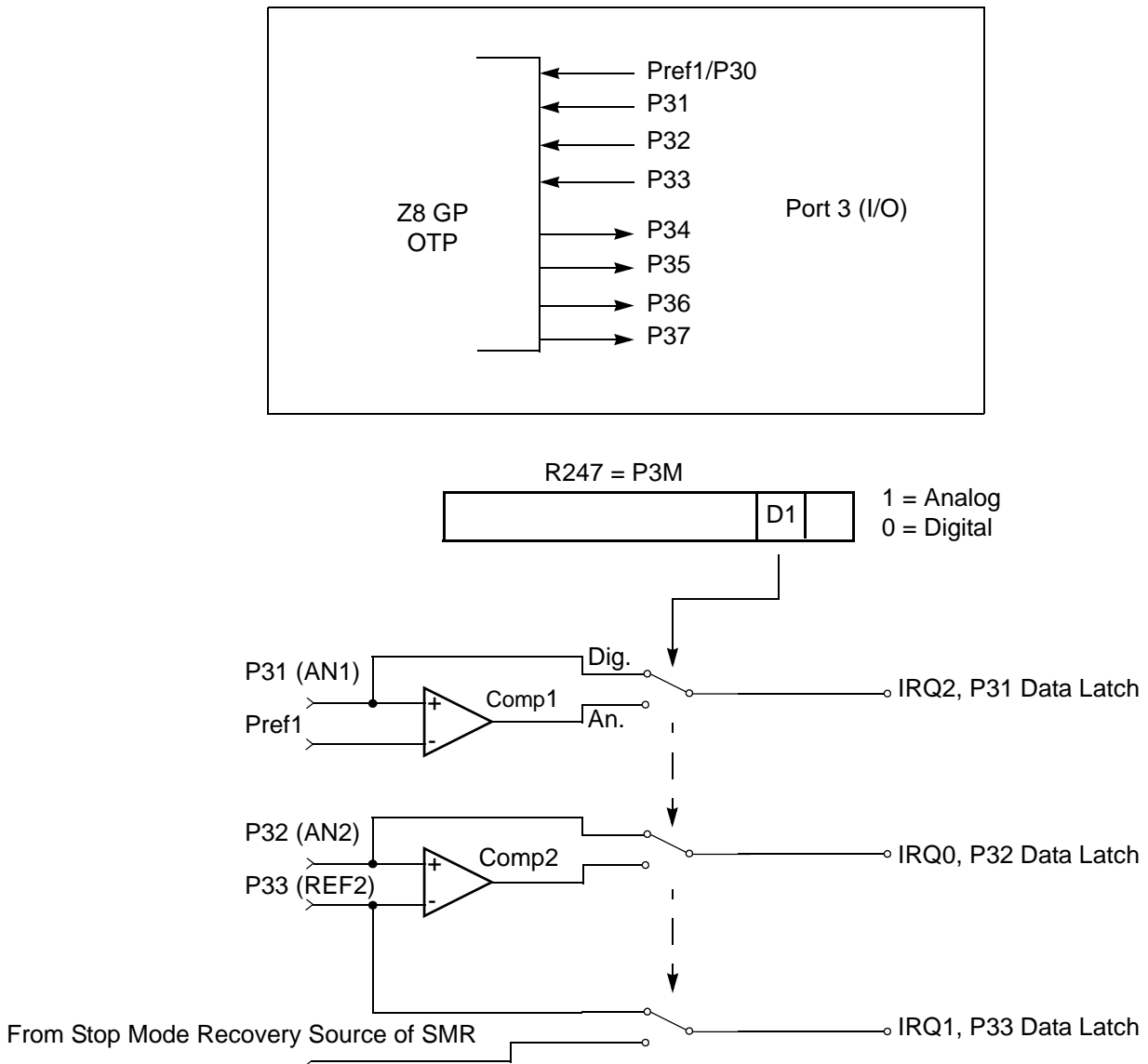


Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “T8 and T16 Common Functions—

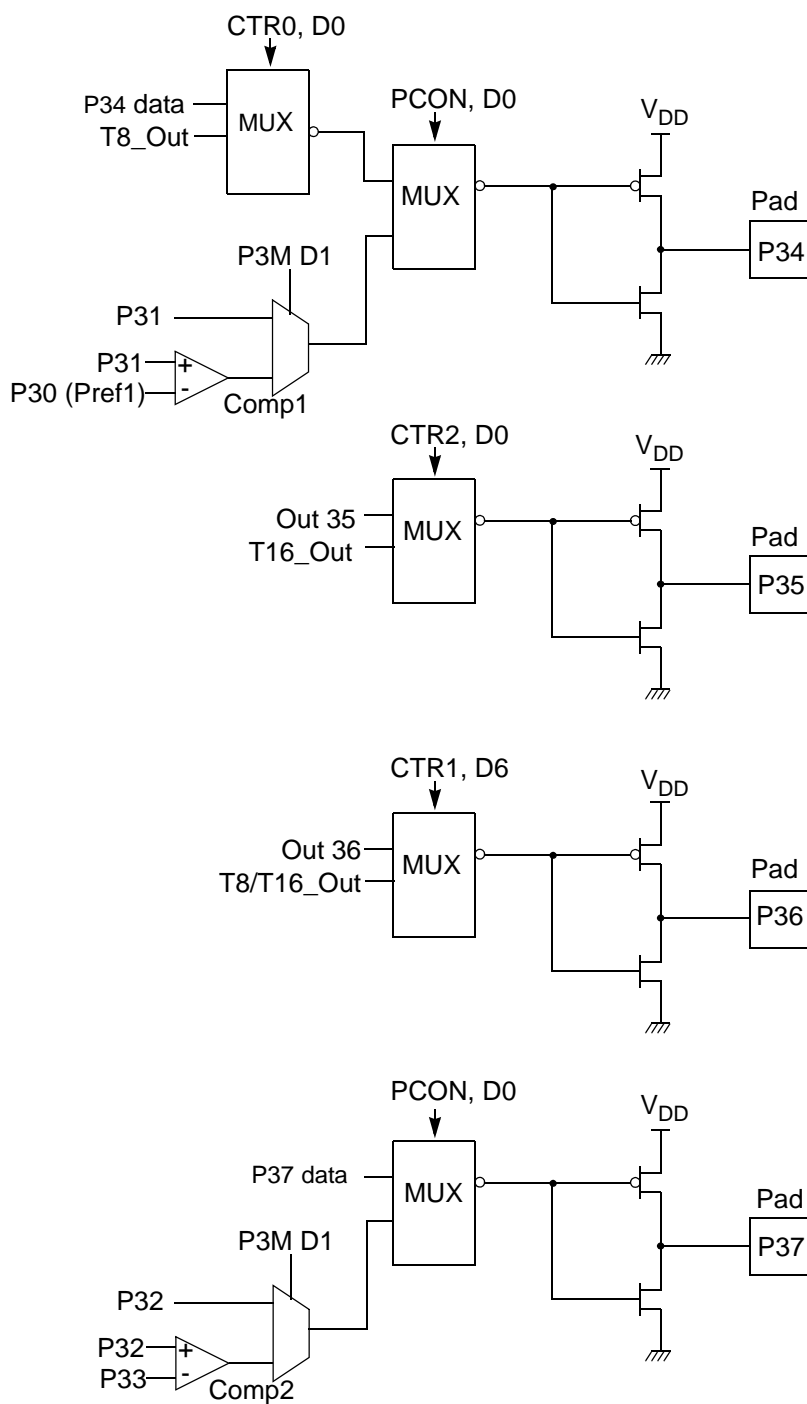


Figure 13. Port 3 Counter/Timer Output Configuration

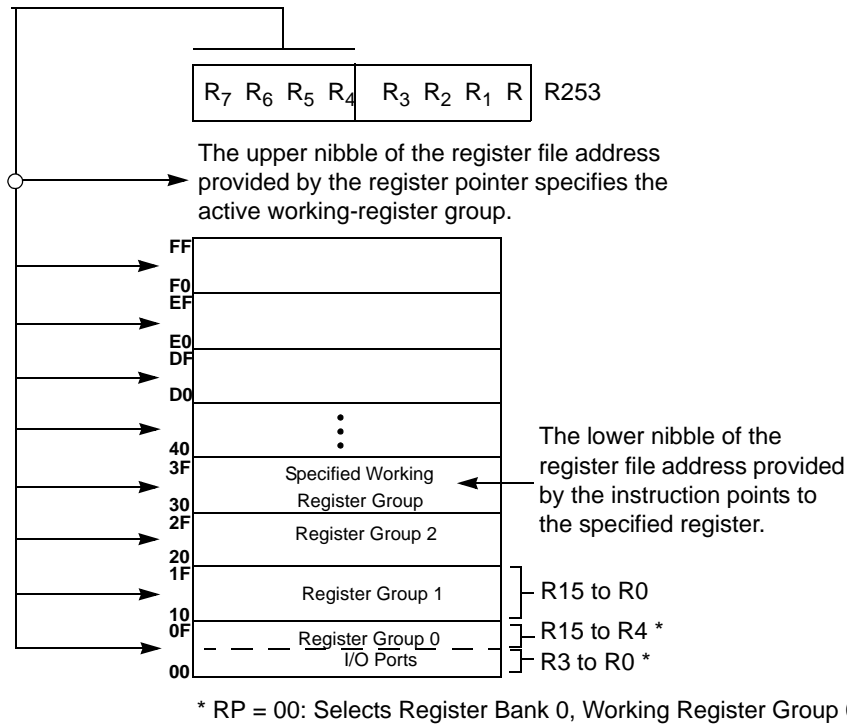


Figure 17. Register Pointer—Detail

Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

Table 18. CTR3 (D)03H: T8/T16 Control Register (Continued)

Field	Bit Position		Value	Description
Reserved	---43210	R	1	Always reads 11111
		W	x	No Effect

*Indicates the value upon Power-On Reset.

**Indicates the value upon Power-On Reset. Not reset with a Stop Mode recovery.

Counter/Timer Functional Blocks

Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 18).

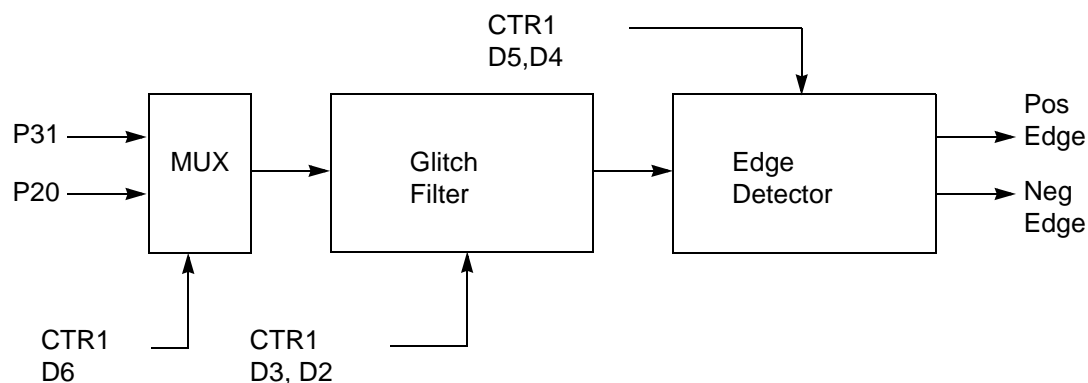


Figure 18. Glitch Filter Circuitry

T8 Transmit Mode

Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1; if it is 1, T8_OUT is 0. See Figure 19.

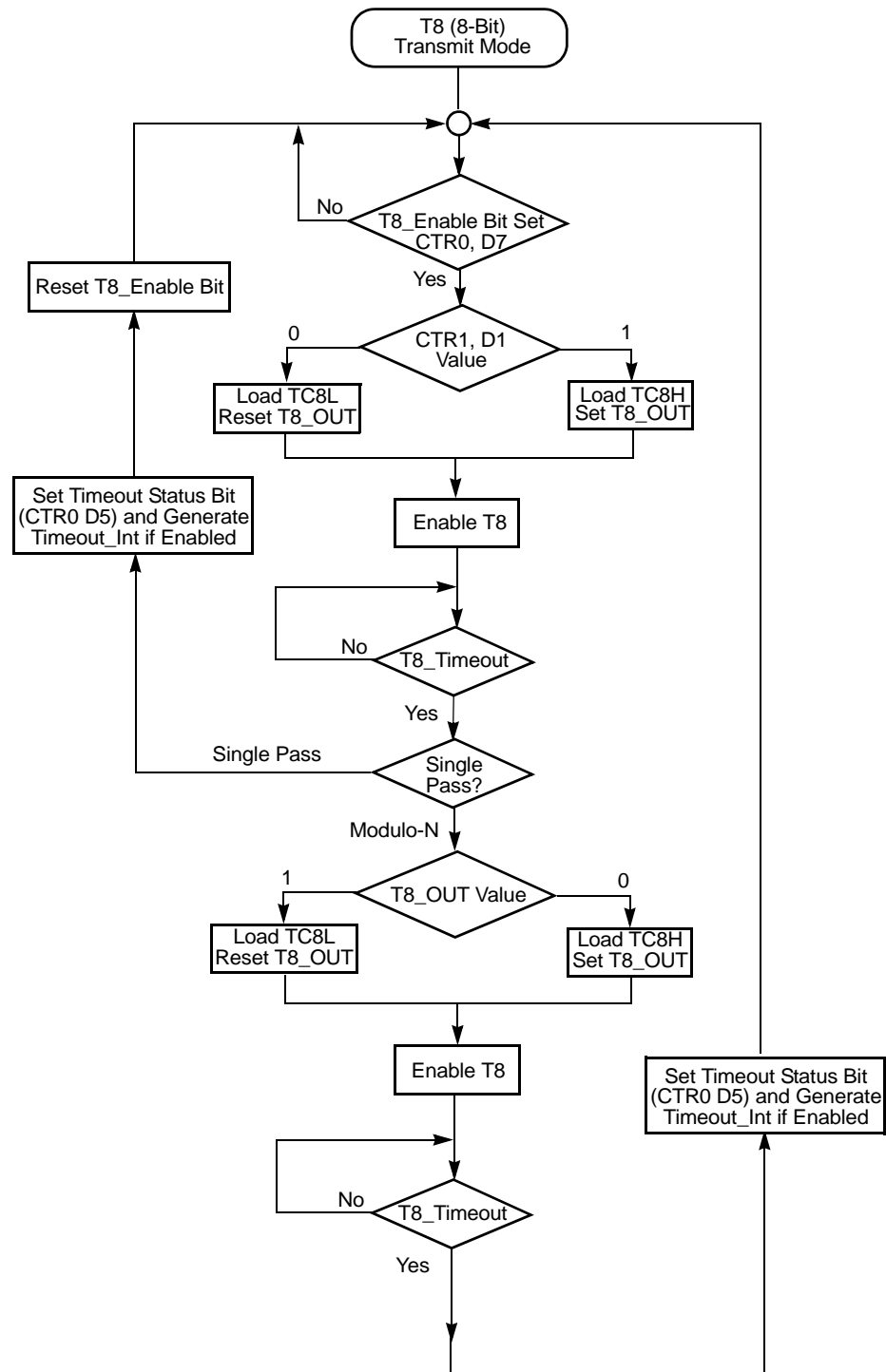


Figure 19. Transmit Mode Flowchart

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.

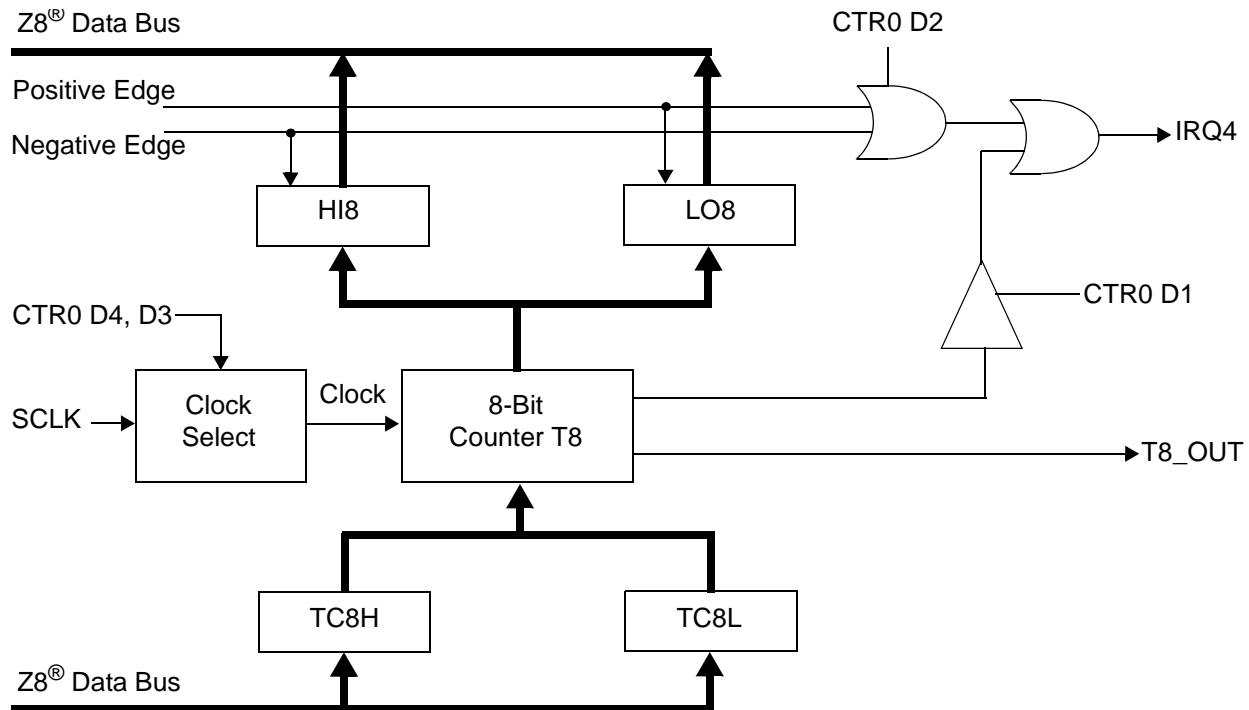


Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.

into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFh (see Figure 23 and Figure 24).

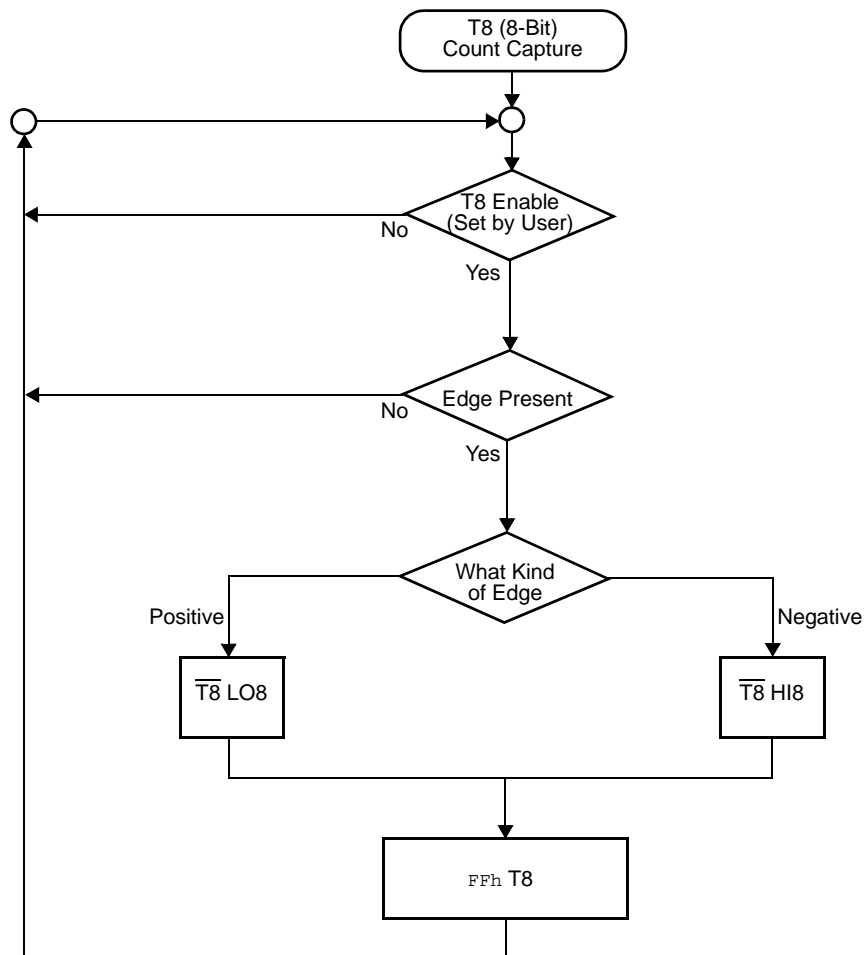


Figure 23. Demodulation Mode Count Capture Flowchart

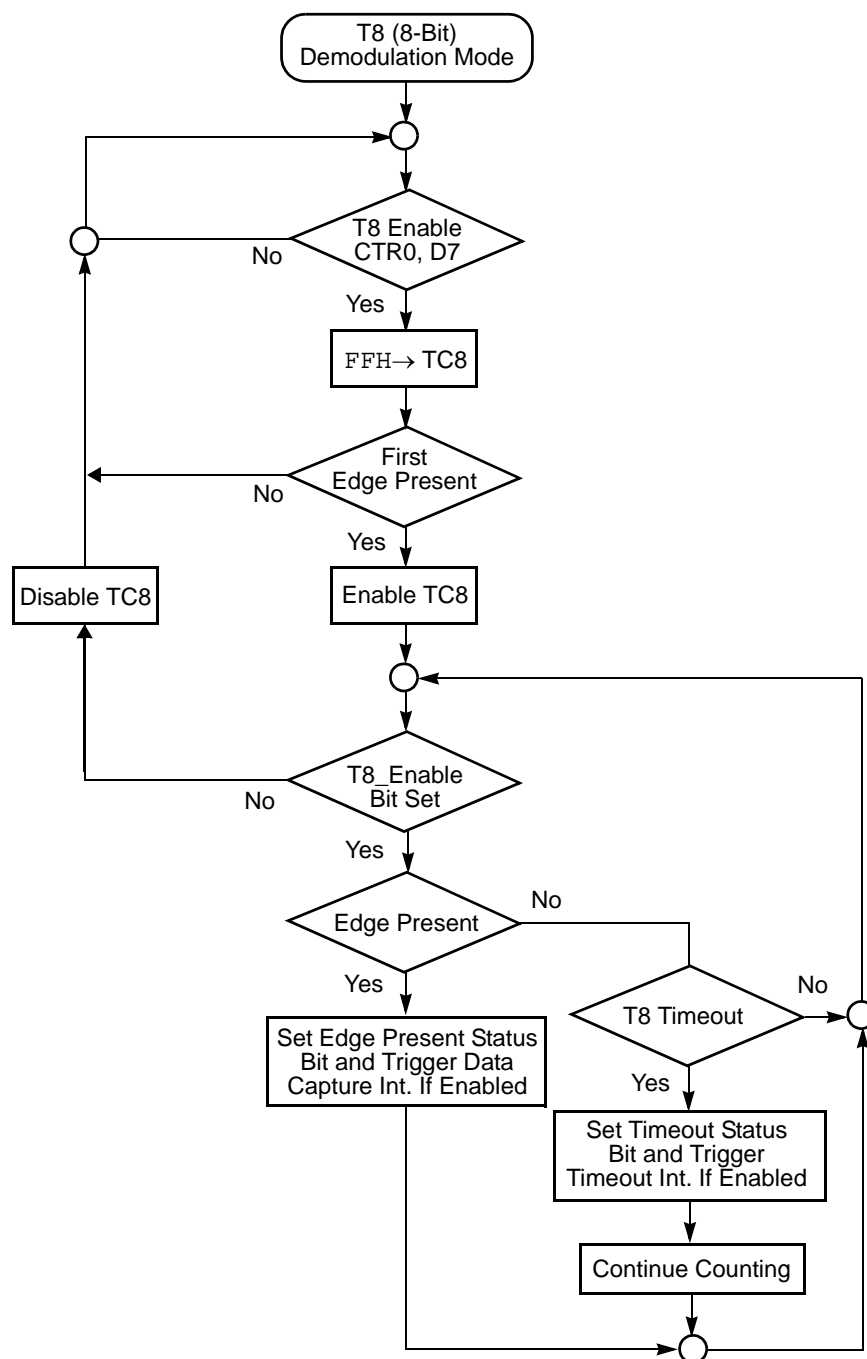


Figure 24. Demodulation Mode Flowchart

If D6 of CTR2 Is 1

T16 ignores the subsequent edges in the input signal and continues counting down. A timeout of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If the D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both depending on CTR1, D5; D4), continuing to ignore subsequent edges.

This T16 mode generally measures mark time, the length of an active carrier signal burst.

If T16 reaches 0, T16 continues counting from `FFFFh`. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt timeout can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in TRANSMIT Mode. T8 and T16 must be programmed in Single-Pass mode (CTR0, D6; CTR2, D6), and Ping-Pong mode must be programmed in CTR1, D3; D2. The user can begin the operation by enabling either T8 or T16 (CTR0, D7 or CTR2, D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1, D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled, and T16 is enabled. T16_OUT then switches to its initial value (CTR1, D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, repeating the entire cycle. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0, D1; CTR2, D1). To stop the ping-pong operation, write 00 to bits D3 and D2 of CTR1. See Figure 28.

- **Note:** Enabling ping-pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and reset the status flags before instituting this operation.

Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal or ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ω . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.

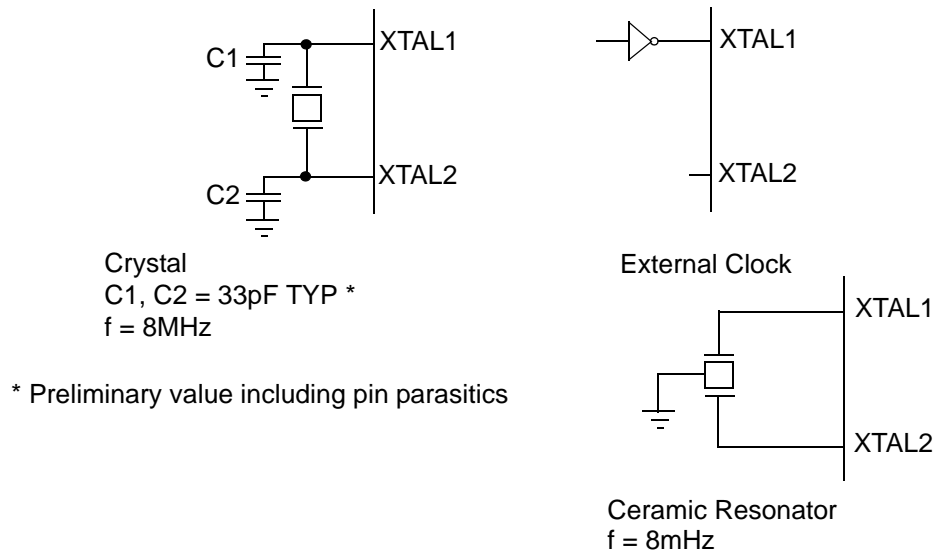
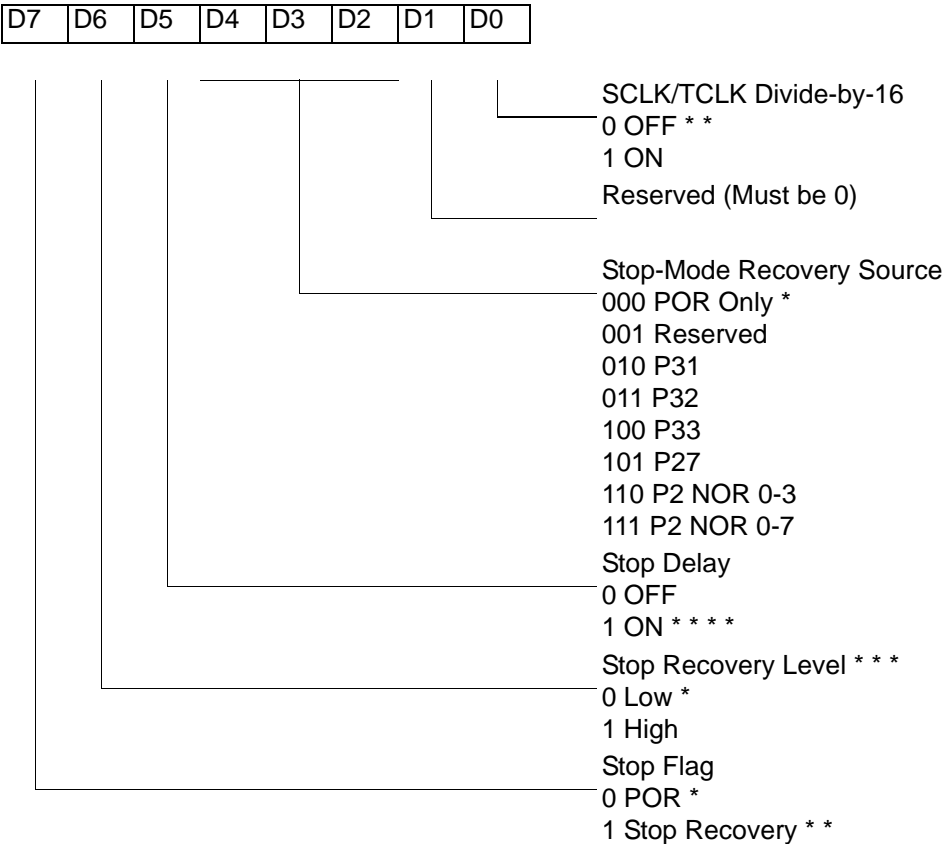


Figure 31. Oscillator Configuration



SMR(0F)0BH



* Default after Power On Reset or Watch-Dog Reset
* * Default setting after Reset and Stop Mode Recovery
* * * At the XOR gate input
* * * * Default setting after reset. Must be 1 if using a crystal or resonator clock source.

Figure 33. STOP Mode Recovery Register

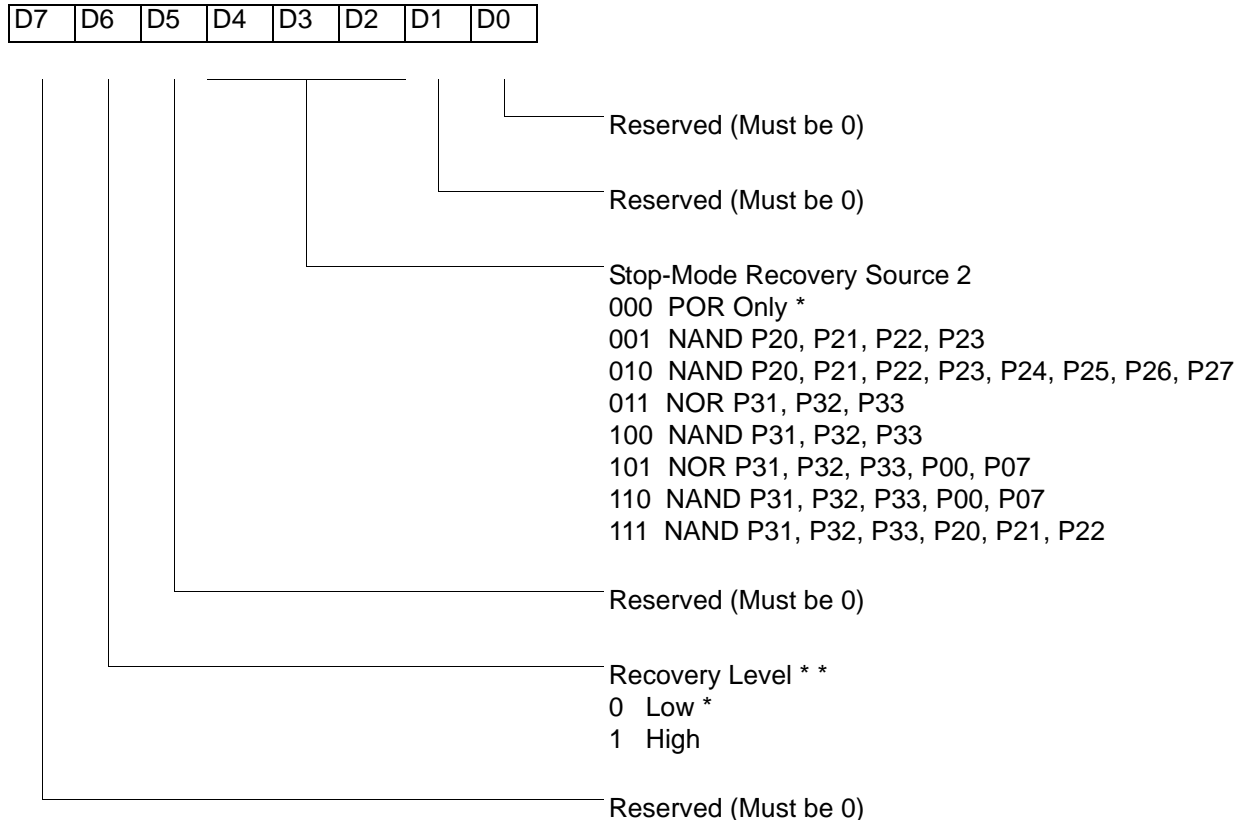
SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK (Figure 34). This control selectively reduces device power consumption during normal processor execution (SCLK control) and/or Halt Mode (where TCLK sources interrupt logic). After Stop Mode Recovery, this bit is set to a 0.

Stop Mode Recovery Register 2 (SMR2)

This register determines the mode of Stop Mode Recovery for SMR2 (Figure 36).

SMR2(0F)DH



Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

* Default setting after reset

** At the XOR gate input

Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only)

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop Mode Recovery.

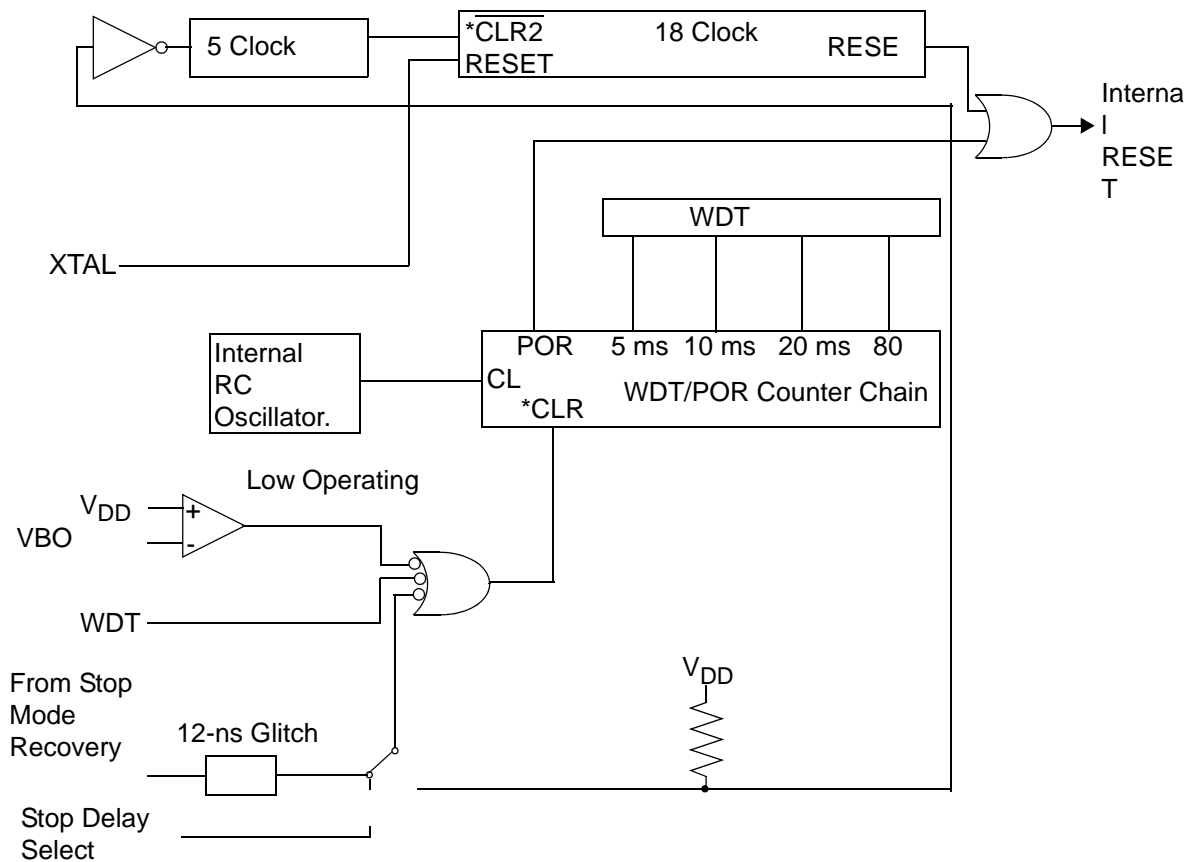
► **Note:** Port pins configured as outputs are ignored as an SMR or SMR2 recovery source. For example, if the NAND or P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

Table 23. Watch-Dog Timer Time Select

D1	D0	Timeout of Internal RC-Oscillator
0	0	5ms min.
0	1	10ms min.
1	0	20ms min.
1	1	80ms min.

WDTMR During Halt (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1. See Figure 38.



* CLR1 and $\overline{\text{CLR2}}$ enable the WDT/POR and 18 Clock Reset timers respectively upon a Low-to-

Figure 38. Resets and WDT

WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

EPROM Selectable Options

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

Table 24. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V_{DD} is at the required level for correct operation of the device. Reset is globally driven when V_{DD} falls below V_{BO} . A small drop in V_{DD} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V_{DD} is allowed to stay above V_{RAM} , the RAM content is preserved. When the power level is returned to above V_{BO} , the device performs a POR and functions normally.

CTR1(0D)01H

D7	D6	D5	D4	D3	D2	D1	D0
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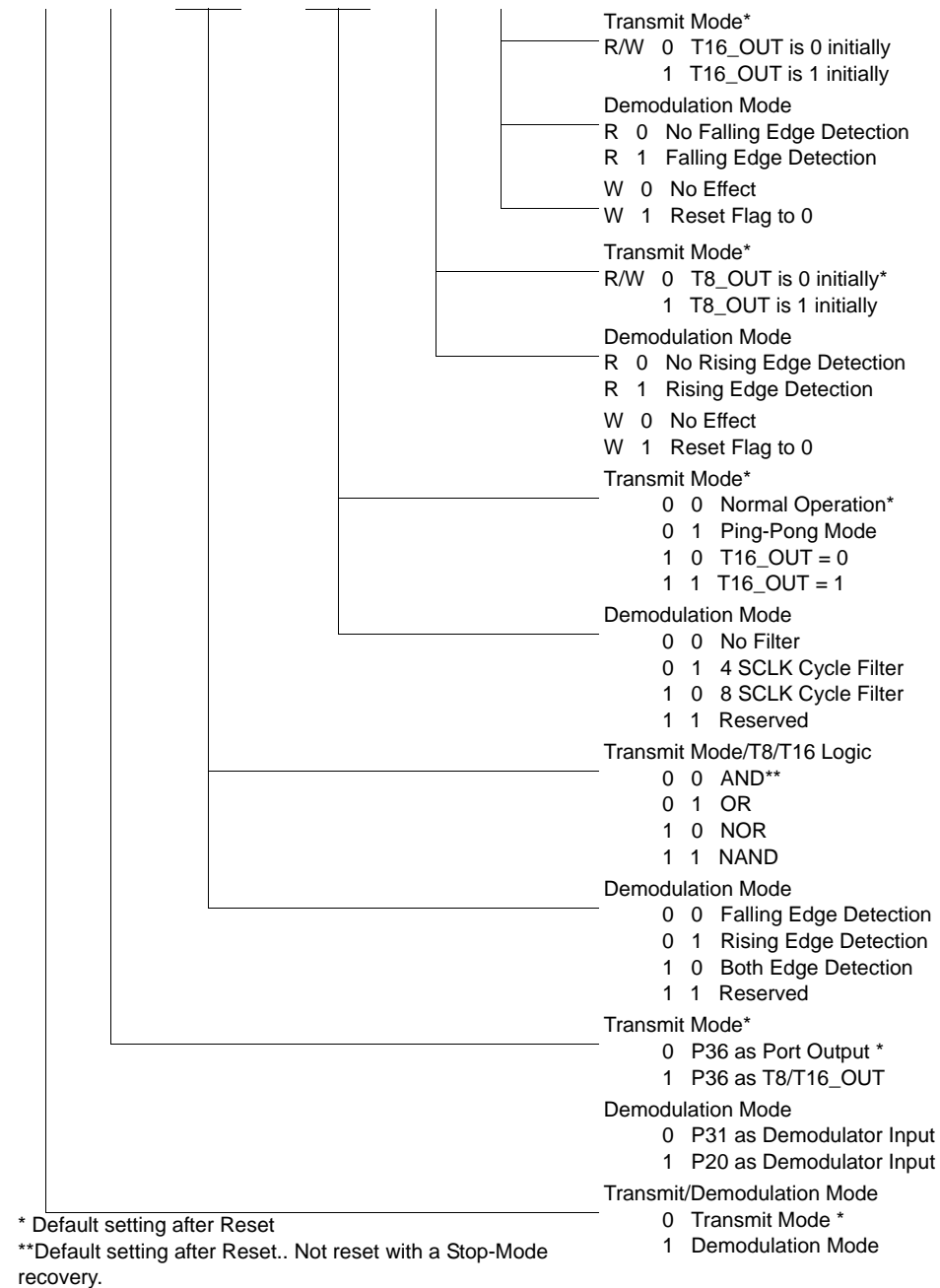


Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)



- **Notes:** Take care in differentiating the Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Changing from one mode to another cannot be performed without disabling the counter/timers.

R250 IRQ(FAH)

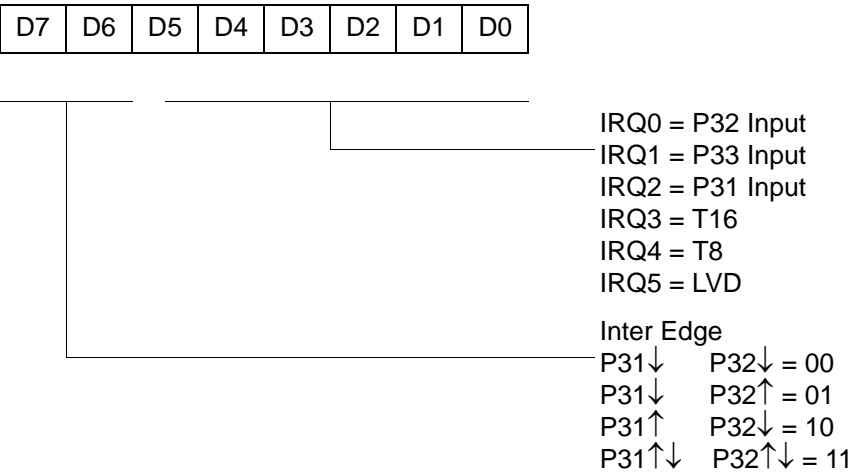


Figure 52. Interrupt Request Register (FAH: Read/Write)

R251 IMR(FBH)



* Default setting after reset
** Only by using EI, DI instruction; DI is required before changing the IMR register

Figure 53. Interrupt Mask Register (FBH: Read/Write)



R252 Flags(FCH)

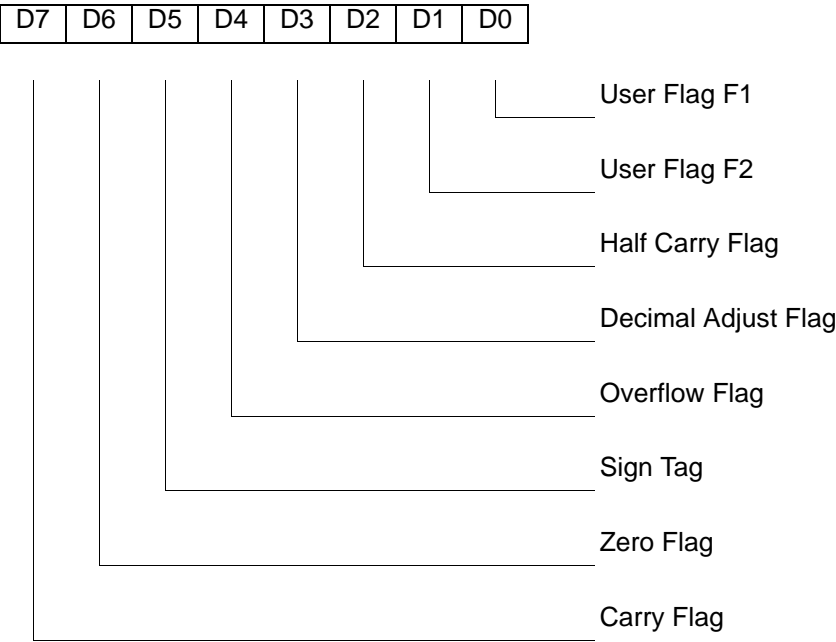
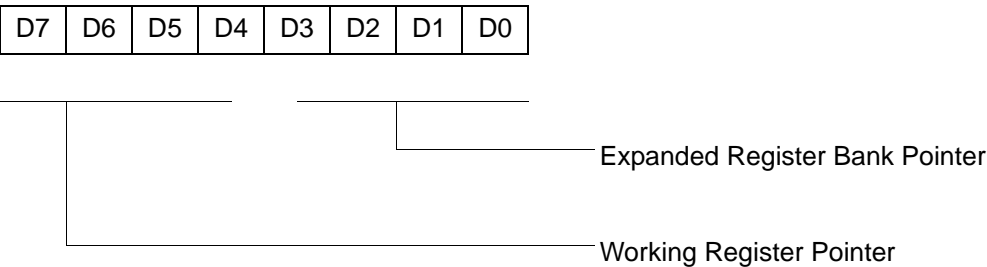


Figure 54. Flag Register (FCH: Read/Write)

R253 RP(FDH)



Default setting after reset = 0000 0000

Figure 55. Register Pointer (FDH: Read/Write)



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