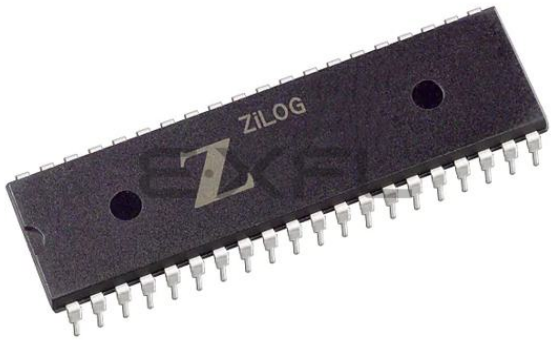


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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | - |
| Peripherals | HLVD, POR, WDT |
| Number of I/O | 32 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 237 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.620", 15.75mm) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/zgp323hsp4016c |

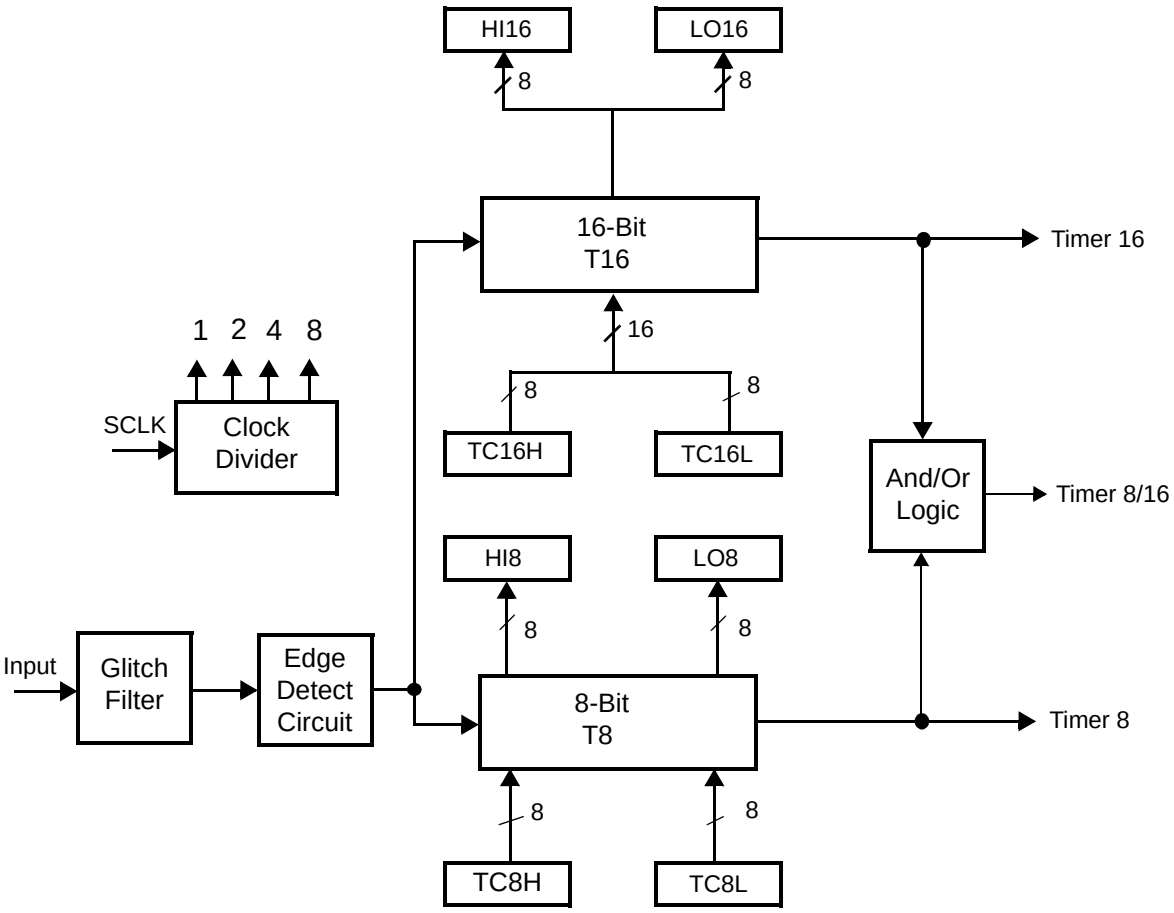



**Figure 2. Counter/Timers Diagram**

## Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.

**Table 11. GP323HA DC Characteristics**

| | | | $T_A$= -40°C to +125°C | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **$V_{CC}$** | **Min** | **Typ(7)** | **Max** | **Units** | **Conditions** | **Notes** |
| $V_{CC}$ | Supply Voltage | | 2.0 | | 5.5 | V | See Note 5 | 5 |
| $V_{CH}$ | Clock Input High Voltage | 2.0-5.5 | 0.8 $V_{CC}$ | | $V_{CC}$+0.3 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 2.0-5.5 | $V_{SS}$–0.3 | | 0.4 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 2.0-5.5 | 0.7 $V_{CC}$ | | $V_{CC}$+0.3 | V | | |
| $V_{IL}$ | Input Low Voltage | 2.0-5.5 | $V_{SS}$–0.3 | | 0.2 $V_{CC}$ | V | | |
| $V_{OH1}$ | Output High Voltage | 2.0-5.5 | $V_{CC}$–0.4 | | | V | $I_{OH}$ = –0.5mA | |
| $V_{OH2}$ | Output High Voltage (P36, P37, P00, P01) | 2.0-5.5 | $V_{CC}$–0.8 | | | V | $I_{OH}$ = –7mA | |
| $V_{OL1}$ | Output Low Voltage | 2.0-5.5 | | | 0.4 | V | $I_{OL}$ = 4.0mA | |
| $V_{OL2}$ | Output Low Voltage (P00, P01, P36, P37) | 2.0-5.5 | | | 0.8 | V | $I_{OL}$ = 10mA | |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 2.0-5.5 | | | 25 | mV | | |
| $V_{REF}$ | Comparator Reference Voltage | 2.0-5.5 | 0 | | $V_{DD}$ -1.75 | V | | |
| $I_{IL}$ | Input Leakage | 2.0-5.5 | –1 | | 1 | µA | $V_{IN}$ = 0V, $V_{CC}$ Pull-ups disabled | |
| $R_{PU}$ | Pull-up Resistance | 2.0V | 200 | | 700 | KΩ | $V_{IN}$ = 0V; Pullups selected by mask option | |
| | | 3.6V | 50 | | 300 | KΩ | | |
| | | 5.0V | 25 | | 175 | KΩ | | |
| $I_{OL}$ | Output Leakage | 2.0-5.5 | –1 | | 1 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{CC}$ | Supply Current | 2.0V | | 1 | 3 | mA | at 8.0 MHz | 1, 2 |
| | | 3.6V | | 5 | 10 | mA | at 8.0 MHz | 1, 2 |
| | | 5.5V | | 10 | 15 | mA | at 8.0 MHz | 1, 2 |
| $I_{CC1}$ | Standby Current (HALT Mode) | 2.0V | | 0.5 | 1.6 | mA | $V_{IN}$ = 0V, Clock at 8.0MHz | 1, 2, 6 |
| | | 3.6V | | 0.8 | 2.0 | mA | $V_{IN}$ = 0V, Clock at 8.0MHz | 1, 2, 6 |
| | | 5.5V | | 1.3 | 3.2 | mA | $V_{IN}$ = 0V, Clock at 8.0MHz | 1, 2, 6 |
| $I_{CC2}$ | Standby Current (Stop Mode) | 2.0V | | 1.6 | 15 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT not Running | 3 |
| | | 3.6V | | 1.8 | 20 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT not Running | 3 |
| | | 5.5V | | 1.9 | 25 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT not Running | 3 |
| | | 2.0V | | 5 | 30 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT is Running | 3 |
| | | 3.6V | | 8 | 40 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT is Running | 3 |
| | | 5.5V | | 15 | 60 | µA | $V_{IN}$ = 0 V, $V_{CC}$ WDT is Running | 3 |
| $I_{LV}$ | Standby Current (Low Voltage) | | | 1.2 | 6 | µA | Measured at 1.3V | 4 |
| $V_{BO}$ | $V_{CC}$ Low Voltage Protection | | | 1.9 | 2.15 | V | 8MHz maximum Ext. CLK Freq. | |
| $V_{LVD}$ | $V_{CC}$ Low Voltage Detection | | | 2.4 | | V | | |

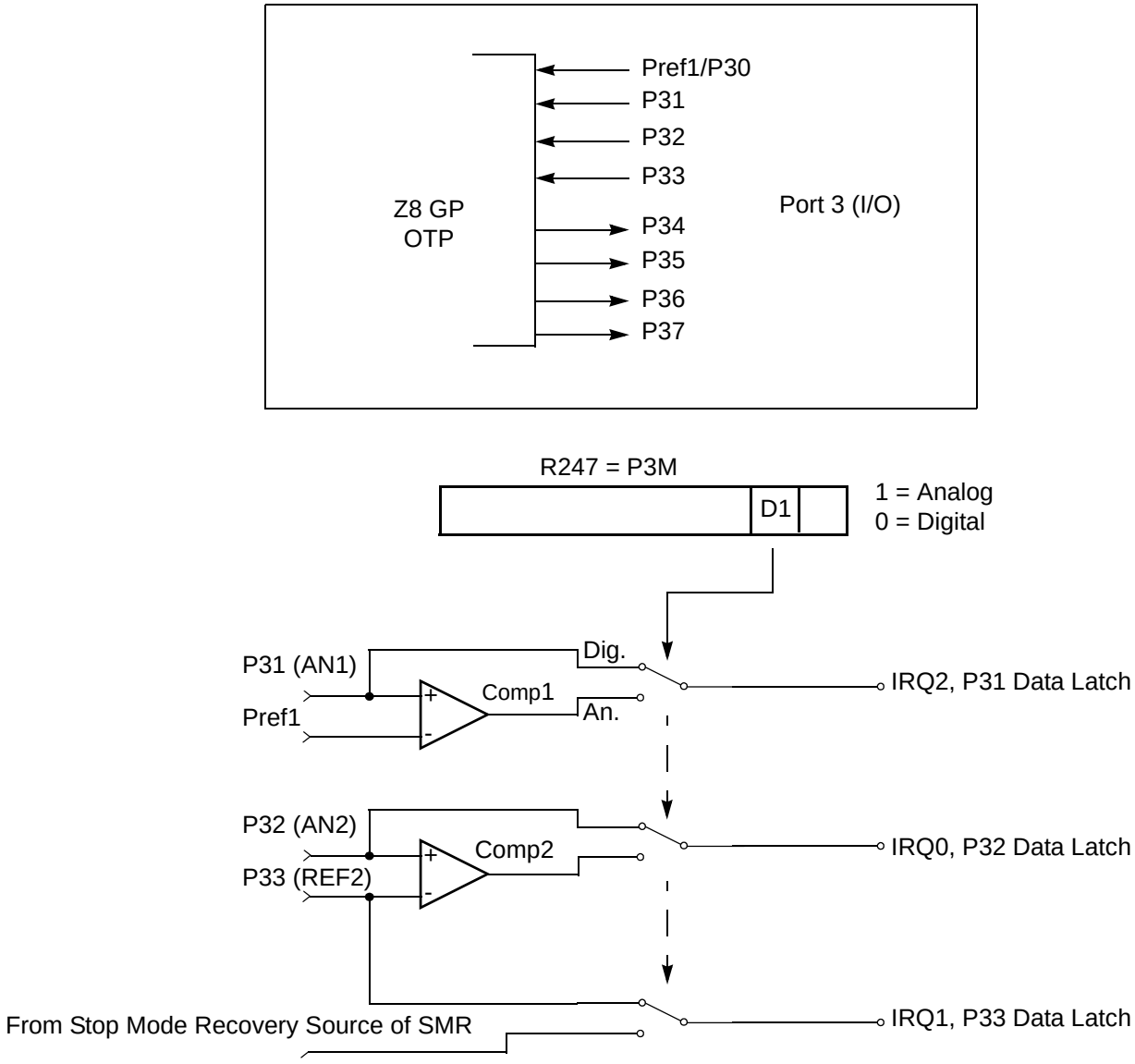



**Figure 12. Port 3 Configuration**

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “T8 and T16 Common Functions—

### Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 22. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

### Comparator Outputs

These channels can be programmed to be output on P34 and P37 through the PCON register.

## $\overline{\text{RESET}}$ (Input, Active Low)

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP asserts (Low) the $\overline{\text{RESET}}$ pin, the internal pull-up is disabled. The Z8 GP does not assert the $\overline{\text{RESET}}$ pin when under VBO.

**Note:** The external Reset does not initiate an exit from STOP mode.

# Functional Description

This device incorporates special functions to enhance the Z8®, functionality in consumer and battery-operated applications.

## Program Memory

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

## RAM

This device features 256B of RAM. See Figure 14.

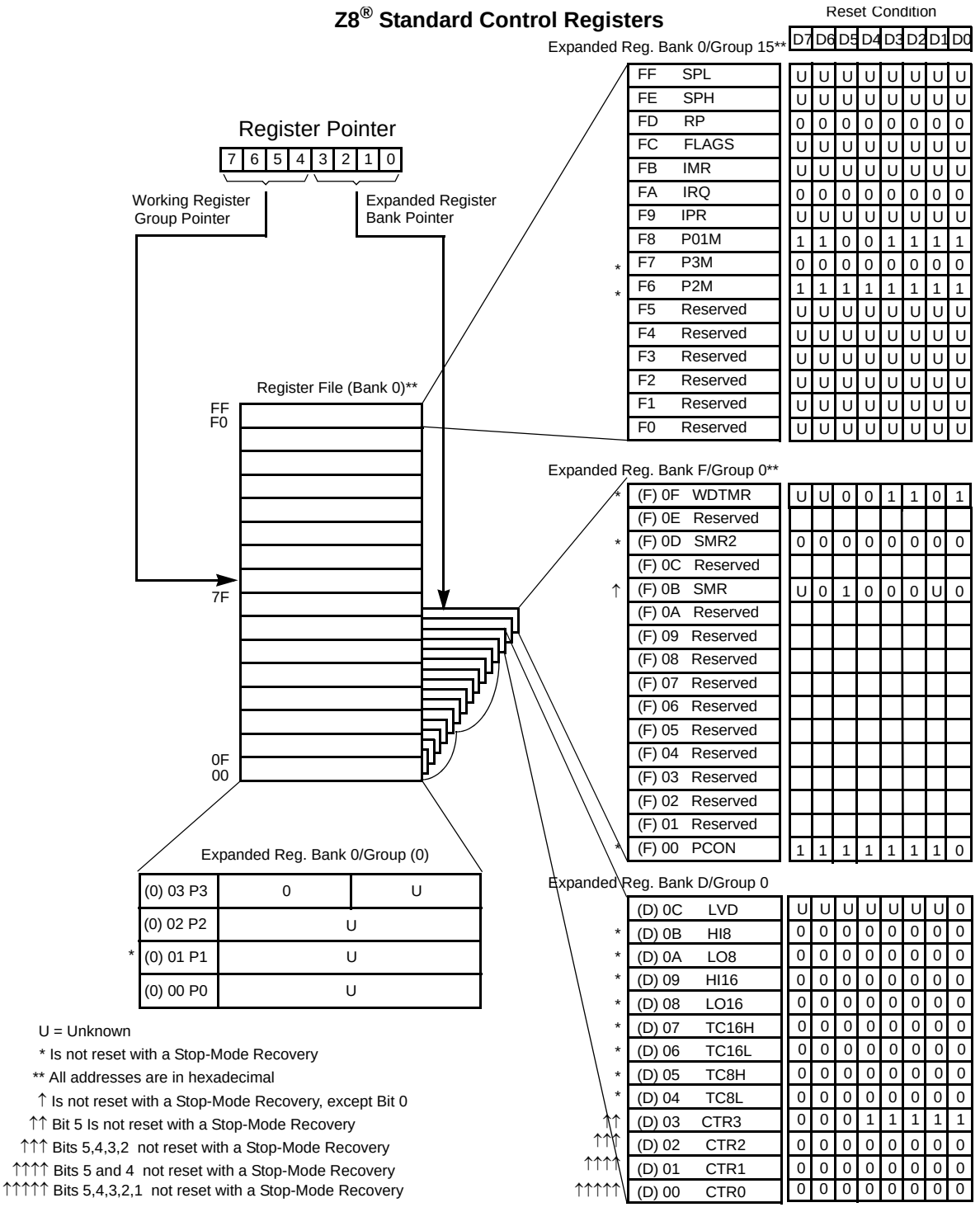



**Figure 15. Expanded Register File Architecture**

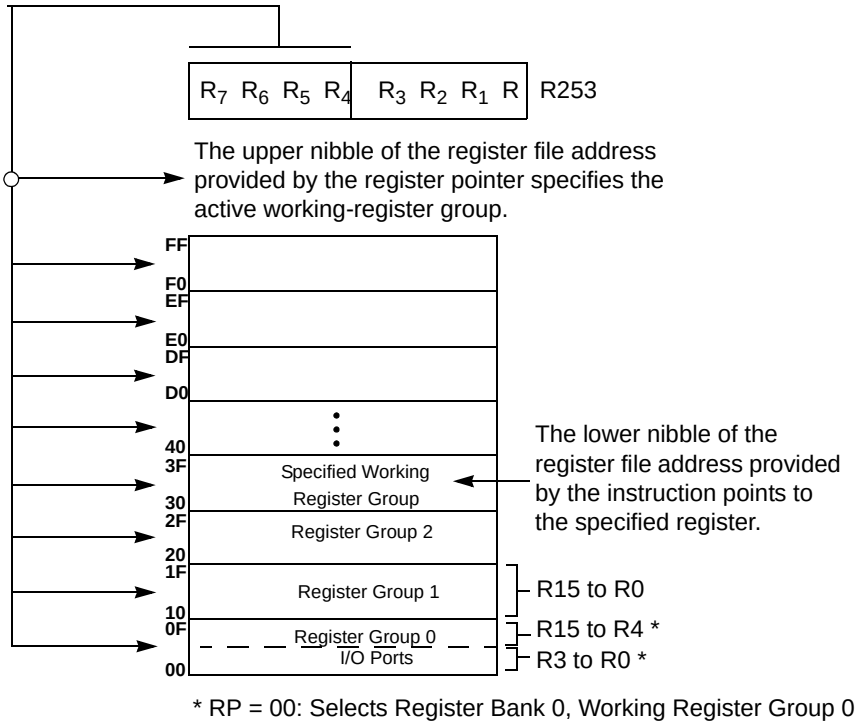



**Figure 17. Register Pointer—Detail**

## Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.

### Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

| Field | Bit Position | | Description |
|---|---|---|---|
| T16_Data_LO | [7:0] | R/W | Data |

### Counter/Timer8 High Hold Register—TC8H(D)05H

| Field | Bit Position | | Description |
|---|---|---|---|
| T8_Level_HI | [7:0] | R/W | Data |

### Counter/Timer8 Low Hold Register—TC8L(D)04H

| Field | Bit Position | | Description |
|---|---|---|---|
| T8_Level_LO | [7:0] | R/W | Data |

### CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

**Table 15. CTR0(D)00H Counter/Timer8 Control Register**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| T8_Enable | 7------- | R/W | 0*<br>1<br>0<br>1 | Counter Disabled<br>Counter Enabled<br>Stop Counter<br>Enable Counter |
| Single/Modulo-N | -6------- | R/W | 0*<br>1 | Modulo-N<br>Single Pass |
| Time_Out | --5------ | R/W | 0**<br>1<br>0<br>1 | No Counter Time-Out<br>Counter Time-Out Occurred<br>No Effect<br>Reset Flag to 0 |
| T8 _Clock | ---43--- | R/W | 0 0**<br>0 1<br>1 0<br>1 1 | SCLK<br>SCLK/2<br>SCLK/4<br>SCLK/8 |
| Capture_INT_Mask | -----2-- | R/W | 0**<br>1 | Disable Data Capture Interrupt<br>Enable Data Capture Interrupt |

### Capture_INT_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

### Counter_INT_Mask

Set this bit to allow an interrupt when T8 has a timeout.

### P34_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

### T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

**Table 16. CTR1(0D)01H T8 and T16 Common Functions**

| Field | Bit Position | | Value | Description |
|---|---|---|---|---|
| Mode | 7------- | R/W | 0* | Transmit Mode |
| | | | | Demodulation Mode |
| P36_Out/ | -6------ | R/W | | Transmit Mode |
| Demodulator_Input | | | 0* | Port Output |
| | | | 1 | T8/T16 Output |
| | | | | Demodulation Mode |
| | | | 0* | P31 |
| | | | 1 | P20 |
| T8/T16_Logic/ | --54---- | R/W | | Transmit Mode |
| Edge _Detect | | | 00** | AND |
| | | | 01 | OR |
| | | | 10 | NOR |
| | | | 11 | NAND |
| | | | | Demodulation Mode |
| | | | 00** | Falling Edge |
| | | | 01 | Rising Edge |
| | | | 10 | Both Edges |
| | | | 11 | Reserved |

**Note:** The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.

**Caution:** Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.

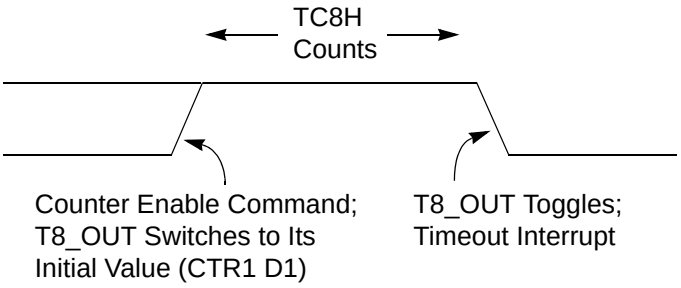



**Figure 21. T8_OUT in Single-Pass Mode**

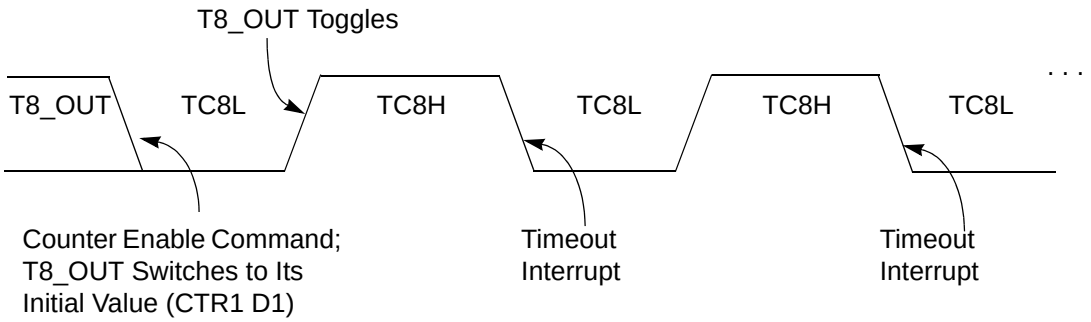



**Figure 22. T8_OUT in Modulo-N Mode**

### T8 Demodulation Mode

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put

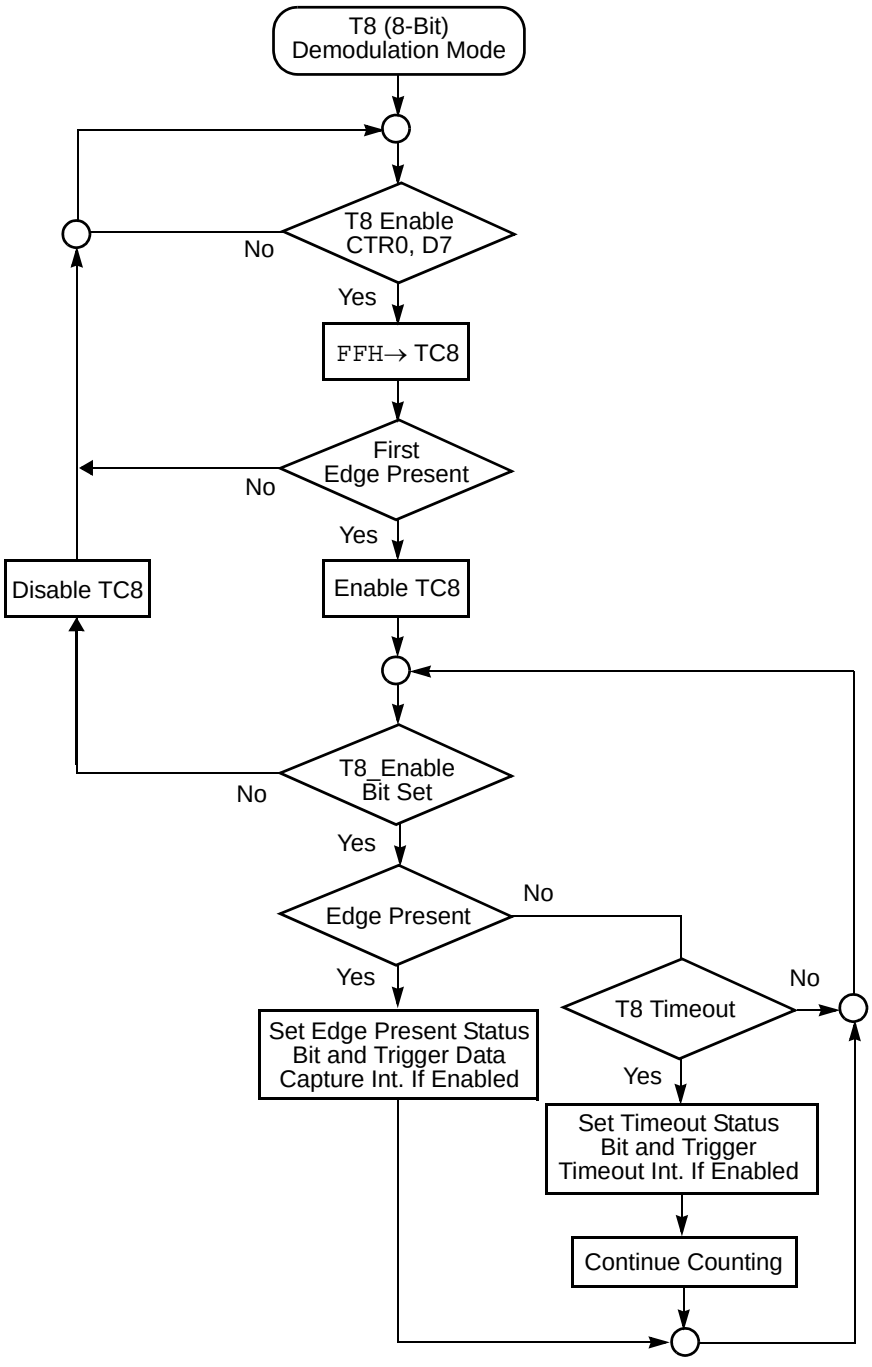
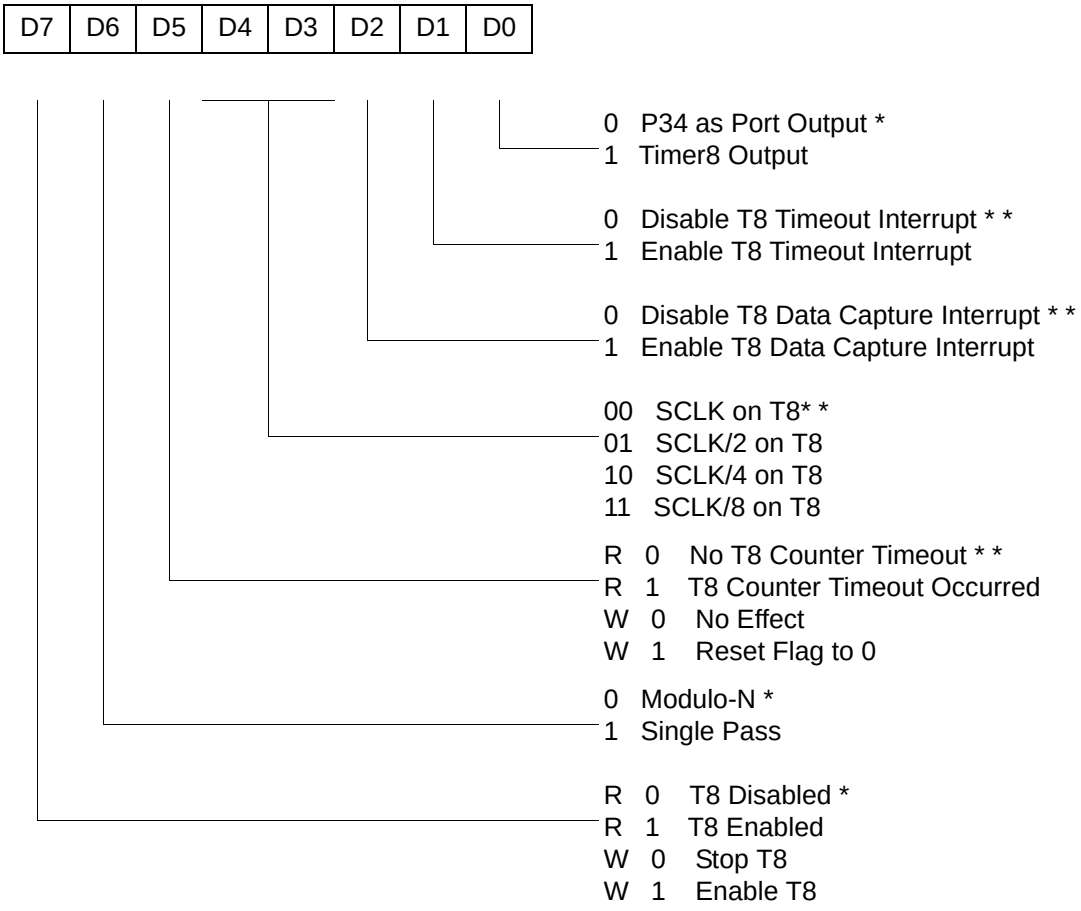



**Figure 24. Demodulation Mode Flowchart**

# Expanded Register File Control Registers (0D)

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

CTR0(0D)00H

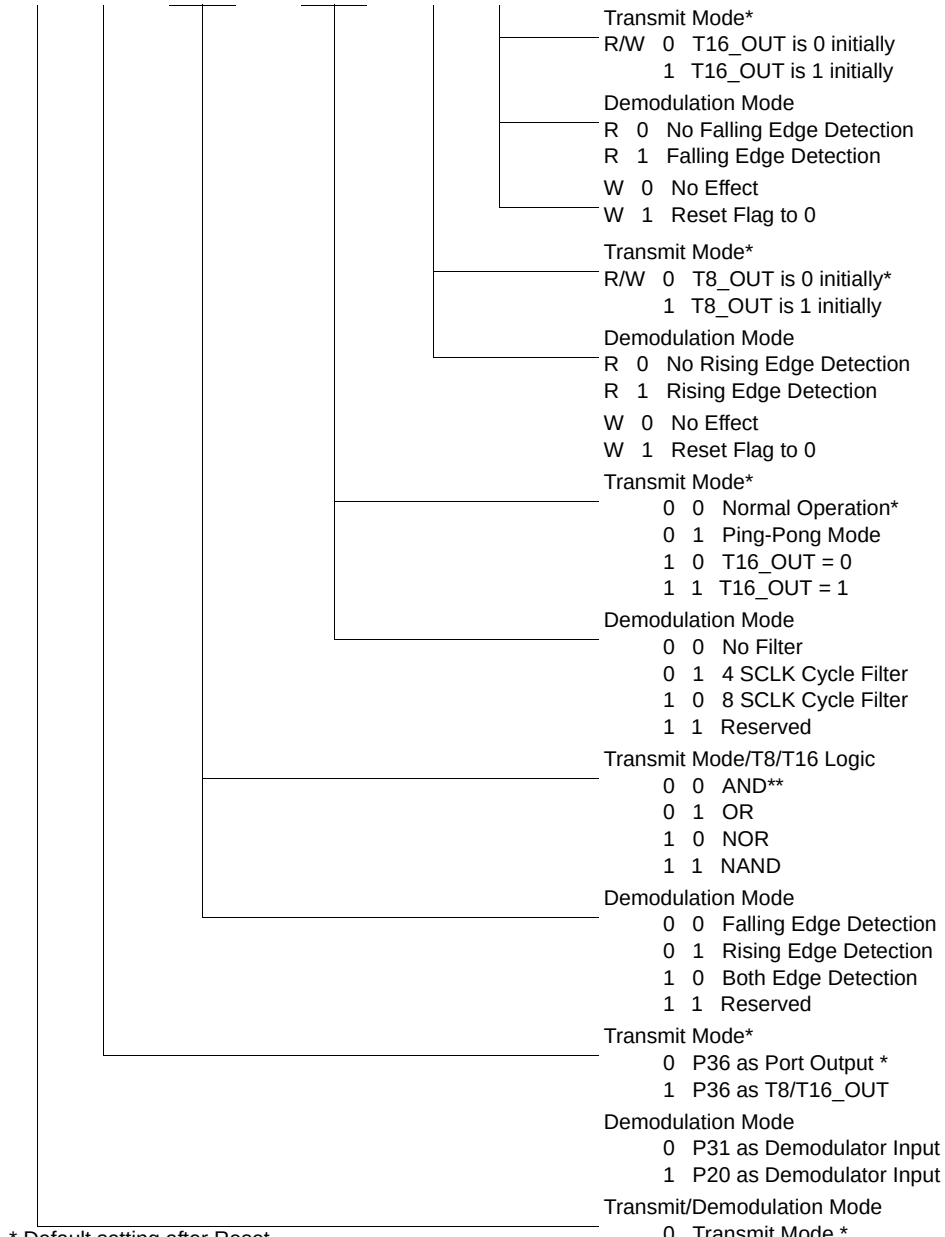



* Default setting after reset.
* * Default setting after Reset.. Not reset with a Stop-Mode recovery.

**Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)**

CTR1(0D)01H

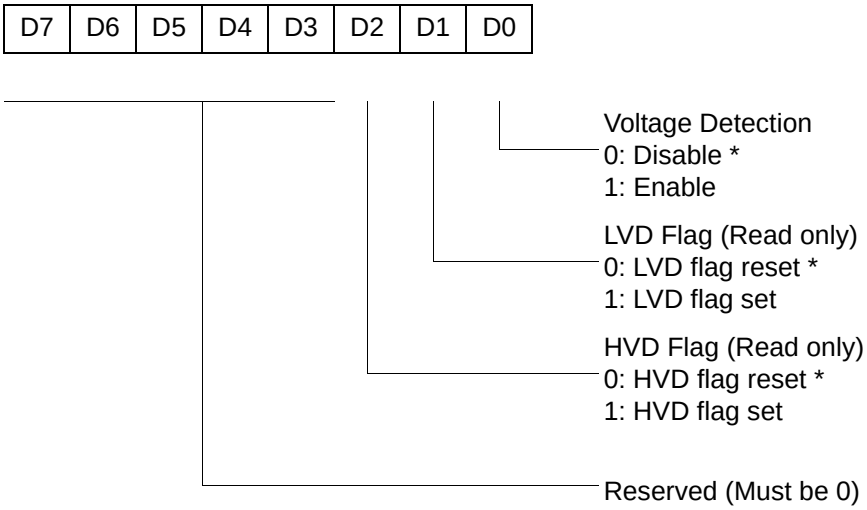
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|




* Default setting after Reset
**Default setting after Reset.. Not reset with a Stop-Mode recovery.

**Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)**

LVD(0D)0CH




* Default setting after reset.

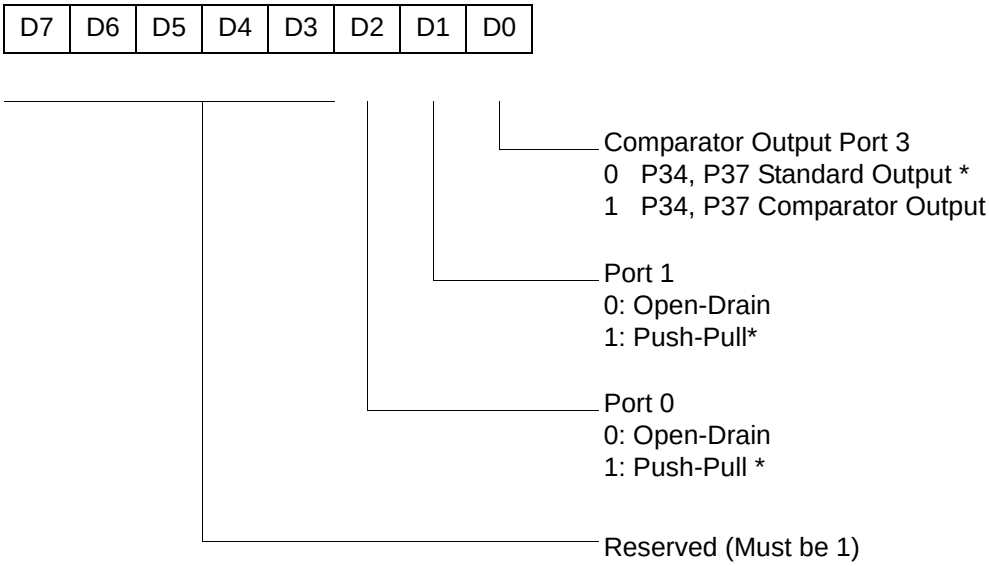
**Figure 43. Voltage Detection Register**

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

## Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.

PCON(0F)00H




* Default setting after reset

**Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)**

R254 SPH(FEH)

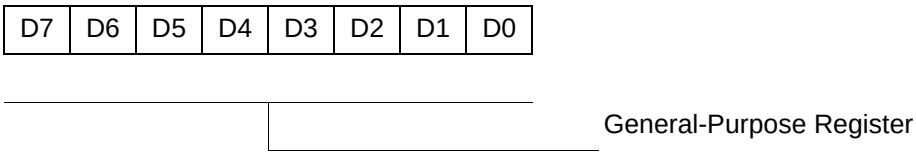



**Figure 56. Stack Pointer High (FEH: Read/Write)**

R255 SPL(FFH)

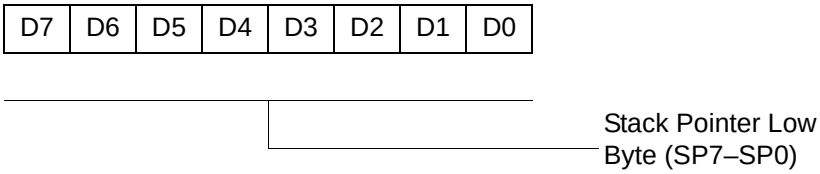
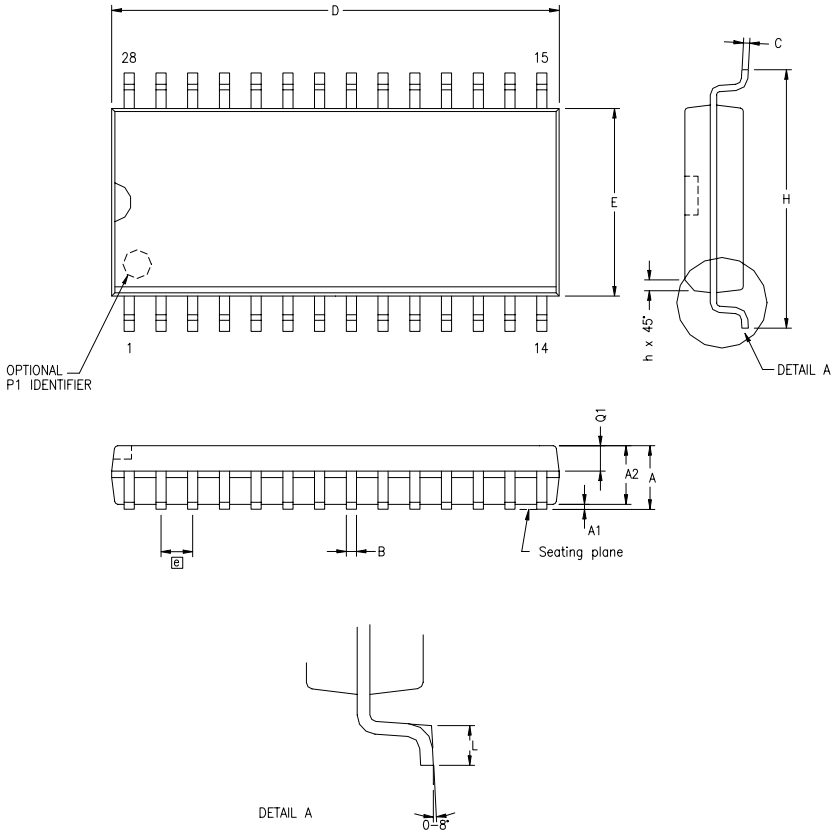



**Figure 57. Stack Pointer Low (FFH: Read/Write)**

# Package Information

Package information for all versions of ZGP323H is depicted in Figures 59 through Figure 68.




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.40 | 2.64 | .094 | .104 |
| A1 | 0.10 | 0.30 | .004 | .012 |
| A2 | 2.24 | 2.44 | .088 | .096 |
| B | 0.36 | 0.46 | .014 | .018 |
| C | 0.23 | 0.30 | .009 | .012 |
| D | 17.78 | 18.00 | .700 | .710 |
| E | 7.40 | 7.60 | .291 | .299 |
| e | 1.27 BSC | | .050 BSC | |
| H | 10.00 | 10.65 | .394 | .419 |
| h | 0.30 | 0.71 | .012 | .028 |
| L | 0.61 | 1.00 | .024 | .039 |
| Q1 | 0.97 | 1.09 | .038 | .043 |

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

**Figure 62. 28-Pin SOIC Package Diagram**

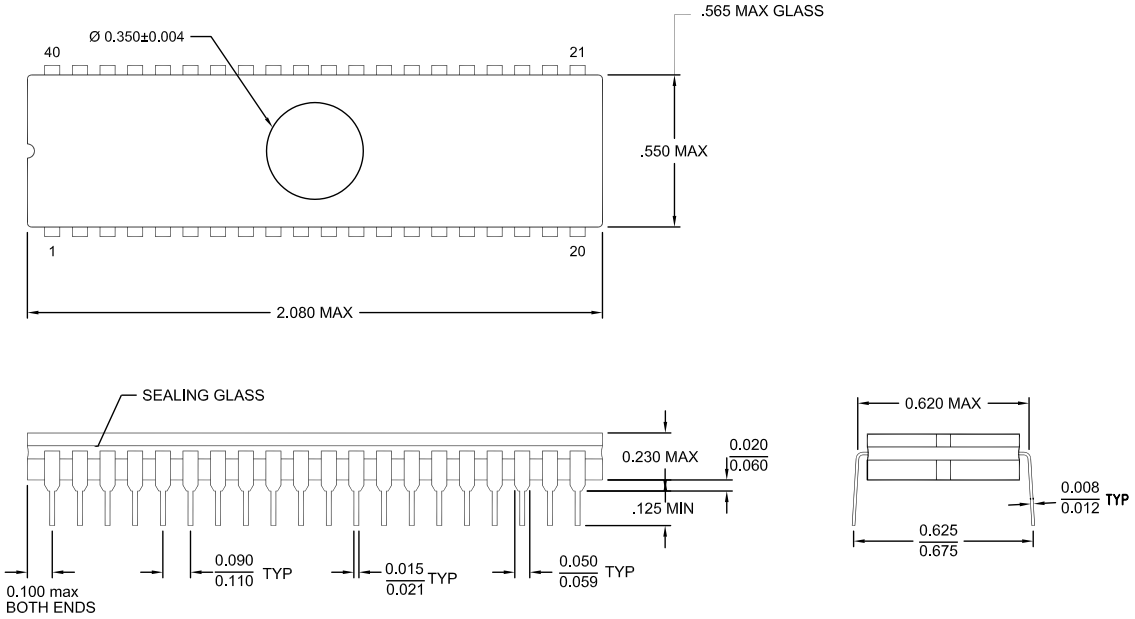



**Figure 67. 40-Pin CDIP Package Diagram**

| 16KB Standard Temperature: 0° to +70°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HSH4816C | 48-pin SSOP 16K OTP | ZGP323HSS2816C | 28-pin SOIC 16K OTP |
| ZGP323HSP4016C | 40-pin PDIP 16K OTP | ZGP323HSH2016C | 20-pin SSOP 16K OTP |
| ZGP323HSH2816C | 28-pin SSOP 16K OTP | ZGP323HSP2016C | 20-pin PDIP 16K OTP |
| ZGP323HSP2816C | 28-pin PDIP 16K OTP | ZGP323HSS2016C | 20-pin SOIC 16K OTP |

| 16KB Extended Temperature: -40° to +105°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HEH4816C | 48-pin SSOP 16K OTP | ZGP323HES2816C | 28-pin SOIC 16K OTP |
| ZGP323HEP4016C | 40-pin PDIP 16K OTP | ZGP323HEH2016C | 20-pin SSOP 16K OTP |
| ZGP323HEH2816C | 28-pin SSOP 16K OTP | ZGP323HEP2016C | 20-pin PDIP 16K OTP |
| ZGP323HEP2816C | 28-pin PDIP 16K OTP | ZGP323HES2016C | 20-pin SOIC 16K OTP |

| 16KB Automotive Temperature: -40° to +125°C | | | |
|---|---|---|---|
| **Part Number** | **Description** | **Part Number** | **Description** |
| ZGP323HAH4816C | 48-pin SSOP 16K OTP | ZGP323HAS2816C | 28-pin SOIC 16K OTP |
| ZGP323HAP4016C | 40-pin PDIP 16K OTP | ZGP323HAH2016C | 20-pin SSOP 16K OTP |
| ZGP323HAH2816C | 28-pin SSOP 16K OTP | ZGP323HAP2016C | 20-pin PDIP 16K OTP |
| ZGP323HAP2816C | 28-pin PDIP 16K OTP | ZGP323HAS2016C | 20-pin SOIC 16K OTP |
| Replace C with G for Lead-Free Packaging | | | |