



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hsp4016c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



<b>-</b> : 00		04	~
Figure 68.	48-Pin SSOP Package Design		J





Figure 2. Counter/Timers Diagram

# **Pin Description**

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.



#### Table 11. GP323HA DC Characteristics

			T <sub>A</sub> = -40°C	c to +12	5°C			
Symbol	Parameter	V <sub>CC</sub>	Min	Typ(7)	Max	Units	Conditions	Notes
V <sub>CC</sub>	Supply Voltage		2.0		5.5	V	See Note 5	5
V <sub>CH</sub>	Clock Input High Voltage	2.0-5.5	0.8 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V	Driven by External Clock Generator	
V <sub>CL</sub>	Clock Input Low Voltage	2.0-5.5	V <sub>SS</sub> –0.3		0.4	V	Driven by External Clock Generator	
V <sub>IH</sub>	Input High Voltage	2.0-5.5	0.7 V <sub>CC</sub>		V <sub>CC</sub> +0.3	V		
V <sub>IL</sub>	Input Low Voltage	2.0-5.5	V <sub>SS</sub> -0.3		0.2 V <sub>CC</sub>	V		
V <sub>OH1</sub>	Output High Voltage	2.0-5.5	V <sub>CC</sub> -0.4			V	I <sub>OH</sub> = -0.5mA	
V <sub>OH2</sub>	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	V <sub>CC</sub> -0.8			V	I <sub>OH</sub> = -7mA	
V <sub>OL1</sub>	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0 \text{mA}$	
V <sub>OL2</sub>	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	I <sub>OL</sub> = 10mA	
V <sub>OFFSET</sub>	Comparator Input Offset Voltage	2.0-5.5			25	mV		
V <sub>REF</sub>	Comparator Reference Voltage	2.0-5.5	0		V <sub>DD</sub> -1.75	V		
IIL	Input Leakage	2.0-5.5	-1		1	μA	V <sub>IN</sub> = 0V, V <sub>CC</sub> Pull-ups disabled	
R <sub>PU</sub>	Pull-up Resistance	2.0V	200		700	KΩ	V <sub>IN</sub> = 0V; Pullups selected by mask	
		3.6V	50		300	KΩ	option	
		5.0V	25		175	KΩ	_	
I <sub>OL</sub>	Output Leakage	2.0-5.5	-1		1	μΑ	$V_{IN} = 0V, V_{CC}$	
I <sub>CC</sub>	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I <sub>CC1</sub>	Standby Current	2.0V		0.5	1.6	mA	V <sub>IN</sub> = 0V, Clock at 8.0MHz	1, 2, 6
	(HALI Mode)	3.6V		0.8	2.0	mA	$V_{IN} = 0V$ , Clock at 8.0MHz	1, 2, 6
<u> </u>		5.5V		1.3	3.2	mA	$V_{IN} = 0V$ , Clock at 8.0MHz	1, 2, 6
I <sub>CC2</sub>	Standby Current (Stop	2.0V		1.6	15	μA	$V_{IN} = 0$ V, $V_{CC}$ WDT not Running	3
	Mode)	3.6V		1.8	20	μA	$V_{IN} = 0$ V, $V_{CC}$ WDT not Running	3
		5.5V		1.9	25	μΑ	$v_{IN} = 0$ V, $v_{CC}$ WDT not Running	3
		2.00		с С	30	μΑ	$v_{IN} = 0$ V, $v_{CC}$ WDT is Running	ა ი
		3.0V 5.5V		0 15	40 60	μΑ	$v_{IN} = 0.0$ , $v_{CC}$ wDT is Running	ა ვ
	Chan allow Course at	0.00		10	00	μΑ	$v_{\rm IN} = 0$ v, $v_{\rm CC}$ with the Ruthing	3
	(Low Voltage)			1.2	0	μΑ		4
V <sub>BO</sub>	V <sub>CC</sub> Low Voltage Protection			1.9	2.15	V	8MHz maximum Ext. CLK Freq.	
V <sub>LVD</sub>	V <sub>CC</sub> Low Voltage Detection			2.4		V		







#### Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—



# 25

#### **Comparator Inputs**

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 12 on page 22. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.



**Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery source, these inputs must be placed into digital mode.

#### **Comparator Outputs**

These channels can be programmed to be output on P34 and P37 through the PCON register.

### **RESET (Input, Active Low)**

Reset initializes the MCU and is accomplished either through Power-On, Watch-Dog Timer, Stop Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line must be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

When the Z8 GP asserts (Low) the  $\overline{\text{RESET}}$  pin, the internal pull-up is disabled. The Z8 GP does not assert the  $\overline{\text{RESET}}$  pin when under VBO.



**Note:** The external Reset does not initiate an exit from STOP mode.

# **Functional Description**

This device incorporates special functions to enhance the Z8<sup>®</sup>, functionality in consumer and battery-operated applications.

#### **Program Memory**

This device addresses up to 32KB of OTP memory. The first 12 Bytes are reserved for interrupt vectors. These locations contain the six 16-bit vectors that correspond to the six available interrupts.

#### RAM

This device features 256B of RAM. See Figure 14.





Expanded Reg. Bank 0/Group 15"         Register Pointer         [7] [5] [4] [3] [2] [10]         Working Register         Group Pointer         Bank Pointer         FF         FP         Bank Pointer         FF         FP         Bank Pointer         FF         FF         FF         FF         Bank Pointer         FF          FF		Z8 <sup>®</sup> Standard	Control Registers	Res	et C	Cond	itior	۱
Register Pointer       FF       SPL FE       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U <thu< th=""> <thu< th="">       U       U</thu<></thu<>			Expanded Reg. Bank 0/Group 15	** D7 D6 D	5 D4	D3	D2[	D1 D0
Register Pointer       Image: Construction of the second of					1	ii		
Register Pointer       T       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D       D								
Register Pointer         U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       <			FD RP		0	0	0	
7       6       5       4       3       2       1       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0		Register Pointer	FC FLAGS					
Working Register Group Pointer       Expanded Register Bank Pointer       FA       IRQ       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0 <td< td=""><td>7</td><td>7 6 5 4 3 2 1 0</td><td>FB IMB</td><td></td><td></td><td></td><td></td><td></td></td<>	7	7 6 5 4 3 2 1 0	FB IMB					
Working Register       Expanded Register       F3       F3 <td></td> <td></td> <td>FA IBO</td> <td></td> <td>0</td> <td>0</td> <td>0</td> <td></td>			FA IBO		0	0	0	
Ordop Pollies       Dirth Antes         PB       PD1M       1       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0 <t< td=""><td>Working Regist</td><td>ter Expanded Regist</td><td>er F9 IPR</td><td></td><td></td><td></td><td></td><td></td></t<>	Working Regist	ter Expanded Regist	er F9 IPR					
F7       P3M       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0	Group Pointer	Dank Fonter	F8 P01M	1 1 0	0	1	1	1 1
F6       P2M       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1			F7 P3M		0	0	0	0 0
F5       Reserved       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I       I			F6 P2M	1 1 1	1	1	1	1 1
F4       Reserved         F3       Reserved         F3       Reserved         F4       Reserved         F5       Reserved         F6       F6         F6       F7         F7       F8         F8       F8         F7       F8         F8       F8         F9       F8 <td></td> <td></td> <td>F5 Reserved</td> <td></td> <td></td> <td><math>\frac{1}{1}</math></td> <td>ii l</td> <td></td>			F5 Reserved			$\frac{1}{1}$	ii l	
Fig       Reserved       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U			F4 Reserved			11	<del>U</del>	
File       (Bank 0)**       File       (Bank 0)**       File       (Bank 0)**         File       Reserved       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U			F3 Reserved		U U	U	U	
Findersterning (bank 0)**       Findersterning (bank 0)**			F2 Reserved		U U	U	Ŭ	
F0       Reserved       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U       U	FF	Register File (Bank 0)	F1 Reserved		U U	Ŭ	U	υυ
Image: Second State Sta	Fo		F0 Reserved		U U	Ŭ	U	
Figure 1       Expanded Reg. Bank F/Group 0**         (F) 0F       WD 1MR         (F) 0F       WD 1MR         (F) 0F       Reserved         (F) 0F       Reserved         (F) 0R       Reserved						1-1	~	
Image: constraint of the second state stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop-Mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the stop mode Recovery         Image: constraint of the stop-Mode Recovery       Image: constraint of the			Expanded Reg. Bank F/Group 0*	*				
(F) 0E Reserved       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0			(F) 0F WDTMR	U U O	0	1	1	0 1
F) OD SMR2       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0			(F) 0E Reserved			Π		
7F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F       F			* (F) 0D SMR2	0 0 0	0	0	0	0 0
7F       (F) 0B SMR       U 0 1 0 0 0 U 0         (F) 0B Reserved       (F) 0B Reserved       (F) 0B Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved       (F) 0F Reserved       (F) 0F Reserved         (F) 0F Reserved </td <td>_</td> <td></td> <td>(F) 0C Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	_		(F) 0C Reserved					
(F) 0A Reserved       (F) 09 Reserved         (F) 06 Reserved       (F) 06 Reserved         (F) 07 Reserved       (F) 06 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 09 Reserved       (F) 07 Reserved         (F) 00 Reserved       (F) 00 Reserved         (D) 00 C LVD       (D) 0 0 0 0 0 0 0 0	7F	· ↓	↑ (F) 0B SMR	U 0 1	0	0	0	U 0
(F) 09       Reserved         (F) 07       Reserved         (F) 08       Reserved         (F) 07       Reserved         (F) 07       Reserved         (F) 08       Reserved         (F) 07       Reserved         (F) 08       Reserved         (F) 07       Reserved         (F) 08       Reserved         (F) 01       Reserved         (F) 02       Reserved         (F) 01       Reserved         (F) 02       Reserved         (F) 01       Reserved         (F) 01       Reserved         (F) 01       Reserved         (F) 01       Reserved         (F) 02       Reserved         (F) 03       Reserved         (F) 04       Reserved         (F) 01       Reserved		<b>_</b>	(F) 0A Reserved			Π		
(F) 08 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 07 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 08 Reserved       (F) 07 Reserved         (F) 00 PCON       (F) 01 Reserved         (O) 01 P1       U         (O) 00 P0       U         U = Unknown       (D) 00 C T16L         * 18 not reset with a Stop-Mode Recovery         * 111 Bits 5,4,3,2 not reset with a Stop-Mode Recovery         * 111 Bits 5,4,3,2,2 not reset with a			(F) 09 Reserved					
0F       (F) 07 Reserved       (F) 06 Reserved         (F) 06 Reserved       (F) 05 Reserved         (F) 07 Reserved       (F) 04 Reserved         (F) 07 Reserved       (F) 04 Reserved         (F) 03 Reserved       (F) 04 Reserved         (F) 03 Reserved       (F) 04 Reserved         (F) 03 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 04 Reserved         (F) 02 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 04 Reserved         (F) 02 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 04 Reserved         (F) 02 Reserved       (F) 04 Reserved         (F) 04 Reserved       (F) 04 Reserved			(F) 08 Reserved					
0F       (F) 06 Reserved       (F) 05 Reserved         (F) 04 Reserved       (F) 04 Reserved         (F) 03 Reserved       (F) 04 Reserved         (F) 02 Reserved       (F) 04 Reserved         (F) 03 Reserved       (F) 04 Reserved         (F) 01 Reserved       (F) 01 Reserved         (F) 02 Reserved       (F) 01 Reserved         (F) 02 Reserved       (F) 01 Reserved         (F) 01 Reserved       (F) 01 Reserved         (F) 02 Reserved       (F) 01 Reserved         (F) 02 Reserved       (F) 01 Reserved         (F) 03 P3 0       (F) 01 Reserved         (F) 00 PCON       (F) 01 Reserved         (F) 01 Reserved       (F) 01 Reserved         (F) 02 Reserved       (F) 01 Reserved         (F) 00 PCON       (F) 01 Reserved         (F) 01 P1       (F) 01 Reserved         (D) 02 P2       (F) 00 PCON         (F) 03 B Hil8       (F) 00 0 0 0 0 0 0 0         (D) 04 LO8       (F) 00 0 0 0 0 0         (F) 03 B LO16       (F) 00 0 0 0 0 0         (F) 04 C LD8       (F) 00 0 0 0 0 0         (D) 05 TC8H       (F) 00 0 0 0 0 0         (F) 03 C TR3       (F) 0 0 0 0 0 0         (F) 04 TC8L       (F) 0 0 0 0 0 0         (F) 04 C C R2<			(F) 07 Reserved					
0F       0F <td< td=""><td></td><td></td><td>(F) 06 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 06 Reserved					
0F       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00       00 <td< td=""><td></td><td></td><td>(F) 05 Reserved</td><td></td><td></td><td></td><td></td><td></td></td<>			(F) 05 Reserved					
00       Image: constraint of the set with a Stop-Mode Recovery         1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1 <td>0F</td> <td><u> </u>₩/</td> <td>(F) 04 Reserved</td> <td></td> <td></td> <td></td> <td></td> <td></td>	0F	<u> </u> ₩/	(F) 04 Reserved					
Expanded Reg. Bank 0/Group (0)       (F) 02 Reserved       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1	00		(F) 03 Reserved					
Expanded Reg. Bank 0/Group (0)         (0) 03 P3       0         (0) 02 P2       U         (0) 01 P1       U         (0) 01 P1       U         (0) 00 P0       U         U = Unknown         * Is not reset with a Stop-Mode Recovery         ** All addresses are in hexadecimal         ↑ Is not reset with a Stop-Mode Recovery         ** All addresses are in hexadecimal         ↑ Is not reset with a Stop-Mode Recovery         ** Di 03 CTR3       0         ** (D) 04 TC8L       0         0       0         ** (D) 03 CTR3       0         ** (D) 04 TC8L       0         0       0         ** (D) 02 CTR2       0         ** (D) 04 TC8L       0         0       0         ** (D) 02 CTR2       0         ** (D) 04 TC8L       0         0       0         ** (D) 02 CTR2       0         ** (D) 01 CTR1       0         ** (D) 00 CTR0       0		$\backslash$	(F) 02 Reserved					
Expanded Reg. Bank 0/Group (0)         (0) 03 P3       0       U         (0) 02 P2       U         *       (0) 01 P1       U         (0) 00 P0       U         (0) 00 P0       U         U = Unknown         * Is not reset with a Stop-Mode Recovery         ** All addresses are in hexadecimal         ↑ Is not reset with a Stop-Mode Recovery         ** His 5 Is not reset with a Stop-Mode Recovery         ** (D) 04 TC8L       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       <			(F) 01 Reserved					
(0) 03 P3       0       U         (0) 02 P2       U         * (0) 01 P1       U         (0) 00 P0       U         * (0) 00 P0       U         U = Unknown         * Is not reset with a Stop-Mode Recovery         ** All addresses are in hexadecimal         ^* (D) 05 TC8H       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0	Expa	anded Reg. Bank 0/Group (0)	(F) 00 PCON	1 1 1	1	1	1	1 0
(0) 03 P3       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0			Expanded Reg. Bank D/Group 0					
(b) 02 P2       U         *       (0) 01 P1       U         (0) 00 P0       U         U = Unknown       *         * All addresses are in hexadecimal       *         ↑ Bit 5 Is not reset with a Stop-Mode Recovery         **       (D) 04         **       (D) 05         **       (D) 06         **       (D) 07         **       (D) 08         **       (D) 08         **       (D) 07         **       (D) 08         **       (D) 07         **       (D) 06         **       (D) 06         **       (D) 07         **       (D) 06         **       (D) 07         **       (D) 08         **       (D) 08         **       (D) 04         **       (D) 05         **       (D) 04         **       (D) 03         **       (D) 02         **       (D) 01         **       (D) 01         **       (D) 01         **       (D) 01         **       (D) 02         **       (D) 01       (D) 0	(0) 03 P3	U U		UUI	υ	U	U	υn
*       (0) 01 P1       U         (0) 01 P1       U         (0) 00 P0       U         *       (D) 00 A LO8       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0<	(0) 02 P2	U	* (D) 0B HI8	0 0 0	0	0	0	0 0
(b) 01 1 1       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0	* (0) 01 P1	U	* (D) 0A   08	0 0 0	0	0	0	0 0
(0) 00 P0       U         U = Unknown       (D) 08 LO16       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0	(0) 011 1	<u> </u>	* (D) 09 HI16	0 0 0	0	0	0	0 0
U = Unknown       *       (D) 07 TC16H       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0 <td>(0) 00 P0</td> <td>U</td> <td>* (D) 08 LO16</td> <td>0 0 0</td> <td>0</td> <td>0</td> <td>0</td> <td>0 0</td>	(0) 00 P0	U	* (D) 08 LO16	0 0 0	0	0	0	0 0
* Is not reset with a Stop-Mode Recovery         ** All addresses are in hexadecimal         ^* All addresses are in hexadecimal         ^* Is not reset with a Stop-Mode Recovery, except Bit 0         ^* Bit 5 Is not reset with a Stop-Mode Recovery         ^* Bit 5 Is not reset with a Stop-Mode Recovery         ^* Bit 5 Js not reset with a Stop-Mode Recovery         ^* Bit 5 Js not reset with a Stop-Mode Recovery         ^* Bit 5 Js not reset with a Stop-Mode Recovery         ^* Diss 5,4,3,2 not reset with a Stop-Mode Recovery         ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery         ^* CD 00 CTR1         0       0         ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery         ^* CD 00 CTR0         ^* Diss 5,4,3,2,1 not reset with a Stop-Mode Recovery			* (D) 07 TC16H	0 0 0	0	0	0	0 0
*** All addresses are in hexadecimal       *       (D) 05 TC8H       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0       0 <t< td=""><td>* Is not reset with a Ston-Mor</td><td>de Recoverv</td><td>* (D) 06 TC16L</td><td>0 0 0</td><td>0</td><td>0</td><td>0</td><td>0 0</td></t<>	* Is not reset with a Ston-Mor	de Recoverv	* (D) 06 TC16L	0 0 0	0	0	0	0 0
<sup>+</sup> Is not reset with a Stop-Mode Recovery, except Bit 0 <sup>+</sup> 1bit 5 Is not reset with a Stop-Mode Recovery <sup>+</sup> (D) 04 TC8L <sup>-</sup> 0 0 0 0 0 0 0 0 0 0 0 <sup>+</sup> (D) 03 CTR3 <sup>-</sup> 0 0 0 0 1 1 1 1 1 <sup>+</sup> 1 <sup>+</sup> (D) 02 CTR2 <sup>-</sup> 0 0 0 0 0 0 0 0 0 <sup>-</sup> 1 1 1 1 <sup>+</sup>	** All addresses are in beyade	ecimal	* (D) 05 TC8H	0 0 0	0	0	0	0 0
	↑ Is not reset with a Stop-Mo	de Recovery, except Bit 0	* (D) 04 TC8L	0 0 0	0	0	0	0 0
<sup>↑</sup> ↑↑ Bits 5,4,3,2 not reset with a Stop-Mode Recovery <sup>↑</sup> ↑↑↑ <sup>↑</sup> ↑↑↑ <sup>↑</sup> ↑↑↑ <sup>↑</sup> ↑↑↑↑ <sup>↑</sup> ↑↑↑ <sup>↑</sup> ↑↑ <sup>↑</sup> ↑ <sup>↑</sup>	↑↑ Bit 5 Is not reset with a Sto	p-Mode Recovery	1↑ (D) 03 CTR3	0 0 0	1	1	1	1 1
<sup>↑↑↑↑</sup> Bits 5 and 4 not reset with a Stop-Mode Recovery <sup>↑↑↑↑↑</sup> (D) 01 CTR1         (D) 01 CTR1         (D) 0 0 0 0 0 0 0 0         (D) 01 CTR1         (D) 00 CTR0         (D)	↑↑↑ Bits 5,4,3.2 not reset with	a Stop-Mode Recoverv	↑↑↑ (D) 02 CTR2	0 0 0	0	0	0	0 0
↑↑↑↑↑ Bits 5,4,3,2,1 not reset with a Stop-Mode Recovery ↑↑↑↑↑↓ (D) 00 CTR0 0 0 0 0 0 0 0 0 0 0	↑↑↑↑ Bits 5 and 4 not reset with	a Stop-Mode Recovery	↑↑↑↑ (D) 01 CTR1	0 0 0	0	0	0	0 0
	↑↑↑↑↑ Bits 5,4,3,2,1 not reset wit	th a Stop-Mode Recovery	↑↑↑↑↑ (D) 00 CTR0	0 0 0	0	0	0	0 0

#### Figure 15. Expanded Register File Architecture







Figure 17. Register Pointer—Detail

#### Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



#### 33

#### Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position	Description	
T16_Data_LO	[7:0]	R/W	Data

#### Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position	Description	
T8_Level_HI	[7:0]	R/W	Data

#### Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position		Description
T8_Level_LO	[7:0]	R/W	Data

#### CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

Table 15. CTR0(D)00H Counter/Timera	<b>3 Control Register</b>
-------------------------------------	---------------------------

Field	<b>Bit Position</b>		Value	Description
T8_Enable	7	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6	R/W	0*	Modulo-N
-			1	Single Pass
Time_Out	5	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8 _Clock	43	R/W	0 0**	SCLK
			0 1	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	2	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt



#### 35

#### Capture\_INT\_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

#### Counter\_INT\_Mask

Set this bit to allow an interrupt when T8 has a timeout.

#### P34\_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

#### T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Mode	7	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/	-6	R/W		Transmit Mode
Demodulator_Input			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0*	P31
			1	P20
T8/T16_Logic/	54	R/W		Transmit Mode
Edge _Detect			00**	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

#### Table 16. CTR1(0D)01H T8 and T16 Common Functions



Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.



**Caution:** Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.







Figure 22. T8\_OUT in Modulo-N Mode

#### **T8 Demodulation Mode**

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put







Figure 24. Demodulation Mode Flowchart



# **Expanded Register File Control Registers (0D)**

The expanded register file control registers (0D) are depicted in Figure 39 through Figure 43.

#### CTR0(0D)00H

D7	D6	D5	D4	D3	D2	D1	D0	
								<ul> <li>0 P34 as Port Output *</li> <li>1 Timer8 Output</li> <li>0 Disable T8 Timeout Interrupt * *</li> <li>1 Enable T8 Timeout Interrupt</li> <li>0 Disable T8 Data Capture Interrupt * *</li> <li>1 Enable T8 Data Capture Interrupt * *</li> <li>1 Enable T8 Data Capture Interrupt</li> <li>00 SCLK on T8* *</li> <li>00 SCLK on T8* *</li> <li>01 SCLK/2 on T8</li> <li>10 SCLK/4 on T8</li> <li>11 SCLK/8 on T8</li> <li>R 0 No T8 Counter Timeout * *</li> <li>R 1 T8 Counter Timeout Occurred</li> <li>W 0 No Effect</li> <li>W 1 Reset Flag to 0</li> <li>0 Modulo-N *</li> <li>1 Single Pass</li> <li>R 0 T8 Disabled *</li> <li>R 1 T8 Enabled</li> <li>W 0 Stop T8</li> <li>W 4 Enable T9</li> </ul>
								VV I ETIADIE IO

\* Default setting after reset.

\* \* Default setting after Reset.. Not reset with a Stop-Mode recovery.

#### Figure 39. TC8 Control Register ((0D)O0H: Read/Write Except Where Noted)





СП	R1(0L	))01H							
D7	D6	D5	D4	D3	D2	D1	D0		
									Transmit Mode* R/W 0 T16_OUT is 0 initially 1 T16_OUT is 1 initially Demodulation Mode R 0 No Falling Edge Detection R 1 Falling Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* R/W 0 T8_OUT is 0 initially* 1 T8_OUT is 1 initially Demodulation Mode R 0 No Rising Edge Detection R 1 Rising Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* 0 0 Normal Operation* 0 1 Ping-Pong Mode 1 0 T16_OUT = 0 1 1 T16_OUT = 1 Demodulation Mode 0 0 No Filter 0 1 4 SCLK Cycle Filter 1 0 8 SCLK Cycle Filter 1 0 R SCLK Cycle Filter 1 0 NOR 1 0 NOR 1 1 NAND Demodulation Mode 0 0 0 Falling Edge Detection
									<ul> <li>0 0 Falling Edge Detection</li> <li>0 1 Rising Edge Detection</li> <li>1 0 Both Edge Detection</li> <li>1 1 Reserved</li> <li>Transmit Mode*</li> </ul>
	L								0 P36 as Port Output * 1 P36 as T8/T16_OUT Demodulation Mode 0 P31 as Demodulator Input 1 P20 as Demodulator Input
* De **De recc	efault se efault se overy.	etting after etting aft	er Res er Res	et et Not	reset v	with a S	Stop-N	lode	Transmit/Demodulation Mode 0 Transmit Mode * 1 Demodulation Mode

Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)



#### LVD(0D)0CH



\* Default setting after reset.

#### Figure 43. Voltage Detection Register

**Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

# **Expanded Register File Control Registers (0F)**

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.



#### PCON(0F)00H



\* Default setting after reset

Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only)



#### R254 SPH(FEH)



#### Figure 56. Stack Pointer High (FEH: Read/Write)

#### R255 SPL(FFH)



Stack Pointer Low Byte (SP7–SP0)

Figure 57. Stack Pointer Low (FFH: Read/Write)

## **Package Information**

Package information for all versions of ZGP323H is depicted in Figures 59 through Figure 68.







Figure 62. 28-Pin SOIC Package Diagram





Figure 67. 40-Pin CDIP Package Diagram



#### 16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4816C	48-pin SSOP 16K OTP	ZGP323HSS2816C	28-pin SOIC 16K OTP
ZGP323HSP4016C	40-pin PDIP 16K OTP	ZGP323HSH2016C	20-pin SSOP 16K OTP
ZGP323HSH2816C	28-pin SSOP 16K OTP	ZGP323HSP2016C	20-pin PDIP 16K OTP
ZGP323HSP2816C	28-pin PDIP 16K OTP	ZGP323HSS2016C	20-pin SOIC 16K OTP

16KB Extended Temperature: -40° to +105°C				
Part Number	Description	Part Number	Description	
ZGP323HEH4816C	48-pin SSOP 16K OTP	ZGP323HES2816C	28-pin SOIC 16K OTP	
ZGP323HEP4016C	40-pin PDIP 16K OTP	ZGP323HEH2016C	20-pin SSOP 16K OTP	
ZGP323HEH2816C	28-pin SSOP 16K OTP	ZGP323HEP2016C	20-pin PDIP 16K OTP	
ZGP323HEP2816C	28-pin PDIP 16K OTP	ZGP323HES2016C	20-pin SOIC 16K OTP	

# 16KB Automotive Temperature: -40° to +125°CPart NumberDescriptionPart NumberDescriptionZGP323HAH4816C48-pin SSOP 16K OTPZGP323HAS2816C28-pin SOIC 16K OTPZGP323HAP4016C40-pin PDIP 16K OTPZGP323HAH2016C20-pin SSOP 16K OTPZGP323HAH2816C28-pin SSOP 16K OTPZGP323HAP2016C20-pin PDIP 16K OTPZGP323HAP2816C28-pin PDIP 16K OTPZGP323HAS2016C20-pin SOIC 16K OTPZGP323HAP2816C28-pin PDIP 16K OTPZGP323HAS2016C20-pin SOIC 16K OTPReplace C with G for Lead-Free Packaging

#### ZGP323H Z8<sup>®</sup> OTP Microcontroller with IR Timers



28-pin DIP/SOIC/SSOP 6 40- and 48-pin 8 40-pin DIP 7 48-pin SSOP 8 pin functions port 0 (P07 - P00) 18 port 0 (P17 - P10) 19 port 0 configuration 19 port 1 configuration 20 port 2 (P27 - P20) 20 port 2 (P37 - P30) 21 port 2 configuration 21 port 3 configuration 22 port 3 counter/timer configuration 24 reset) 25 XTAL1 (time-based input 18 XTAL2 (time-based output) 18 ping-pong mode 48 port 0 configuration 19 port 0 pin function 18 port 1 configuration 20 port 1 pin function 19 port 2 configuration 21 port 2 pin function 20 port 3 configuration 22 port 3 pin function 21 port 3counter/timer configuration 24 port configuration register 55 power connections 3 power supply 5 program memory 25 map 26 R ratings, absolute maximum 10 register 61 CTR(D)01h 35 CTR0(D)00h 33 CTR2(D)02h 37 CTR3(D)03h 39 flag 80 HI16(D)09h 32

HI8(D)0Bh 32 interrupt priority 78 interrupt request 79 interruptmask 79 L016(D)08h 32 L08(D)0Ah 32 LVD(D)0Ch 65 pointer 80 port 0 and 1 77 port 2 configuration 75 port 3 mode 76 port configuration 55, 75 SMR2(F)0Dh 40 stack pointer high 81 stack pointer low 81 stop mode recovery 57 stop mode recovery 2 61 stop-mode recovery 73 stop-mode recovery 274 T16 control 69 T8 and T16 common control functions 67 T8/T16 control 70 TC16H(D)07h 32 TC16L(D)06h 33 TC8 control 66 TC8H(D)05h 33 TC8L(D)04h 33 voltage detection 71 watch-dog timer 75 register description Counter/Timer2 LS-Byte Hold 33 Counter/Timer2 MS-Byte Hold 32 Counter/Timer8 Control 33 Counter/Timer8 High Hold 33 Counter/Timer8 Low Hold 33 CTR2 Counter/Timer 16 Control 37 CTR3 T8/T16 Control 39 Stop Mode Recovery2 40 T16 Capture LO 32 T8 and T16 Common functions 35 T8\_Capture\_HI 32