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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323hss2004c00tr">https://www.e-xfl.com/product-detail/zilog/zgp323hss2004c00tr</a>



Figure 34. SCLK Circuit .....	58
Figure 35. Stop Mode Recovery Source .....	59
Figure 36. Stop Mode Recovery Register 2 ((0F)DH:D2–D4, D6 Write Only) ..	61
Figure 37. Watch-Dog Timer Mode Register (Write Only) .....	62
Figure 38. Resets and WDT .....	63
Figure 39. TC8 Control Register ((0D)00H: Read/Write Except Where Noted)	66
Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write) ...	67
Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted) .	69
Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted) .....	70
Figure 43. Voltage Detection Register .....	71
Figure 44. Port Configuration Register (PCON)(0F)00H: Write Only) .....	72
Figure 45. Stop Mode Recovery Register ((0F)0BH: D6–D0=Write Only, D7=Read Only) .....	73
Figure 46. Stop Mode Recovery Register 2 ((0F)0DH:D2–D4, D6 Write Only)	74
Figure 47. Watch-Dog Timer Register ((0F) 0FH: Write Only) .....	75
Figure 48. Port 2 Mode Register (F6H: Write Only) .....	75
Figure 49. Port 3 Mode Register (F7H: Write Only) .....	76
Figure 50. Port 0 and 1 Mode Register (F8H: Write Only) .....	77
Figure 51. Interrupt Priority Register (F9H: Write Only) .....	78
Figure 52. Interrupt Request Register (FAH: Read/Write) .....	79
Figure 53. Interrupt Mask Register (FBH: Read/Write) .....	79
Figure 54. Flag Register (FCH: Read/Write) .....	80
Figure 55. Register Pointer (FDH: Read/Write) .....	80
Figure 56. Stack Pointer High (FEH: Read/Write) .....	81
Figure 57. Stack Pointer Low (FFH: Read/Write) .....	81
Figure 58. 20-Pin CDIP Package .....	82
Figure 59. 20-Pin PDIP Package Diagram .....	82
Figure 60. 20-Pin SOIC Package Diagram .....	83
Figure 61. 20-Pin SSOP Package Diagram .....	84
Figure 62. 28-Pin SOIC Package Diagram .....	85
Figure 63. 28-Pin CDIP Package Diagram .....	86
Figure 64. 28-Pin PDIP Package Diagram .....	86
Figure 65. 28-Pin SSOP Package Diagram .....	87
Figure 66. 40-Pin PDIP Package Diagram .....	87
Figure 67. 40-Pin CDIP Package Diagram .....	88



# ***List of Tables***

Table 1.	Revision History of this Document . . . . .	iii
Table 2.	Features . . . . .	1
Table 3.	Power Connections . . . . .	3
Table 4.	20-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification . . . . .	5
Table 5.	28-Pin PDIP/SOIC/SSOP/CDIP* Pin Identification . . . . .	6
Table 6.	40- and 48-Pin Configuration . . . . .	8
Table 7.	Absolute Maximum Ratings . . . . .	10
Table 8.	Capacitance . . . . .	11
Table 9.	GP323HS DC Characteristics . . . . .	11
Table 10.	GP323HE DC Characteristics . . . . .	12
Table 11.	GP323HA DC Characteristics . . . . .	14
Table 12.	EPROM/OTP Characteristics . . . . .	15
Table 13.	AC Characteristics . . . . .	17
Table 14.	Port 3 Pin Function Summary. . . . .	23
Table 15.	CTR1(0D)01H T8 and T16 Common Functions . . . . .	35
Table 16.	Interrupt Types, Sources, and Vectors . . . . .	52
Table 17.	IRQ Register. . . . .	52
Table 18.	SMR2(F)0DH:Stop Mode Recovery Register 2* . . . . .	58
Table 19.	Stop Mode Recovery Source . . . . .	60
Table 20.	Watch-Dog Timer Time Select . . . . .	63
Table 21.	EPROM Selectable Options . . . . .	64



- Port 1: 0–3 pull-up transistors
- Port 1: 4–7 pull-up transistors
- Port 2: 0–7 pull-up transistors
- EPROM Protection
- WDT enabled at POR

## General Description

The ZGP323H is an OTP-based member of the MCU family of infrared microcontrollers. With 237B of general-purpose RAM and up to 32KB of OTP, ZiLOG®'s CMOS microcontrollers offer fast-executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The ZGP323H architecture (Figure 1) is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File allowing access to register-mapped peripherals, input/output (I/O) circuits, and powerful counter/timer circuitry. The Z8® offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: Program Memory, Register File and Expanded Register File. The register file is composed of 256 Bytes (B) of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z8 GP OTP offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (see Figure 2). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages.

► **Note:** All signals with an overline, " $\overline{\phantom{x}}$ ", are active Low. For example,  $\overline{B/W}$ , in which WORD is active Low, and  $\overline{B/W}$ , in which BYTE is active Low.

Power connections use the conventional descriptions listed in Table 3.

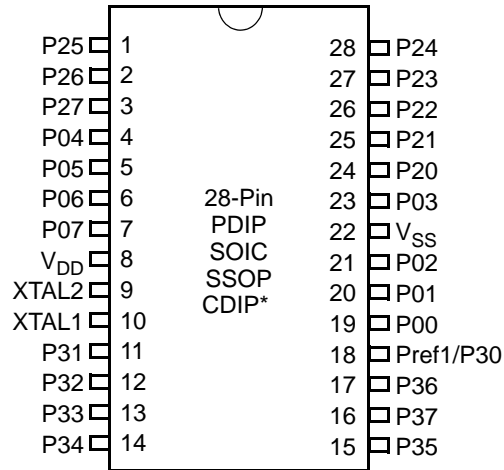


Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

Table 5. 28-Pin PDIP/SOIC/SSOP/CDIP\* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V <sub>DD</sub>		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V <sub>CC</sub> if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V <sub>SS</sub>		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

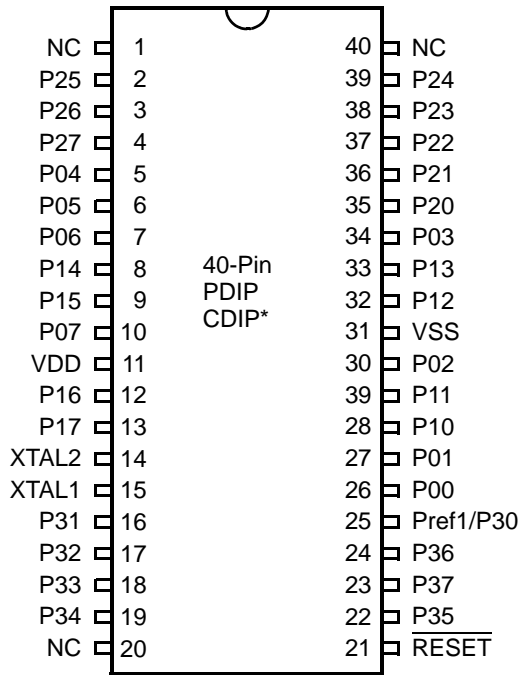


Figure 5. 40-Pin PDIP/CDIP\* Pin Configuration

► **Note:** \*Windowed Cerdip. These units are intended to be used for engineering code development only. ZiLOG does not recommend/guarantee this package for production use.



CTR1(0D)01H" on page 35). Other edge detect and IRQ modes are described in Table 14.

- **Note:** Comparators are powered down by entering Stop Mode. For P31–P33 to be used in a Stop Mode Recovery (SMR) source, these inputs must be placed into digital mode.

**Table 14. Port 3 Pin Function Summary**

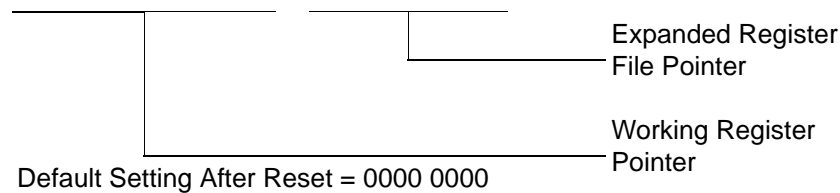
Pin	I/O	Counter/Timers	Comparator	Interrupt
Pref1/P30	IN		RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for each of the counter/timers and the AND/OR Logic (see Figure 13). Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



**Figure 16. Register Pointer**

**Example: Z8 GP: (See Figure 15 on page 28)**

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTR0

R1 = CTR1

R2 = CTR2

R3 = Reserved

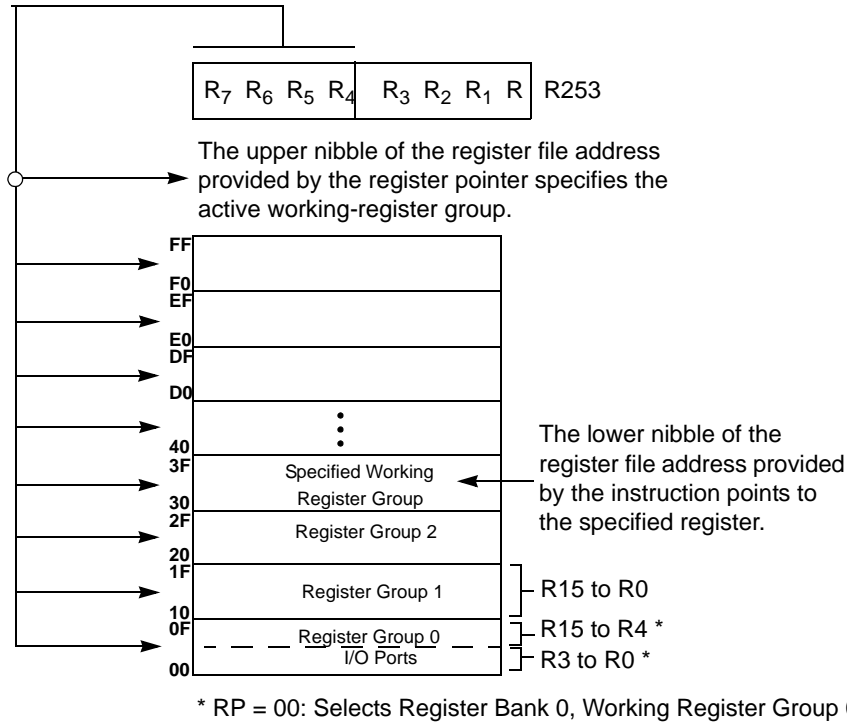


Figure 17. Register Pointer—Detail

### Stack

The internal register file is used for the stack. An 8-bit Stack Pointer SPL (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH (R254) can be used as a general-purpose register.



### Capture\_INT\_Mask

Set this bit to allow an interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

### Counter\_INT\_Mask

Set this bit to allow an interrupt when T8 has a timeout.

### P34\_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

### T8 and T16 Common Functions—CTR1(0D)01H

This register controls the functions in common with the T8 and T16.

Table 16 lists and briefly describes the fields for this register.

**Table 16. CTR1(0D)01H T8 and T16 Common Functions**

Field	Bit Position		Value	Description
Mode	7-----	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/ Demodulator_Input	-6-----	R/W	0*	Transmit Mode
			1	Port Output
				T8/T16 Output
			0*	Demodulation Mode
			1	P31
				P20
T8/T16_Logic/ Edge_Detect	--54----	R/W		Transmit Mode
			00**	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00**	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved

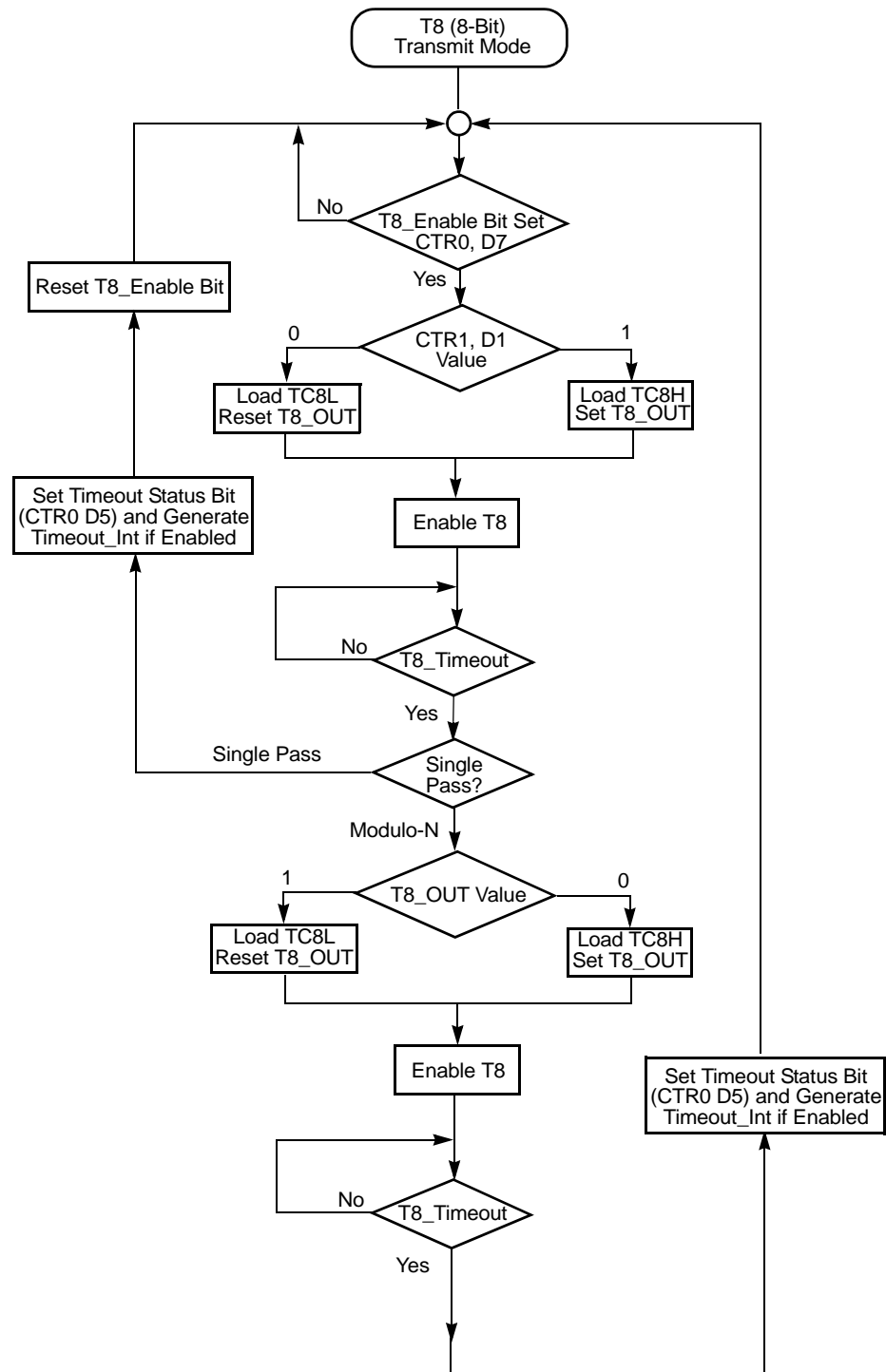
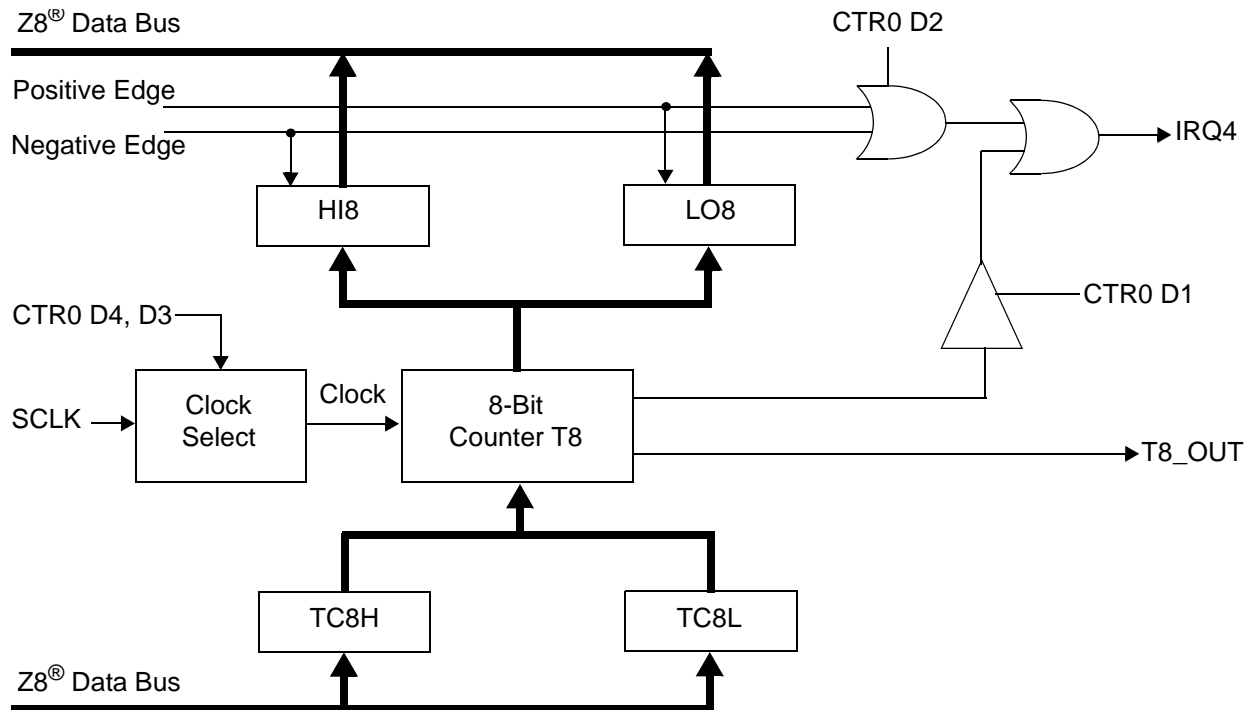


Figure 19. Transmit Mode Flowchart

When T8 is enabled, the output T8\_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8\_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8\_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8\_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8\_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8\_OUT level and repeats the cycle. See Figure 20.



**Figure 20. 8-Bit Counter/Timer Circuits**

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



**Caution:** To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



### Power-On Reset

A timer circuit clocked by a dedicated on-board RC-oscillator is used for the Power-On Reset (POR) timer function. The POR time allows  $V_{DD}$  and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status, including Waking up from  $V_{BO}$  Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Timeout

The POR timer is 2.5 ms minimum. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock).

### HALT Mode

This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after HALT Mode.

### STOP Mode

This instruction turns off the internal clock and external crystal oscillation, reducing the standby current to 10  $\mu$ A or less. STOP Mode is terminated only by a reset, such as WDT timeout, POR, SMR or external reset. This condition causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP (Opcode = FFH) immediately before the appropriate sleep instruction, as follows:

```
FF      NOP      ; clear the pipeline
6F      Stop     ; enter Stop Mode
```

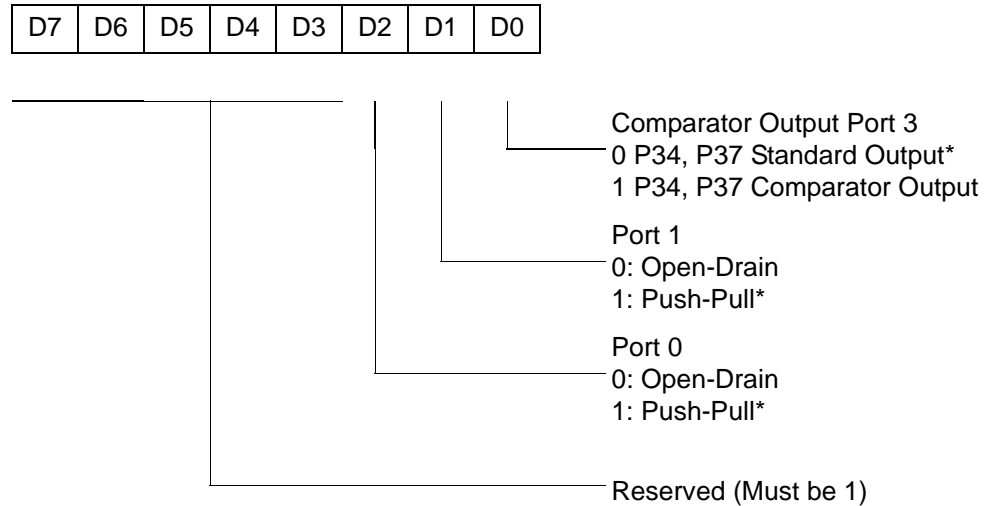
or

```
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

### Port Configuration Register

The Port Configuration (PCON) register (Figure 32) configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00.

PCON(FH)00H



\* Default setting after reset

**Figure 32. Port Configuration Register (PCON) (Write Only)**

#### Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

#### Port 1 Output Mode (D1)

Bit 1 controls the output mode of port 1. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.



### **Port 0 Output Mode (D2)**

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

### **Stop-Mode Recovery Register (SMR)**

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

Table 22. Stop Mode Recovery Source

SMR:432			Operation
D4	D3	D2	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

- **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state. This condition allows the remaining inputs to control the AND/OR function. Refer to SMR2 register on page 61 for other recover sources.

#### Stop Mode Recovery Delay Select (D5)

This bit, if Low, disables the  $T_{POR}$  delay after Stop Mode Recovery. The default configuration of this bit is 1. If the “fast” wake up is selected, the Stop Mode Recovery source must be kept active for at least 5  $T_{pC}$ .

- **Note:** This bit must be set to 1 if using a crystal or resonator clock source. The  $T_{POR}$  delay allows the clock source to stabilize before executing instructions.

#### Stop Mode Recovery Edge Select (D6)

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the device from Stop Mode. A 0 indicates Low level recovery. The default is 0 on POR.

#### Cold or Warm Start (D7)

This bit is read only. It is set to 1 when the device is recovered from Stop Mode. The bit is set to 0 when the device reset is other than Stop Mode Recovery (SMR).

**Low-Voltage Detection Register—LVD(D)0Ch**

- **Note:** Voltage detection does not work at Stop mode. It must be disabled during Stop mode in order to reduce current.

Field	Bit Position	Description		
LVD	76543---	Reserved No Effect		
	----2--	R	1 0*	HVD flag set HVD flag reset
	-----1-	R	1 0*	LVD flag set LVD flag reset
	-----0	R/W	1 0*	Enable VD Disable VD

\*Default after POR

- **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

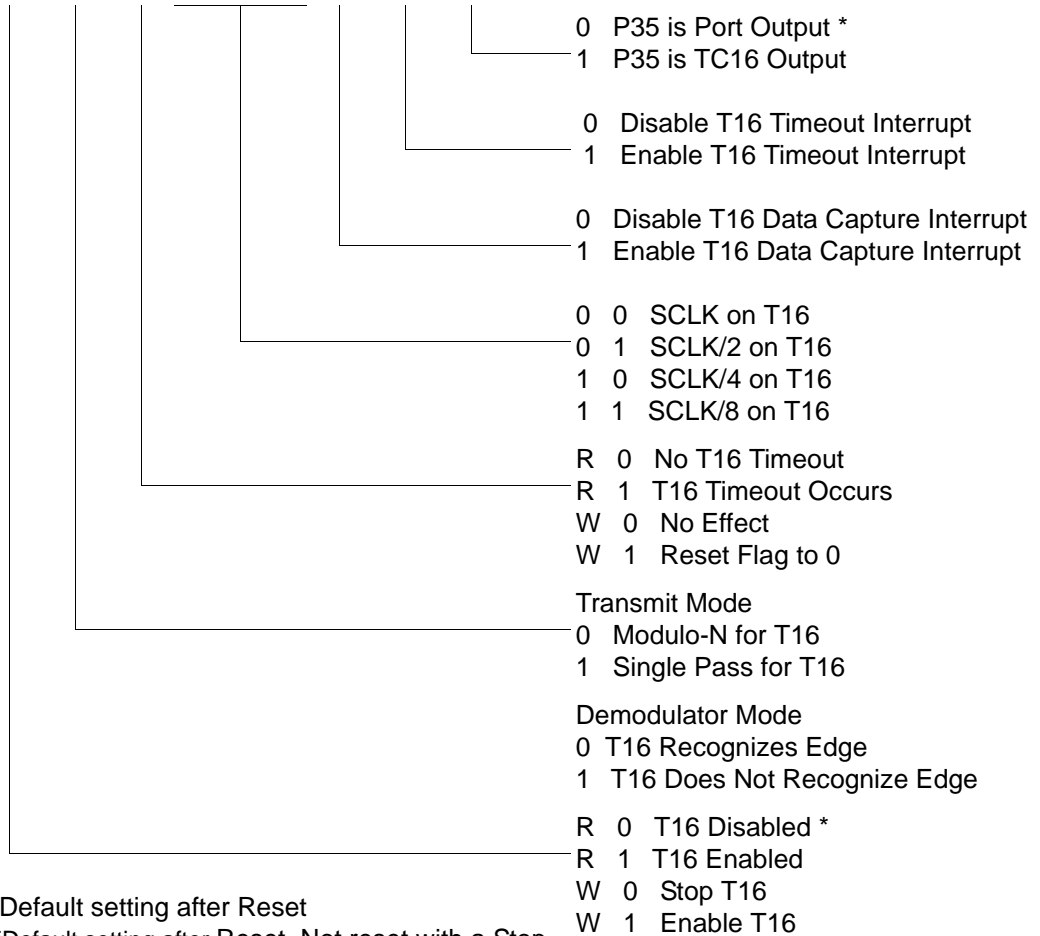
**Voltage Detection and Flags**

The Voltage Detection register (LVD, register 0CH at the expanded register bank 0Dh) offers an option of monitoring the  $V_{CC}$  voltage. The Voltage Detection is enabled when bit 0 of LVD register is set. Once Voltage Detection is enabled, the  $V_{CC}$  level is monitored in real time. The flags in the LVD register valid 20uS after Voltage Detection is enabled. The HVD flag (bit 2 of the LVD register) is set only if  $V_{CC}$  is higher than  $V_{HVD}$ . The LVD flag (bit 1 of the LVD register) is set only if  $V_{CC}$  is lower than the  $V_{LVD}$ . When Voltage Detection is enabled, the LVD flag also triggers IRQ5. The IRQ bit 5 latches the low voltage condition until it is cleared by instructions or reset. The IRQ5 interrupt is served if it is enabled in the IMR register. Otherwise, bit 5 of IRQ register is latched as a flag only.

- **Notes:** If it is necessary to receive an LVD interrupt upon power-up at an operating voltage lower than the low battery detect threshold, enable interrupts using the Enable Interrupt instruction (EI) prior to enabling the voltage detection.

CTR2(0D)02H

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

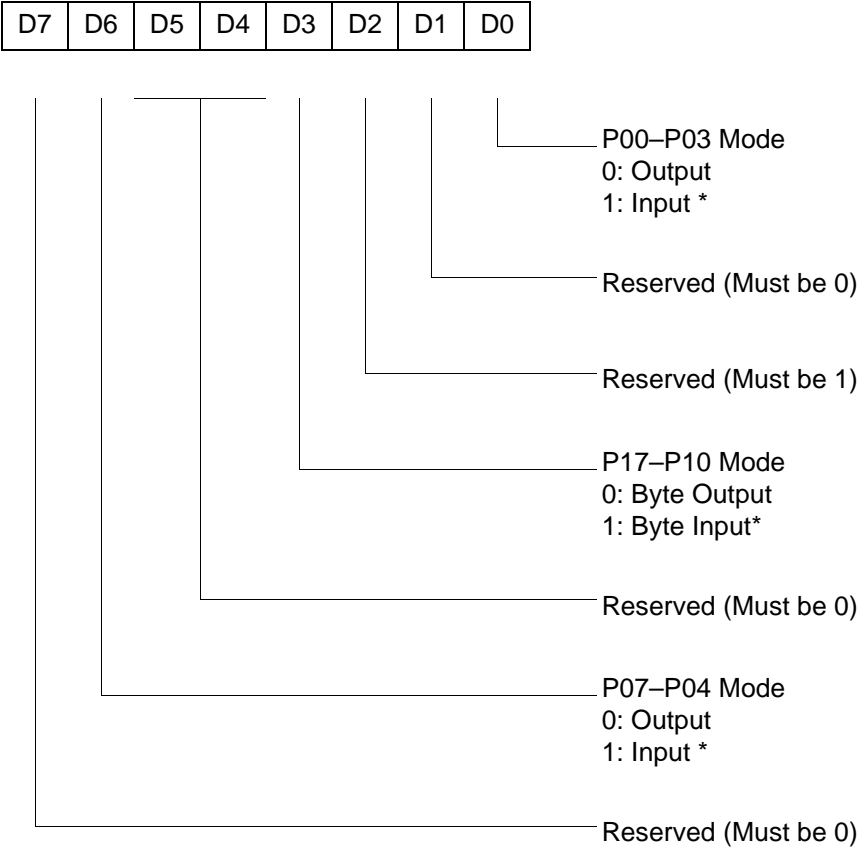


\* Default setting after Reset

\*\*Default setting after Reset. Not reset with a Stop-Mode recovery.

**Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)**

R248 P01M(F8H)



\* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)



## Ordering Information

### 32KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4832C	48-pin SSOP 32K OTP	ZGP323HSS2832C	28-pin SOIC 32K OTP
ZGP323HSP4032C	40-pin PDIP 32K OTP	ZGP323HSH2032C	20-pin SSOP 32K OTP
ZGP323HSK2832E	28-pin CDIP 32K OTP	ZGP323HSK2032E	20-pin CDIP 32K OTP
ZGP323HSK4032E	40-pin CDIP 32K OTP	ZGP323HSP2032C	20-pin PDIP 32K OTP
ZGP323HSH2832C	28-pin SSOP 32K OTP	ZGP323HSS2032C	20-pin SOIC 32K OTP
ZGP323HSP2832C	28-pin PDIP 32K OTP		

### 32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4832C	48-pin SSOP 32K OTP	ZGP323HES2832C	28-pin SOIC 32K OTP
ZGP323HEP4032C	40-pin PDIP 32K OTP	ZGP323HEH2032C	20-pin SSOP 32K OTP
ZGP323HEH2832C	28-pin SSOP 32K OTP	ZGP323HEP2032C	20-pin PDIP 32K OTP
ZGP323HEP2832C	28-pin PDIP 32K OTP	ZGP323HES2032C	20-pin SOIC 32K OTP

### 32KB Automotive Temperature: -40° to +125°C

Part Number	Description	Part Number	Description
ZGP323HAH4832C	48-pin SSOP 32K OTP	ZGP323HAS2832C	28-pin SOIC 32K OTP
ZGP323HAP4032C	40-pin PDIP 32K OTP	ZGP323HAH2032C	20-pin SSOP 32K OTP
ZGP323HAH2832C	28-pin SSOP 32K OTP	ZGP323HAP2032C	20-pin PDIP 32K OTP
ZGP323HAP2832C	28-pin PDIP 32K OTP	ZGP323HAS2032C	20-pin SOIC 32K OTP

Replace C with G for Lead-Free Packaging



**Example**

