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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/zgp323hss2008g">https://www.e-xfl.com/product-detail/zilog/zgp323hss2008g</a>



Figure 68. 48-Pin SSOP Package Design ..... 89



## Development Features

Table 2 lists the features of ZiLOG<sup>®</sup>'s ZGP323H members.

**Table 2. Features**

Device	OTP (KB)	RAM (Bytes)	I/O Lines	Voltage Range
ZGP323H OTP MCU Family	4, 8, 16, 32	237	32, 24 or 16	2.0V–5.5V

- Low power consumption—18mW (typical)
- T = Temperature  
S = Standard 0° to +70°C  
E = Extended -40° to +105°C  
A = Automotive -40° to +125°C
- Three standby modes:
  - STOP— (typical 1.8μA)
  - HALT— (typical 0.8mA)
  - Low voltage reset
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
- Six priority interrupts
  - Three external
  - Two assigned to counter/timers
  - One low-voltage detection interrupt
- Low voltage detection and high voltage detection flags
- Programmable Watch-Dog Timer/Power-On Reset (WDT/POR) circuits
- Two independent comparators with programmable interrupt polarity
- Programmable EPROM options
  - Port 0: 0–3 pull-up transistors
  - Port 0: 4–7 pull-up transistors

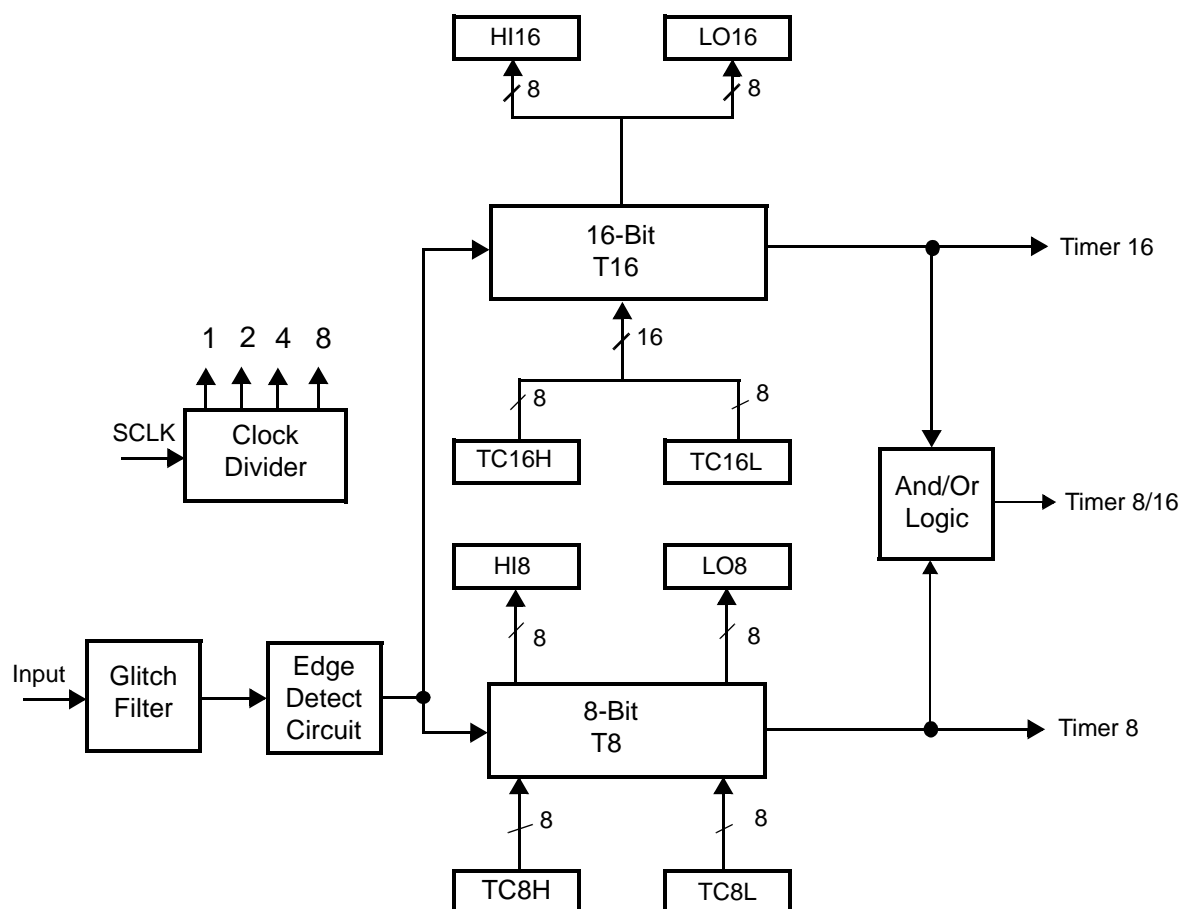


Figure 2. Counter/Timers Diagram

## Pin Description

The pin configuration for the 20-pin PDIP/SOIC/SSOP is illustrated in Figure 3 and described in Table 4. The pin configuration for the 28-pin PDIP/SOIC/SSOP are depicted in Figure 4 and described in Table 5. The pin configurations for the 40-pin PDIP and 48-pin SSOP versions are illustrated in Figure 5, Figure 6, and described in Table 6.

For customer engineering code development, a UV eraseable windowed cerdip packaging is offered in 20-pin, 28-pin, and 40-pin configurations. ZiLOG does not recommend nor guarantee these packages for use in production.

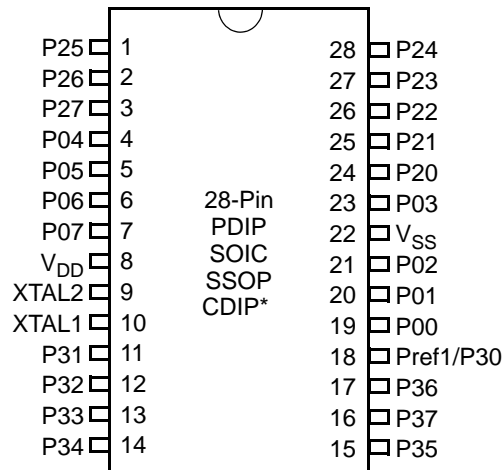


Figure 4. 28-Pin PDIP/SOIC/SSOP/CDIP\* Pin Configuration

Table 5. 28-Pin PDIP/SOIC/SSOP/CDIP\* Pin Identification

Pin	Symbol	Direction	Description
1-3	P25-P27	Input/Output	Port 2, Bits 5,6,7
4-7	P04-P07	Input/Output	Port 0, Bits 4,5,6,7
8	V <sub>DD</sub>		Power supply
9	XTAL2	Output	Crystal, oscillator clock
10	XTAL1	Input	Crystal, oscillator clock
11-13	P31-P33	Input	Port 3, Bits 1,2,3
14	P34	Output	Port 3, Bit 4
15	P35	Output	Port 3, Bit 5
16	P37	Output	Port 3, Bit 7
17	P36	Output	Port 3, Bit 6
18	Pref1/P30 Port 3 Bit 0	Input	Analog ref input; connect to V <sub>CC</sub> if not used Input for Pref1/P30
19-21	P00-P02	Input/Output	Port 0, Bits 0,1,2
22	V <sub>SS</sub>		Ground
23	P03	Input/Output	Port 0, Bit 3
24-28	P20-P24	Input/Output	Port 2, Bits 0-4

## Capacitance

Table 8 lists the capacitances.

**Table 8. Capacitance**

Parameter	Maximum
Input capacitance	12pF
Output capacitance	12pF
I/O capacitance	12pF
Note: $T_A = 25^\circ\text{C}$ , $V_{CC} = \text{GND} = 0\text{V}$ , $f = 1.0\text{MHz}$ , unmeasured pins returned to GND	

## DC Characteristics

**Table 9. GP323HS DC Characteristics**

Symbol	Parameter	$V_{CC}$	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$			Units	Conditions	Notes
			Min	Typ(7)	Max			
$V_{CC}$	Supply Voltage		2.0		5.5	V	See Note 5	5
$V_{CH}$	Clock Input High Voltage	2.0-5.5	$0.8 V_{CC}$		$V_{CC}+0.3$	V	Driven by External Clock Generator	
$V_{CL}$	Clock Input Low Voltage	2.0-5.5	$V_{SS}-0.3$		0.4	V	Driven by External Clock Generator	
$V_{IH}$	Input High Voltage	2.0-5.5	$0.7 V_{CC}$		$V_{CC}+0.3$	V		
$V_{IL}$	Input Low Voltage	2.0-5.5	$V_{SS}-0.3$		$0.2 V_{CC}$	V		
$V_{OH1}$	Output High Voltage	2.0-5.5	$V_{CC}-0.4$			V	$I_{OH} = -0.5\text{mA}$	
$V_{OH2}$	Output High Voltage (P36, P37, P00, P01)	2.0-5.5	$V_{CC}-0.8$			V	$I_{OH} = -7\text{mA}$	
$V_{OL1}$	Output Low Voltage	2.0-5.5			0.4	V	$I_{OL} = 4.0\text{mA}$	
$V_{OL2}$	Output Low Voltage (P00, P01, P36, P37)	2.0-5.5			0.8	V	$I_{OL} = 10\text{mA}$	
$V_{OFFSET}$	Comparator Input Offset Voltage	2.0-5.5			25	mV		
$V_{REF}$	Comparator Reference Voltage	2.0-5.5	0		$V_{CC}$ 1.75	V		
$I_{IL}$	Input Leakage	2.0-5.5	-1		1	$\mu\text{A}$	$V_{IN} = 0\text{V}$ , $V_{CC}$ Pull-ups disabled	
$R_{PU}$	Pull-up Resistance	2.0V	225		675	$\text{K}\Omega$	$V_{IN} = 0\text{V}$ ; Pullups selected by mask option	
		3.6V	75		275	$\text{K}\Omega$		
		5.0V	40		160	$\text{K}\Omega$		



AC Characteristics

Figure 8 and Table 13 describe the Alternating Current (AC) characteristics.

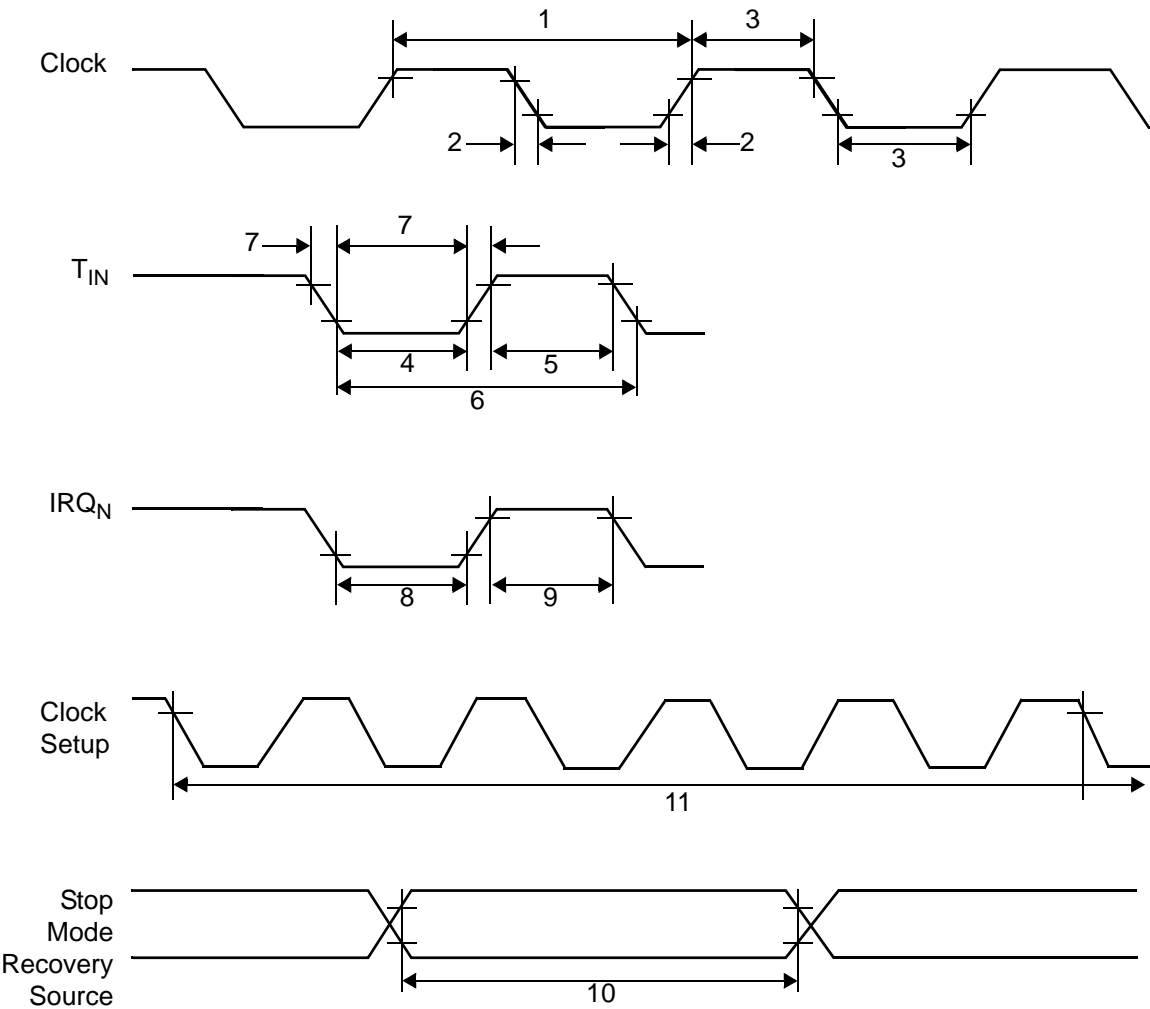


Figure 8. AC Timing Diagram



## Pin Functions

### XTAL1 Crystal 1 (Time-Based Input)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator input. Additionally, an optional external single-phase clock can be coded to the on-chip oscillator input.

### XTAL2 Crystal 2 (Time-Based Output)

This pin connects a parallel-resonant crystal or ceramic resonator to the on-chip oscillator output.

### Port 0 (P07–P00)

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port. The output drivers are push-pull or open-drain controlled by bit D2 in the PCON register.

If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

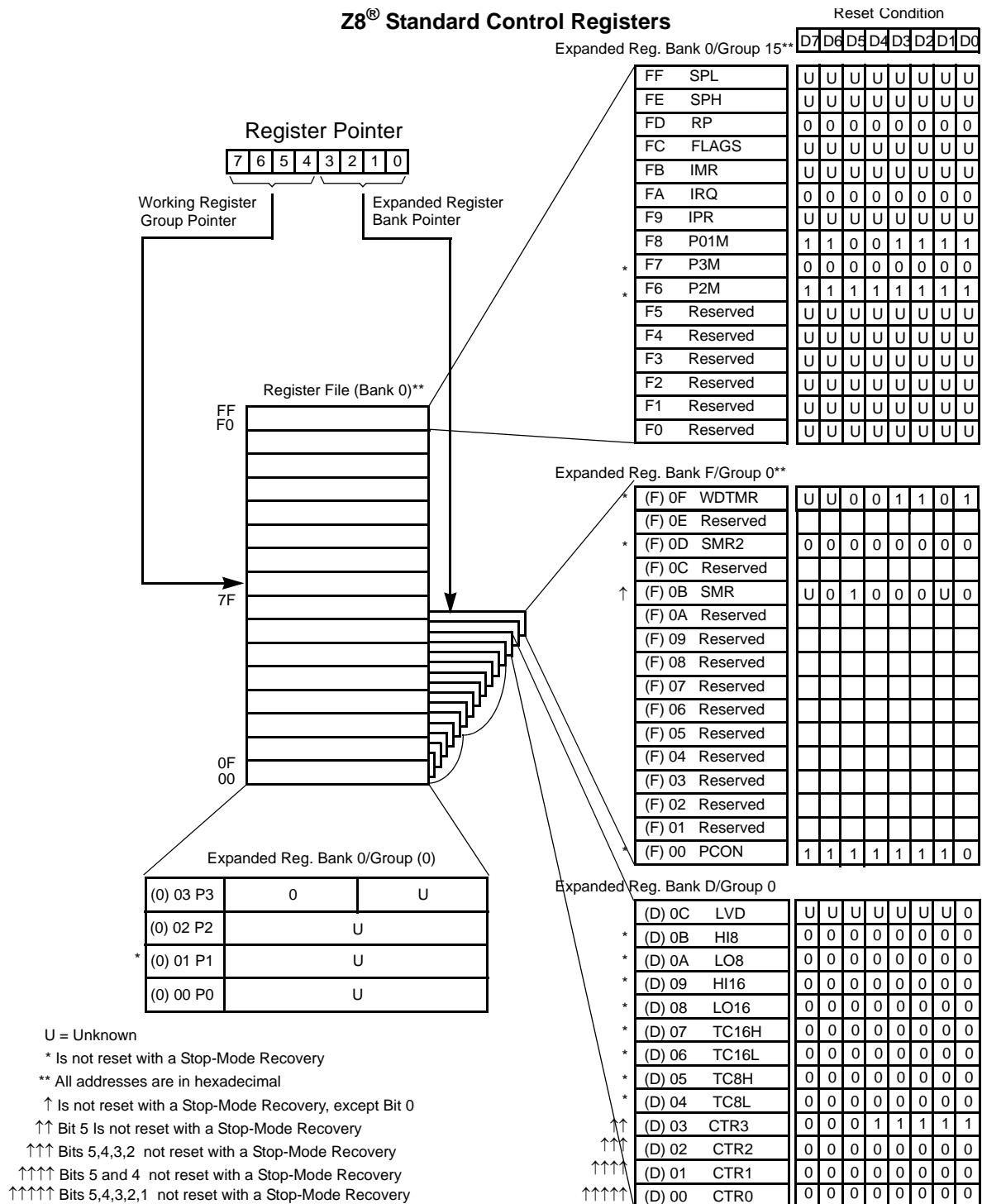
An optional pull-up transistor is available as a mask option on all Port 0 bits with nibble select.

- **Notes:** Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

The Port 0 direction is reset to its default state following an SMR.



## Z8<sup>®</sup> Standard Control Registers

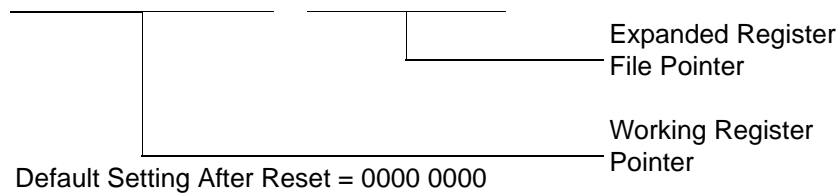


### Figure 15. Expanded Register File Architecture

The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A 0H in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.

R253 RP

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----



**Figure 16. Register Pointer**

**Example: Z8 GP: (See Figure 15 on page 28)**

R253 RP = 00h

R0 = Port 0

R1 = Port 1

R2 = Port 2

R3 = Port 3

But if:

R253 RP = 0Dh

R0 = CTR0

R1 = CTR1

R2 = CTR2

R3 = Reserved

## Timers

### T8\_Capture\_HI—HI8(D)0BH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 1.

Field	Bit Position	Description
T8_Capture_HI	[7:0]	R/W Captured Data - No Effect

### T8\_Capture\_LO—L08(D)0AH

This register holds the captured data from the output of the 8-bit Counter/Timer0. Typically, this register holds the number of counts when the input signal is 0.

Field	Bit Position	Description
T8_Capture_LO	[7:0]	R/W Captured Data - No Effect

### T16\_Capture\_HI—HI16(D)09H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position	Description
T16_Capture_HI	[7:0]	R/W Captured Data - No Effect

### T16\_Capture\_LO—L016(D)08H

This register holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position	Description
T16_Capture_LO	[7:0]	R/W Captured Data - No Effect

### Counter/Timer2 MS-Byte Hold Register—TC16H(D)07H

Field	Bit Position	Description
T16_Data_HI	[7:0]	R/W Data



### Counter/Timer2 LS-Byte Hold Register—TC16L(D)06H

Field	Bit Position	Description
T16_Data_LO	[7:0]	R/W Data

### Counter/Timer8 High Hold Register—TC8H(D)05H

Field	Bit Position	Description
T8_Level_HI	[7:0]	R/W Data

### Counter/Timer8 Low Hold Register—TC8L(D)04H

Field	Bit Position	Description
T8_Level_LO	[7:0]	R/W Data

### CTR0 Counter/Timer8 Control Register—CTR0(D)00H

Table 15 lists and briefly describes the fields for this register.

**Table 15. CTR0(D)00H Counter/Timer8 Control Register**

Field	Bit Position		Value	Description
T8_Enable	7-----	R/W	0*	Counter Disabled
			1	Counter Enabled
			0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-----	R/W	0*	Modulo-N
			1	Single Pass
Time_Out	--5-----	R/W	0**	No Counter Time-Out
			1	Counter Time-Out Occurred
			0	No Effect
			1	Reset Flag to 0
T8_Clock	---43---	R/W	0 0**	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_Mask	----2--	R/W	0**	Disable Data Capture Interrupt
			1	Enable Data Capture Interrupt

When T8 is enabled, the output T8\_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8\_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8\_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8\_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8\_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8\_OUT level and repeats the cycle. See Figure 20.

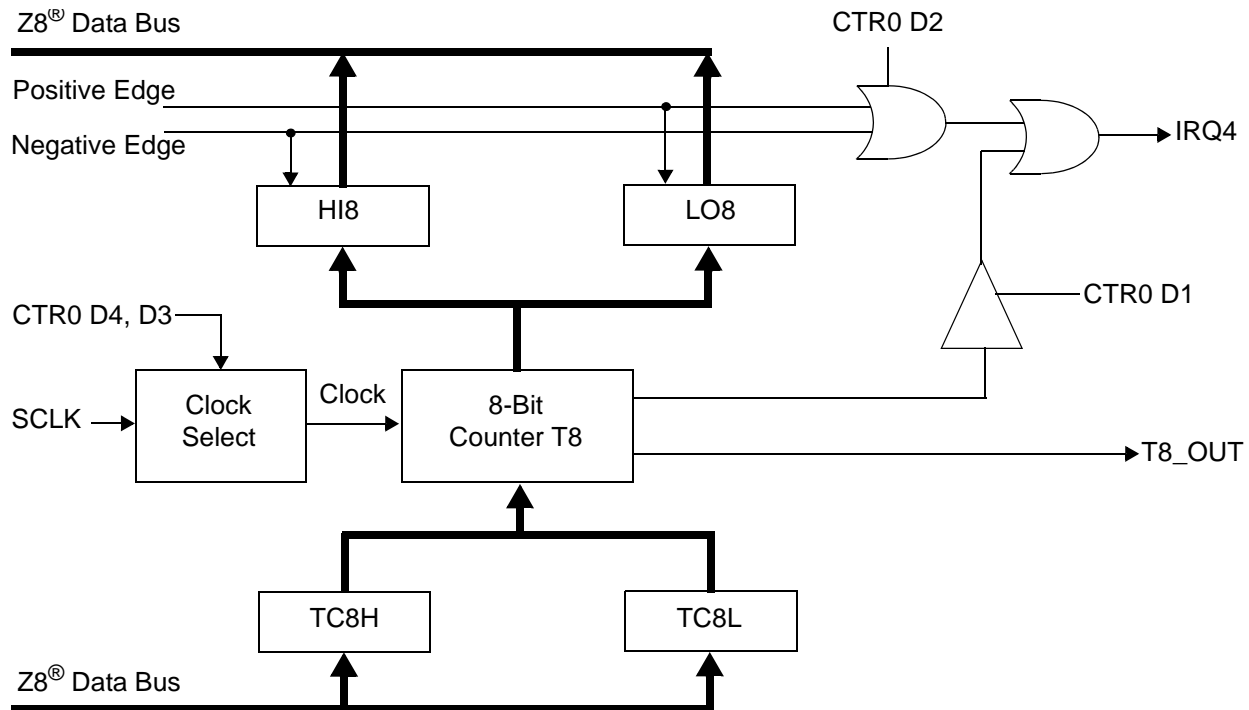
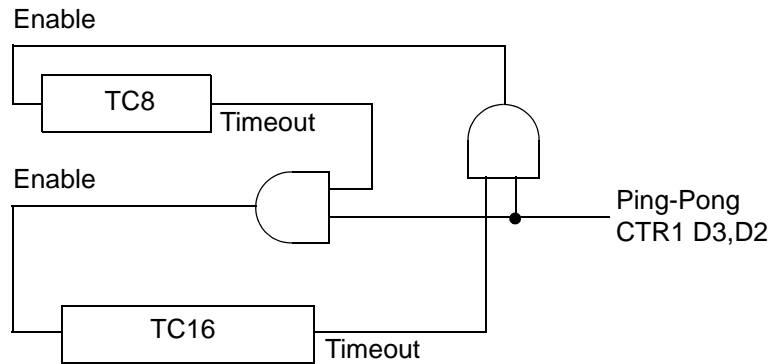


Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



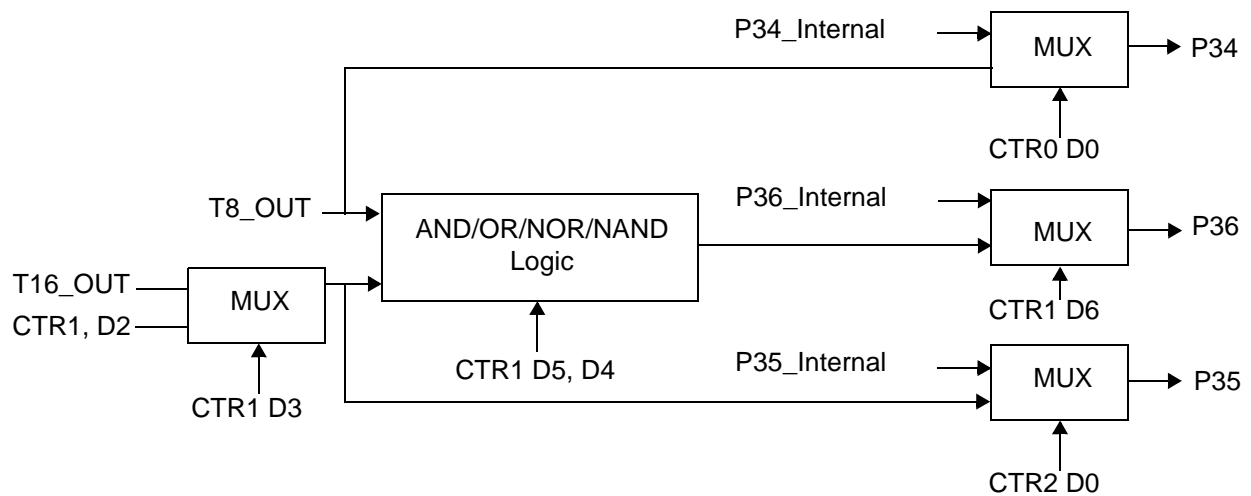
**Caution:** To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



**Figure 28. Ping-Pong Mode Diagram**

### Initiating PING-PONG Mode

First, make sure both counter/timers are not running. Set T8 into Single-Pass mode (CTR0, D6), set T16 into SINGLE-PASS mode (CTR2, D6), and set the Ping-Pong mode (CTR1, D2; D3). These instructions can be in random order. Finally, start PING-PONG mode by enabling either T8 (CTR0, D7) or T16 (CTR2, D7). See Figure 29.



**Figure 29. Output Circuit**

The initial value of T8 or T16 must not be 1. Stopping the timer and restarting the timer reloads the initial value to avoid an unknown previous value.

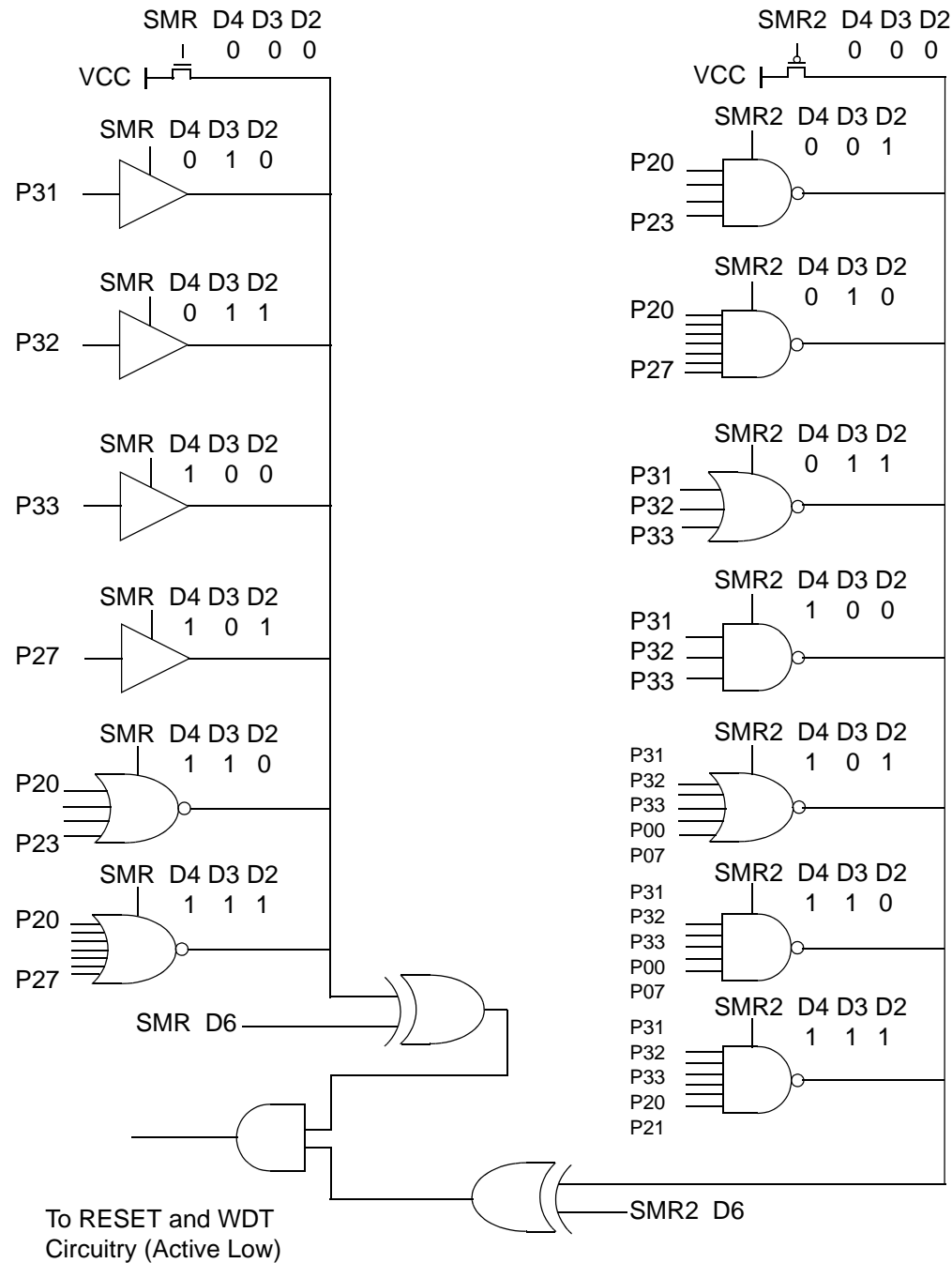


Figure 35. Stop Mode Recovery Source

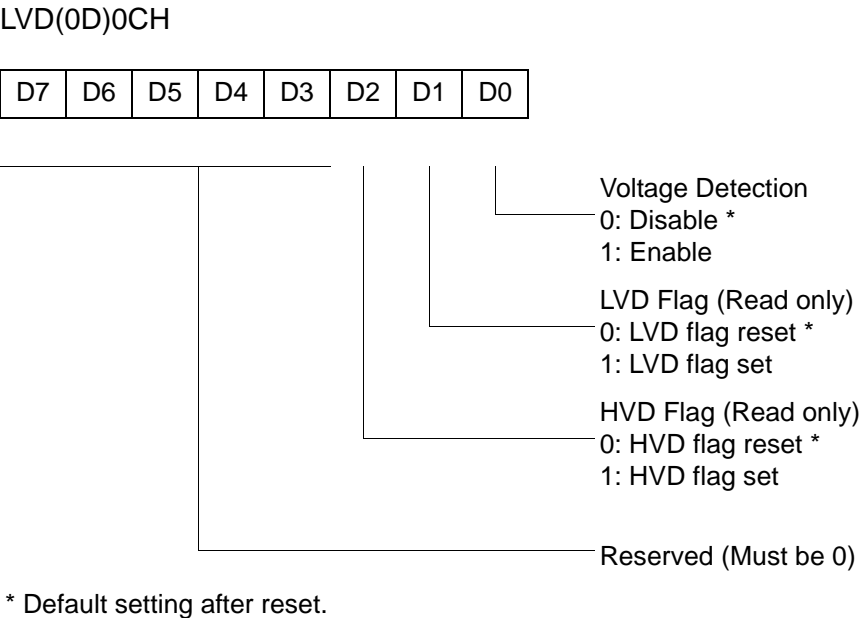


Figure 43. Voltage Detection Register

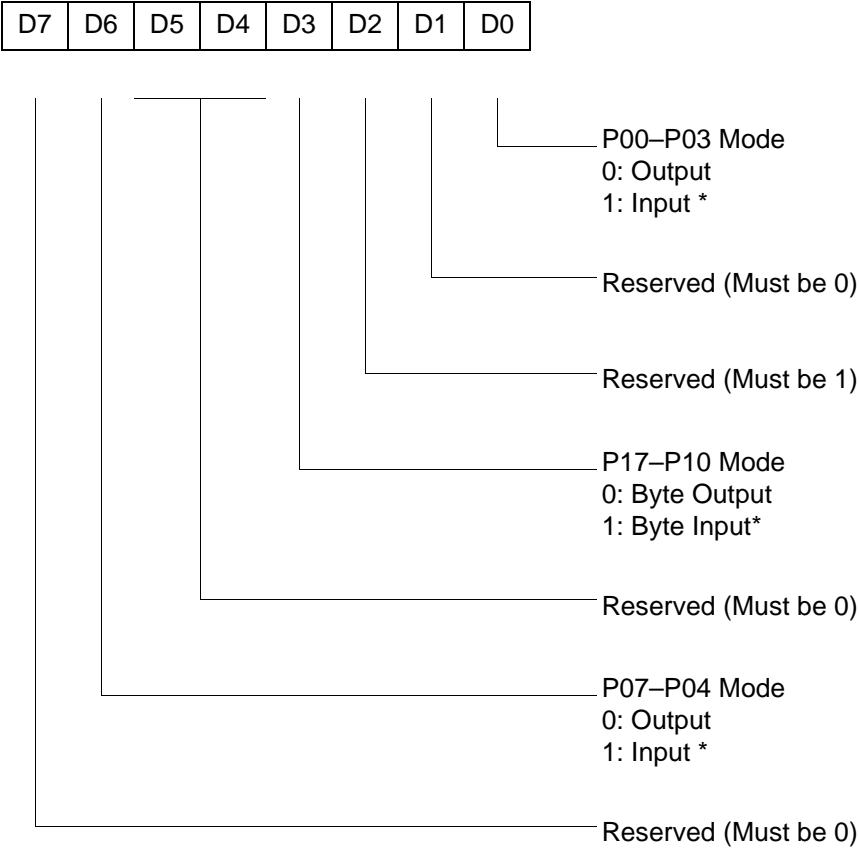
► **Note:** Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

## Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.



R248 P01M(F8H)



\* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

Figure 50. Port 0 and 1 Mode Register (F8H: Write Only)

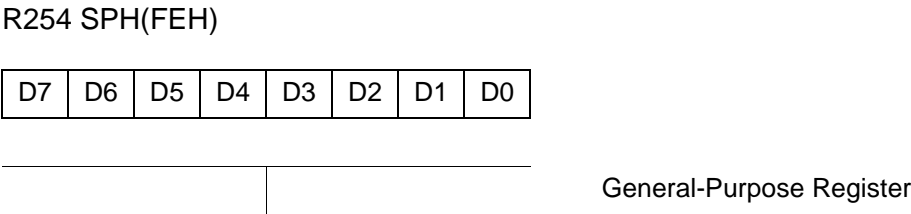


Figure 56. Stack Pointer High (FEH: Read/Write)

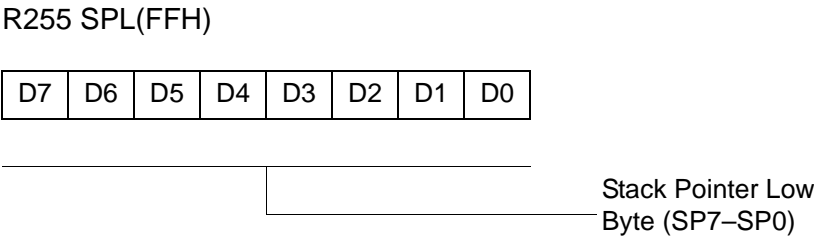


Figure 57. Stack Pointer Low (FFH: Read/Write)

Package Information

Package information for all versions of ZGP323H is depicted in Figures 59 through Figure 68.



**4KB Standard Temperature: 0° to +70°C**

Part Number	Description	Part Number	Description
ZGP323HSH4804C	48-pin SSOP 4K OTP	ZGP323HSS2804C	28-pin SOIC 4K OTP
ZGP323HSP4004C	40-pin PDIP 4K OTP	ZGP323HSH2004C	20-pin SSOP 4K OTP
ZGP323HSH2804C	28-pin SSOP 4K OTP	ZGP323HSP2004C	20-pin PDIP 4K OTP
ZGP323HSP2804C	28-pin PDIP 4K OTP	ZGP323HSS2004C	20-pin SOIC 4K OTP

**4KB Extended Temperature: -40° to +105°C**

Part Number	Description	Part Number	Description
ZGP323HEH4804C	48-pin SSOP 4K OTP	ZGP323HES2804C	28-pin SOIC 4K OTP
ZGP323HEP4004C	40-pin PDIP 4K OTP	ZGP323HEH2004C	20-pin SSOP 4K OTP
ZGP323HEH2804C	28-pin SSOP 4K OTP	ZGP323HEP2004C	20-pin PDIP 4K OTP
ZGP323HEP2804C	28-pin PDIP 4K OTP	ZGP323HES2004C	20-pin SOIC 4K OTP

**4KB Automotive Temperature: -40° to +125°C**

Part Number	Description	Part Number	Description
ZGP323HAH4804C	48-pin SSOP 4K OTP	ZGP323HAS2804C	28-pin SOIC 4K OTP
ZGP323HAP4004C	40-pin PDIP 4K OTP	ZGP323HAH2004C	20-pin SSOP 4K OTP
ZGP323HAH2804C	28-pin SSOP 4K OTP	ZGP323HAP2004C	20-pin PDIP 4K OTP
ZGP323HAP2804C	28-pin PDIP 4K OTP	ZGP323HAS2004C	20-pin SOIC 4K OTP

Replace C with G for Lead-Free Packaging

**Additional Components**

Part Number	Description	Part Number	Description
ZGP323ICE01ZEM (For 3.6V Emulation only)	Emulator/programmer	ZGP32300100ZPR (Ethernet)	Programming system
		ZGP32300200ZPR (USB)	Programming system



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

**Codes**

ZG = ZiLOG General Purpose Family

P = OTP

323 = Family Designation

H = High Voltage

T = Temperature

S = Standard 0° to +70°C

E = Extended -40° to +105°C

A = Automotive -40° to +125°C

P = Package Type:

K = CDIP

P = PDIP

H = SSOP

S = SOIC

## = Number of Pins

CC = Memory Size

M = Molding Compound

C = Standard Plastic Packaging Molding Compound

G = Green Plastic Molding Compound

E = Standard Cer Dip flow



**Example**

