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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Obsolete
Z8
8-Bit
8MHz
-
HLVD, POR, WDT
16
16KB (16K x 8)
ОТР
-
237 x 8
2V ~ 5.5V
-
Internal
0°C ~ 70°C (TA)
Surface Mount
20-SOIC (0.295", 7.50mm Width)
-
https://www.e-xfl.com/product-detail/zilog/zgp323hss2016c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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# Table 3. Power Connections

Connection	Circuit	Device	
Power	V <sub>CC</sub>	V <sub>DD</sub>	
Ground	GND	V <sub>SS</sub>	



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram







### Figure 12. Port 3 Configuration

Two on-board comparators process analog signals on P31 and P32, with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edgedetection circuit is through P31 or P20 (see "T8 and T16 Common Functions—



Location of 3	2768	Not Accessible
first Byte of	_100	On-Chip
executed		KOM
after RESET	12	Reset Start Address
	11	IRQ5
	10	IRQ5
	9	IRQ4
	8	IRQ4
	7	IRQ3
(Lower Byte)	6	IRQ3
	5	IRQ2
Interrupt Vector	4	→ IRQ2
(Upper Byte)	3	IRQ1
	2	IRQ1
	1	IRQ0
	0	IRQ0



# **Expanded Register File**

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8<sup>®</sup> register address space (R0 through R15) has been implemented as 16 banks, with 16 registers per bank. These register groups are known as the



ERF (Expanded Register File). Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

**Note:** An expanded register bank is also referred to as an expanded register group (see Figure 15).



Field	Bit Position		Value	Description
Transmit_Submode/	32	R/W		Transmit Mode
Glitch_Filter			00*	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00*	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/	1-			Transmit Mode
Rising Edge		R/W	0*	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/	0			Transmit Mode
Falling_Edge		R/W	0*	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0*	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

#### Table 16.CTR1(0D)01H T8 and T16 Common Functions (Continued)

#### Note:

\*Default at Power-On Reset

\*Default at Power-On Reset. Not reset with Stop Mode recovery.

### Mode

If the result is 0, the counter/timers are in TRANSMIT mode; otherwise, they are in DEMODULATION mode.

### P36\_Out/Demodulator\_Input

In TRANSMIT Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In DEMODULATION Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

If the input signal is from Port 31, a capture event may also generate an IRQ2 interrupt. To prevent generating an IRQ2, either disable the IRQ2 interrupt by clearing its IMR bit D2 or use P20 as the input.



When T8 is enabled, the output T8\_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8\_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8\_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8\_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8\_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8\_OUT level and repeats the cycle. See Figure 20.



Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



**Caution:** To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



into LO8; if it is a negative edge, data is put into HI8. From that point, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt can be generated if enabled (CTR0, D2). Meanwhile, T8 is loaded with FFh and starts counting again. If T8 reaches 0, the timeout status bit (CTR0, D5) is set, and an interrupt can be generated if enabled (CTR0, D1). T8 then continues counting from FFH (see Figure 23 and Figure 24).



Figure 23. Demodulation Mode Count Capture Flowchart



# **T16 Transmit Mode**

In NORMAL or PING-PONG mode, the output of T16 when not enabled, is dependent on CTR1, D0. If it is a 0, T16\_OUT is a 1; if it is a 1, T16\_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3; D2 to a 10 or 11.

When T16 is enabled, TC16H \* 256 + TC16L is loaded, and T16\_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16\_OUT is toggled (in NORMAL or PING-PONG mode), an interrupt (CTR2, D1) is generated (if enabled), and a status bit (CTR2, D5) is set. See Figure 25.



Figure 25. 16-Bit Counter/Timer Circuits

**Note:** Global interrupts override this function as described in "Interrupts" on page 50.

If T16 is in SINGLE-PASS mode, it is stopped at this point (see Figure 26). If it is in Modulo-N Mode, it is loaded with TC16H \* 256 + TC16L, and the counting continues (see Figure 27).

You can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded.



**Caution:** Do not load these registers at the time the values are to be loaded into the counter/timer to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 causes T16 to count from 0 to FFFFH to FFFFH. Transition from 0 to FFFFH is not a timeout condition.







Figure 27. T16\_OUT in Modulo-N Mode

# **T16 DEMODULATION Mode**

The user must program TC16L and TC16H to FFH. After T16 is enabled, and the first edge (rising, falling, or both depending on CTR1 D5; D4) is detected, T16 captures HI16 and LO16, reloads, and begins counting.

# If D6 of CTR2 Is 0

When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current count in T16 is complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1, D1; D0) is set, and an interrupt is generated if enabled (CTR2, D2). T16 is loaded with FFFFH and starts again.

This T16 mode is generally used to measure space time, the length of time between bursts of carrier signal (marks).



# Clock

The device's on-chip oscillator has a high-gain, parallel-resonant amplifier, for connection to a crystal or ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100  $\Omega$ . The on-chip oscillator can be driven with a suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground.



f = 8mHz

Figure 31. Oscillator Configuration



# WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Because the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during Stop. The default is 1.

# **EPROM Selectable Options**

There are seven EPROM Selectable Options to choose from based on ROM code requirements. These options are listed in Table 24.

#### Table 24. EPROM Selectable Options

Port 00–03 Pull-Ups	On/Off
Port 04–07 Pull-Ups	On/Off
Port 10–13 Pull-Ups	On/Off
Port 14–17 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
EPROM Protection	On/Off
Watch-Dog Timer at Power-On Reset	On/Off

# Voltage Brown-Out/Standby

An on-chip Voltage Comparator checks that the V<sub>DD</sub> is at the required level for correct operation of the device. Reset is globally driven when V<sub>DD</sub> falls below V<sub>BO</sub>. A small drop in V<sub>DD</sub> causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. If the V<sub>DD</sub> is allowed to stay above V<sub>RAM</sub>, the RAM content is preserved. When the power level is returned to above V<sub>BO</sub>, the device performs a POR and functions normally.





СП	R1(0L	))01H							
D7	D6	D5	D4	D3	D2	D1	D0		
									Transmit Mode* R/W 0 T16_OUT is 0 initially 1 T16_OUT is 1 initially Demodulation Mode R 0 No Falling Edge Detection R 1 Falling Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* R/W 0 T8_OUT is 0 initially* 1 T8_OUT is 1 initially Demodulation Mode R 0 No Rising Edge Detection R 1 Rising Edge Detection W 0 No Effect W 1 Reset Flag to 0 Transmit Mode* 0 0 Normal Operation* 0 1 Ping-Pong Mode 1 0 T16_OUT = 0 1 1 T16_OUT = 1 Demodulation Mode 0 0 No Filter 0 1 4 SCLK Cycle Filter 1 0 8 SCLK Cycle Filter 1 0 R SCLK Cycle Filter 1 0 R 1 0 NOR 1 1 NAND Demodulation Mode 0 0 0 Falling Edge Detection
									<ul> <li>0 0 Falling Edge Detection</li> <li>0 1 Rising Edge Detection</li> <li>1 0 Both Edge Detection</li> <li>1 1 Reserved</li> <li>Transmit Mode*</li> </ul>
	L								0 P36 as Port Output * 1 P36 as T8/T16_OUT Demodulation Mode 0 P31 as Demodulator Input 1 P20 as Demodulator Input
* De **De recc	efault se efault se overy.	etting after etting aft	er Res er Res	et et Not	reset v	with a S	Stop-N	lode	Transmit/Demodulation Mode 0 Transmit Mode * 1 Demodulation Mode

Figure 40. T8 and T16 Common Control Functions ((0D)01H: Read/Write)



# CTR2(0D)02H



Figure 41. T16 Control Register ((0D) 2H: Read/Write Except Where Noted)



MILLIMETER

MAX

2.65

0.30

2.44

0.46

0.30

12.95

7.60

10.65

0.40

1.00

1.07

1.27 BSC



INCH

мах

.104

.012

.096

.018

.012

.510

.299

.419

.016

.039

.042

.050 BSC

MIN

.094

.004

.088

.014

.009

.496

.291

.394

.012

.024

.038



Figure 60. 20-Pin SOIC Package Diagram

PS023803-0305







	MILLIMETER		INCH		
MIN	NOM	MAX	MIN	NOM	MAX
1.73	1.85	1.98	0.068	0.073	0.078
0.05	0.13	0.21	0.002	0.005	0.008
1.68	1.73	1.83	0.066	0.068	0.072
0.25	0.30	0.38	0.010	0.012	0.015
0.13	0.15	0.22	0.005	0.006	0.009
7.07	7.20	7.33	0.278	0.283	0.289
5.20	5.30	5.38	0.205	0.209	0.212
	0.65 BSC			0.0256 BSC	;
7.65	7.80	7.90	0.301	0.307	0.311
0.56	0.75	0.94	0.022	0.030	0.037
0.74	0.78	0.82	0.029	0.031	0.032
	MIN 1.73 0.05 1.68 0.25 0.13 7.07 5.20 7.65 0.56 0.74	MILLIMETER           MIN         NOM           1.73         1.85           0.05         0.13           1.68         1.73           0.25         0.30           0.13         0.15           7.07         7.20           5.20         5.30           0.65         BSC           7.65         7.80           0.56         0.75           0.74         0.78	MILLIMETER           MIN         NOM         MAX           1.73         1.85         1.98           0.05         0.13         0.21           1.68         1.73         1.83           0.25         0.30         0.38           0.13         0.15         0.22           7.07         7.20         7.33           5.20         5.30         5.38           0.65 BSC           7.65         7.80         7.90           0.56         0.75         0.94           0.74         0.78         0.82	MILLIMETER         MIN         NOM         MAX         MIN           1.73         1.85         1.98         0.068           0.05         0.13         0.21         0.002           1.68         1.73         1.83         0.066           0.25         0.30         0.38         0.010           0.13         0.15         0.22         0.005           7.07         7.20         7.33         0.278           5.20         5.30         5.38         0.205           7.65         7.80         7.90         0.301           0.56         0.75         0.94         0.022           0.74         0.78         0.82         0.029	MILLIMETER         INCH           MIN         NOM         MAX         MIN         NOM           1.73         1.85         1.98         0.068         0.073           0.05         0.13         0.21         0.002         0.005           1.68         1.73         1.83         0.066         0.068           0.25         0.30         0.38         0.010         0.012           0.13         0.15         0.22         0.005         0.006           7.07         7.20         7.33         0.278         0.283           5.20         5.30         5.38         0.205         0.209           O.055 BSC           7.65         7.80         7.90         0.301         0.307           0.56         0.75         0.94         0.022         0.030           0.74         0.78         0.82         0.029         0.31



DETAIL A

Н

CONTROLLING DIMENSIONS : MM LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 61. 20-Pin SSOP Package Diagram











Figure 63. 28-Pin CDIP Package Diagram



SVMBOI	OPT #	MILLIN	IETER	INC	H	
SIMDOL	011#	MíN	MAX	MIN	MAX	
A1		0.38	1.02	.015	.040	
A2		3.18	4.19	.125	.165	
В		0.38	0.53	.015	.021	
<b>P1</b>	01	1.40	1.65	.055	.065	
	02	1.14	1.40	.045	.055	
С		0.23	0.38	.009	.015	
D	01	36.58	37.34	1.440	1.470	
	02	35.31	35.94	1.390	1.415	
E		15.24	15.75	.600	.620	
E1	01	13.59	14.10	.535	.555	
	02	12.83	13.08	.505	.515	
e		2.54	TYP	.100 BSC		
eA		15.49	16.76	.610	.660	
L		3.05	3.81	.120	.150	
01	01	1.40	1.91	.055	.075	
	02	1.40	1.78	.055	.070	
•	01	1.52	2.29	.060	.090	
5	02	1.02	1.52	.040	.060	

CONTROLLING DIMENSIONS : INCH



01

02

STANDARD

Figure 64. 28-Pin PDIP Package Diagram



# **Ordering Information**

#### 32KB Standard Temperature: 0° to +70°C

-			
Part Number	Description	Part Number	Description
ZGP323HSH4832C	48-pin SSOP 32K OTP	ZGP323HSS2832C	28-pin SOIC 32K OTP
ZGP323HSP4032C	40-pin PDIP 32K OTP	ZGP323HSH2032C	20-pin SSOP 32K OTP
ZGP323HSK2832E	28-pin CDIP 32K OTP	ZGP323HSK2032E	20-pin CDIP 32K OTP
ZGP323HSK4032E	40-pin CDIP 32K OTP	ZGP323HSP2032C	20-pin PDIP 32K OTP
ZGP323HSH2832C	28-pin SSOP 32K OTP	ZGP323HSS2032C	20-pin SOIC 32K OTP
ZGP323HSP2832C	28-pin PDIP 32K OTP		

#### 32KB Extended Temperature: -40° to +105°C

Part Number	Description	Part Number	Description
ZGP323HEH4832C	48-pin SSOP 32K OTP	ZGP323HES2832C	28-pin SOIC 32K OTP
ZGP323HEP4032C	40-pin PDIP 32K OTP	ZGP323HEH2032C	20-pin SSOP 32K OTP
ZGP323HEH2832C	28-pin SSOP 32K OTP	ZGP323HEP2032C	20-pin PDIP 32K OTP
ZGP323HEP2832C	28-pin PDIP 32K OTP	ZGP323HES2032C	20-pin SOIC 32K OTP

32KB Automotive Temperature: -40° to +125°C			
Part Number	Description	Part Number	Description
ZGP323HAH4832C	48-pin SSOP 32K OTP	ZGP323HAS2832C	28-pin SOIC 32K OTP
ZGP323HAP4032C	40-pin PDIP 32K OTP	ZGP323HAH2032C	20-pin SSOP 32K OTP
ZGP323HAH2832C	28-pin SSOP 32K OTP	ZGP323HAP2032C	20-pin PDIP 32K OTP
ZGP323HAP2832C	28-pin PDIP 32K OTP	ZGP323HAS2032C	20-pin SOIC 32K OTP
Replace C with G fo	r Lead-Free Packaging		

#### ZGP323H Z8<sup>®</sup> OTP Microcontroller with IR Timers



pin 4 Ε **EPROM** selectable options 64 expanded register file 26 expanded register file architecture 28 expanded register file control registers 71 flag 80 interrupt mask register 79 interrupt priority register 78 interrupt request register 79 port 0 and 1 mode register 77 port 2 configuration register 75 port 3 mode register 76 port configuration register 75 register pointer 80 stack pointer high register 81 stack pointer low register 81 stop-mode recovery register 73 stop-mode recovery register 2 74 T16 control register 69 T8 and T16 common control functions register 67 T8/T16 control register 70 TC8 control register 66 watch-dog timer register 75 F features standby modes 1 functional description counter/timer functional blocks 40 CTR(D)01h register 35 CTR0(D)00h register 33 CTR2(D)02h register 37 CTR3(D)03h register 39 expanded register file 26 expanded register file architecture 28 HI16(D)09h register 32 HI8(D)0Bh register 32 L08(D)0Ah register 32 L0I6(D)08h register 32

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