Zilog - ZGP323HSS2816G Datasheet





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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	HLVD, POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/zgp323hss2816g

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Table 3. Power Connections

Connection	Circuit	Device	
Power	V _{CC}	V _{DD}	
Ground	GND	V _{SS}	



Note: Refer to the specific package for available pins.

Figure 1. Functional Block Diagram



T _Δ =0°C to +70°C								
Symbol	Parameter	V _{CC}	Min	Typ(7)	Мах	Units	Conditions	Notes
I _{OL}	Output Leakage	2.0-5.5	-1		1	μA	$V_{IN} = 0V, V_{CC}$	
Icc	Supply Current	2.0V		1	3	mA	at 8.0 MHz	1, 2
		3.6V		5	10	mA	at 8.0 MHz	1, 2
		5.5V		10	15	mA	at 8.0 MHz	1, 2
I _{CC1}	Standby Current	2.0V		0.5	1.6	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
	(HALT Mode)	3.6V		0.8	2.0	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
		5.5V		1.3	3.2	mA	V _{IN} = 0V, Clock at 8.0MHz	1, 2, 6
I _{CC2}	Standby Current (Stop	2.0V		1.6	8	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
	Mode)	3.6V		1.8	10	μA	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
		5.5V		1.9	12	μΑ	$V_{IN} = 0 V, V_{CC} WDT not Running$	3
		2.0V		5	20	μΑ	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		3.6V		8	30	μΑ	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
		5.5V		15	45	μΑ	$V_{IN} = 0 V, V_{CC} WDT$ is Running	3
I _{LV}	Standby Current (Low Voltage)			1.2	6	μA	Measured at 1.3V	4
V _{BO}	V _{CC} Low Voltage			1.9	2.0	V	8MHz maximum	
20	Protection						Ext. CLK Freq.	
V _{LVD}	V _{CC} Low Voltage			2.4		V		
	Detection							
V _{HVD}	Vcc High Voltage			2.7		V		
	Detection							

Table 9. GP323HS DC Characteristics (Continued)

Notes:

1. All outputs unloaded, inputs at rail.

2. CL1 = CL2 = 100 pF.

3. Oscillator stopped.

4. Oscillator stops when V_{CC} falls below V_{BO} limit.

 It is strongly recommended to add a filter capacitor (minimum 0.1 μF), physically close to VCC and V_{SS} pins if operating voltage fluctuations are anticipated, such as those resulting from driving an Infrared LED.

- 6. Comparator and Timers are on. Interrupt disabled.
- 7. Typical values shown are at 25 degrees C.

Table 10. GP323HE DC Characteristics

T _A = -40°C to +105°C								
Symbol	Parameter	V _{CC}	Min	Typ(7)	Max	Units	Conditions	Notes
V _{CC}	Supply Voltage		2.0		5.5	V	See Note 5	5
V _{CH}	Clock Input High Voltage	2.0-5.5	0.8 V _{CC}		V _{CC} +0.3	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	2.0-5.5	V _{SS} -0.3		0.4	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	2.0-5.5	0.7 V _{CC}		V _{CC} +0.3	V		
V _{IL}	Input Low Voltage	2.0-5.5	V _{SS} 0.3		0.2 V _{CC}	V		
V _{OH1}	Output High Voltage	2.0-5.5	V _{CC} -0.4			V	I _{OH} = -0.5mA	



AC Characteristics





Figure 8. AC Timing Diagram



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The upper nibble of the register pointer (see Figure 16) selects which working register group, of 16 bytes in the register file, is accessed out of the possible 256. The lower nibble selects the expanded register file bank and, in the case of the Z8 GP family, banks 0, F, and D are implemented. A OH in the lower nibble allows the normal register file (bank 0) to be addressed. Any other value from 1H to FH exchanges the lower 16 registers to an expanded register bank.





Figure 16. Register Pointer

Example: Z8 GP: (See Figure 15 on page 28)

R253 RP = 00h R0 = Port 0 R1 = Port 1 R2 = Port 2 R3 = Port 3

But if:

R253 RP = 0Dh R0 = CTR0 R1 = CTR1 R2 = CTR2R3 = Reserved



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When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, D1). If the initial value (CTR1, D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter. In SINGLE-PASS Mode (CTR0, D6), T8 counts down to 0 and stops, T8_OUT toggles, the timeout status bit (CTR0, D5) is set, and a timeout interrupt can be generated if it is enabled (CTR0, D1). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the timeout status bit (CTR0, D5), thereby generating an interrupt if enabled (CTR0, D1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 20.



Figure 20. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.



Caution: To ensure known operation do not write these registers at the time the values are to be loaded into the counter/timer. *An initial count of 1 is not allowed (a non-function occurs).* An initial count of 0 causes TC8 to count from 0 to FFH to FEH.



Note: The letter h denotes hexadecimal values.

Transition from 0 to FFh is not a timeout condition.



Caution: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended.

Two successive commands are necessary. First, the counter/timers must be stopped. Second, the status bits must be reset. These commands are required because it takes one counter/timer clock interval for the initiated event to actually occur. See Figure 21 and Figure 22.







Figure 22. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user must program TC8L and TC8H to FFH. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1, D5; D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1, D5; D4) is detected during counting, the current value of T8 is complemented and put into one of the capture registers. If it is a positive edge, data is put





Figure 30. Interrupt Block Diagram



Port 0 Output Mode (D2)

Bit 2 controls the output mode of port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop Mode Recovery (Figure 33). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of Stop recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XORgate input (Figure 35 on page 59) is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop Mode Recovery signal. Bits D0 determines if SCLK/ TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address OBH.







Figure 34. SCLK Circuit

Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the Stop recovery (Figure 35 and Table 22).

Stop-Mode Recovery Register 2—SMR2(F)0DH

Table 21 lists and briefly describes the fields for this register.

Field	Bit Position		Value	Description
Reserved	7		0	Reserved (Must be 0)
Recovery Level	-6	W	0 [†]	Low
-			1	High
Reserved	5		0	Reserved (Must be 0)
Source	432	W	000†	A. POR Only
			001	B. NAND of P23–P20
			010	C. NAND of P27–P20
			011	D. NOR of P33–P31
			100	E. NAND of P33–P31
			101	F. NOR of P33–P31, P00, P07
			110	G. NAND of P33–P31, P00, P07
			111	H. NAND of P33–P31, P22–P20
Reserved	10		00	Reserved (Must be 0)

Table 21.SMR2(F)0DH:Stop	Mode Recovery	Register	2*
--------------------------	---------------	----------	----

Notes:

* Port pins configured as outputs are ignored as a SMR recovery source. † Indicates the value upon Power-On Reset





CTR3(0D)03H

D7	D6	D5	D4	D3	D2	D1	D0	
							DU	Reserved No effect when written Always reads 11111 Sync Mode 0* Disable Sync Mode** 1 Enable Sync Mode T ₈ Enable R 0* T ₈ Enabled R 1 T ₈ Enabled
								W0 Stop T ₈ W1 Enable T ₈
								T ₁₆ Enable R 0* T ₁₆ Disabled R 1 T ₁₆ Enabled W 0 Stop T ₁₆ W 1 Enable T ₁₆

* Default setting after reset. ** Default setting after reset. Not reset with a Stop Mode recovery.

Figure 42. T8/T16 Control Register (0D)03H: Read/Write (Except Where Noted)



LVD(0D)0CH



* Default setting after reset.

Figure 43. Voltage Detection Register

Note: Do not modify register P01M while checking a low-voltage condition. Switching noise of both ports 0 and 1 together might trigger the LVD flag.

Expanded Register File Control Registers (0F)

The expanded register file control registers (0F) are depicted in Figures 44 through Figure 57.



R247 P3M(F7H)



* Default setting after reset. Not reset with a Stop Mode recovery.

Figure 49. Port 3 Mode Register (F7H: Write Only)









Figure 58. 20-Pin CDIP Package





Figure 59. 20-Pin PDIP Package Diagram





CONTROLLING DIMENSIONS : INCH









Figure 68. 48-Pin SSOP Package Design

Note: Check with ZiLOG on the actual bonding diagram and coordinate for chip-on-board assembly.



16KB Standard Temperature: 0° to +70°C

Part Number	Description	Part Number	Description
ZGP323HSH4816C	48-pin SSOP 16K OTP	ZGP323HSS2816C	28-pin SOIC 16K OTP
ZGP323HSP4016C	40-pin PDIP 16K OTP	ZGP323HSH2016C	20-pin SSOP 16K OTP
ZGP323HSH2816C	28-pin SSOP 16K OTP	ZGP323HSP2016C	20-pin PDIP 16K OTP
ZGP323HSP2816C	28-pin PDIP 16K OTP	ZGP323HSS2016C	20-pin SOIC 16K OTP

16KB Extended Temperature: -40° to +105°C							
Part Number	Description	Part Number	Description				
ZGP323HEH4816C	48-pin SSOP 16K OTP	ZGP323HES2816C	28-pin SOIC 16K OTP				
ZGP323HEP4016C	40-pin PDIP 16K OTP	ZGP323HEH2016C	20-pin SSOP 16K OTP				
ZGP323HEH2816C	28-pin SSOP 16K OTP	ZGP323HEP2016C	20-pin PDIP 16K OTP				
ZGP323HEP2816C	28-pin PDIP 16K OTP	ZGP323HES2016C	20-pin SOIC 16K OTP				

16KB Automotive Temperature: -40° to +125°CPart NumberDescriptionPart NumberDescriptionZGP323HAH4816C48-pin SSOP 16K OTPZGP323HAS2816C28-pin SOIC 16K OTPZGP323HAP4016C40-pin PDIP 16K OTPZGP323HAH2016C20-pin SSOP 16K OTPZGP323HAH2816C28-pin SSOP 16K OTPZGP323HAP2016C20-pin PDIP 16K OTPZGP323HAP2816C28-pin PDIP 16K OTPZGP323HAS2016C20-pin SOIC 16K OTPZGP323HAP2816C28-pin PDIP 16K OTPZGP323HAS2016C20-pin SOIC 16K OTPReplace C with G for Lead-Free Packaging



For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

ZG = ZiLOG General Purpose Family

P = OTP

- 323 = Family Designation
- H = High Voltage
- T = Temparature
 - S = Standard 0° to +70°C
 - $E = Extended 40^{\circ} to + 105^{\circ}C$
 - A = Automotive -40° to $+125^{\circ}$ C
- P = Package Type:
 - K = CDIP
 - P = PDIP
 - H = SSOP
 - S = SOIC

= Number of Pins

- CC = Memory Size
- M = Molding Compound
- C = Standard Plastic Packaging Molding Compound
- G = Green Plastic Molding Compound
- E = Standard Cer Dip flow



Example



ZGP323H Z8[®] OTP Microcontroller with IR Timers



pin 4 Ε **EPROM** selectable options 64 expanded register file 26 expanded register file architecture 28 expanded register file control registers 71 flag 80 interrupt mask register 79 interrupt priority register 78 interrupt request register 79 port 0 and 1 mode register 77 port 2 configuration register 75 port 3 mode register 76 port configuration register 75 register pointer 80 stack pointer high register 81 stack pointer low register 81 stop-mode recovery register 73 stop-mode recovery register 2 74 T16 control register 69 T8 and T16 common control functions register 67 T8/T16 control register 70 TC8 control register 66 watch-dog timer register 75 F features standby modes 1 functional description counter/timer functional blocks 40 CTR(D)01h register 35 CTR0(D)00h register 33 CTR2(D)02h register 37 CTR3(D)03h register 39 expanded register file 26 expanded register file architecture 28 HI16(D)09h register 32 HI8(D)0Bh register 32 L08(D)0Ah register 32 L0I6(D)08h register 32

program memory map 26 **RAM 25** register description 65 register file 30 register pointer 29 register pointer detail 31 SMR2(F)0D1h register 40 stack 31 TC16H(D)07h register 32 TC16L(D)06h register 33 TC8H(D)05h register 33 TC8L(D)04h register 33 G glitch filter circuitry 40 Η halt instruction, counter/timer 54 input circuit 40 interrupt block diagram, counter/timer 51 interrupt types, sources and vectors 52 L low-voltage detection register 65 Μ memory, program 25 modulo-N mode T16 OUT 47 T8 OUT 43 0 oscillator configuration 53 output circuit, counter/timer 49 Ρ package information 20-pin DIP package diagram 82 20-pin SSOP package diagram 84 28-pin DIP package diagram 86 28-pin SOIC package diagram 85 28-pin SSOP package diagram 87 40-pin DIP package diagram 87 48-pin SSOP package diagram 89 pin configuration 20-pin DIP/SOIC/SSOP 5