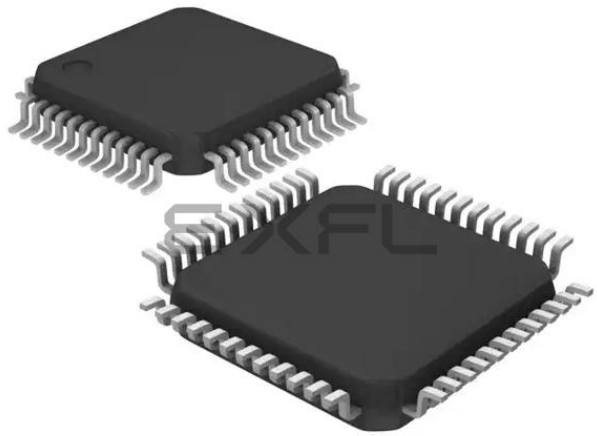

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Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	39
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8036vlf

In **Table 2-2**, peripheral pins in bold identify reset state.

Table 2-2 56F8036 Pins

			Peripherals:											
Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**QSCI**	**QSPI**	**ADC**	**PWM**	**Quad Timer**	**Comp**	**MSCAN**	**Power & Ground**	**JTAG**	**Misc**
1	**GPIOB6**	GPIOB6, RXD0, SDA, CLKIN	**B6**	SDA	RXD0									CLKIN
2	**GPIOB1**	GPIOB1, $\overline{SS0}$, SDA	**B1**	SDA		$\overline{SS0}$								
3	**GPIOB7**	GPIOB7, TXD0, SCL	**B7**	SCL	TXD0									
4	**GPIOB5**	GPIOB5, TA1, FAULT3, CLKIN	**B5**					FAULT3	TA1					CLKIN
5	**GPIOA9**	GPIOA9, FAULT2, TA3, CMPBI1	**A9**					FAULT2	TA3	CMPBI1				
6	**GPIOA11**	GPIOA11, CMPBI2	**A11**							CMPBI2				
7	**GPIOC12**	GPIOC12, ANB4	**C12**				ANB4							
8	**GPIOC4**	GPIOC4, ANB0, CMPBI3	**C4**				ANB0			CMPBI3				
9	**GPIOC5**	GPIOC5, ANB1	**C5**				ANB1							
10	**GPIOC6**	GPIOC6, ANB2, V_{REFHB}	**C6**				ANB2 V_{REFHB}							
11	**GPIOC7**	GPIOC7, ANB3, V_{REFLB}	**C7**				ANB3 V_{REFLB}							
12	**VDDA**	V_{DDA}										V_{DDA}		
13	**VSSA**	V_{SSA}										V_{SSA}		
14	**GPIOC3**	GPIOC3, ANA3, V_{REFLA}	**C3**				ANA3 V_{REFLA}							
15	**GPIOC2**	GPIOC2, ANA2, V_{REFHA}	**C2**				ANA2 V_{REFHA}							
16	**GPIOC1**	GPIOC1, ANA1	**C1**				ANA1							
17	**GPIOC0**	GPIOC0, ANA0, CMPAI3	**C0**				ANA0			CMPAI3				
18	**GPIOC8**	GPIOC8, ANA4	**C8**				ANA4							
19	**VSS**	V_{SS}										V_{SS}		
20	**VCAP**	V_{CAP}										**V_{CAP}**		
21	**TCK**	TCK, GPIOD2	D2										**TCK**	
22	**GPIOB10**	GPIOB10, CMPAO,	**B10**							CMPAO				
23	**RESET**	$\overline{RESET}$, GPIOA7	A7											**$\overline{RESET}$**
24	**GPIOB3**	GPIOB3, MOSI0, TA3, PSRC1	**B3**			MOSI0		PSRC1	TA3					
25	**GPIOB2**	GPIOB2, MISO0, TA2, PSRC0	**B2**			MISO0		PSRC0	TA2					
26	**GPIOA6**	GPIOA6, FAULT0, TA0	**A6**					FAULT0	TA0					
27	**GPIOA10**	GPIOA10, CMPAI2	**A10**							CMPAI2				

Table 2-3 56F8036 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA0 **(PWM0)**	44	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM0** — This is one of the six PWM output pins. After reset, the default state is GPIOA0.
GPIOA1 **(PWM1)**	43	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM1** — This is one of the six PWM output pins. After reset, the default state is GPIOA1.
GPIOA2 **(PWM2)**	35	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM2** — This is one of the six PWM output pins. After reset, the default state is GPIOA2.
GPIOA3 **(PWM3)**	36	Input/ Output Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin. **PWM3** — This is one of the six PWM output pins. After reset, the default state is GPIOA3.

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Table 2-3 56F8036 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOB8 **(SCL[11])** **(CANTX[12])**	42	Input/ Output Input/ Output Open Drain Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **Serial Clock 1** — This pin serves as the I^2C serial clock. **CAN Transmit Data** — This is the SCAN interface output. After reset, the default state is GPIOB8. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[11]The SCL signal is also brought out on the GPIOB0 and GPIOB7 pins. [12]The CANTX signal is also brought out on the GPIOB12 pin.				
GPIOB9 **(SDA[13])** **(CANRX[14])**	34	Input/ Output Input/ Output Input	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **Serial Data 1** — This pin serves as the I^2C serial data line. **CAN Receive Data** — This is the MSCAN interface input. After reset, the default state is GPIOB9. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[13]The SDA signal is also brought out on the GPIOB1 and GPIOB6 pins. [14]The CANRX signal is also brought out on the GPIOB13 pin.				
GPIOB10 **(CMPAO)**	22	Input/ Output Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **Comparator A Output**— This is the output of comparator A. After reset, the default state is GPIOB10. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
GPIOB11 **(CMPBO)**	46	Input/ Output Output	Input, internal pull-up enabled	**Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. **Comparator B Output**— This is the output of comparator B. After reset, the default state is GPIOB11. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.

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Table 2-3 56F8036 Signal and Package Information for the 48-Pin LQFP (Continued)

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOC0 **(ANA0 & CMPAI3)**	17	Input/ Output Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANA0** — Analog input to ADC A, Channel 0. **Comparator A, Input 3** — This is an analog input to Comparator A. When used as an analog input, the signal goes to both the ANA0 and CMPAI3. After reset, the default state is GPIOC0.
GPIOC1 **(ANA1)**	16	Input/ Output Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANA1** — Analog input to ADC A, Channel 1. After reset, the default state is GPIOC1.
GPIOC2 **(ANA2)** **(V_{REFHA})**	15	Input/ Output Analog Input Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANA2** — Analog input to ADC A, Channel 2. **V_{REFHA}** — Analog reference voltage high (ADC A). After reset, the default state is GPIOC2.
GPIOC3 **(ANA3)** **(V_{REFLA})**	14	Input/ Output Analog Input Analog Input	Input	**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. **ANA3** — Analog input to ADC A, Channel 3. **V_{REFLA}** — Analog reference voltage low (ADC A). After reset, the default state is GPIOC3.

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Table 4-2 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
ADC	60	0-2	P:$78	ADC Zero Crossing or Limit Error
PWM	61	0-2	P:$7A	Reload PWM
PWM	62	0-2	P:$7C	PWM Fault
SWILP	63	-1	P:$7E	SW Interrupt Low Priority

1. Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.
2. If the VBA is set to the reset value, the first two locations of the vector table will overlay the chip reset addresses since the reset address would match the base of this vector table.

4.3 Program Map

The Program Memory map is shown in **Table 4-3**.

Table 4-3 Program Memory Map[1] at Reset

Begin/End Address	Memory Allocation
P: $1F FFFF P: $00 8800	RESERVED
P: $00 87FF P: $00 8000	On-Chip RAM[2] 8KB
P: $00 7FFF P: $00 0000	Internal Program Flash 64KB Cop Reset Address = $00 0002 Boot Location = $00 0000

1. All addresses are 16-bit Word addresses.
2. This RAM is shared with Data space starting at address X: $00 0000; see **Figure 4-1**.

Table 4-14 Power Supervisor Registers Address Map (PS_BASE = $00 F140)

Register Acronym	Address Offset	Register Description
PS_CTRL	$0	Control Register
PS_STAT	$1	Status Register
		Reserved

Table 4-15 GPIOA Registers Address Map (GPIOA_BASE = $00 F150)

Register Acronym	Address Offset	Register Description
GPIOA_PUPEN	$0	Pull-up Enable Register
GPIOA_DATA	$1	Data Register
GPIOA_DDIR	$2	Data Direction Register
GPIOA_PEREN	$3	Peripheral Enable Register
GPIOA_IASSRT	$4	Interrupt Assert Register
GPIOA_IEN	$5	Interrupt Enable Register
GPIOA_IEPOL	$6	Interrupt Edge Polarity Register
GPIOA_IPEND	$7	Interrupt Pending Register
GPIOA_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOA_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOA_RDATA	$A	Raw Data Input Register
GPIOA_DRIVE	$B	Output Drive Strength Control Register

Table 4-16 GPIOB Registers Address Map (GPIOB_BASE = $00 F160)

Register Acronym	Address Offset	Register Description
GPIOB_PUPEN	$0	Pull-up Enable Register
GPIOB_DATA	$1	Data Register
GPIOB_DDIR	$2	Data Direction Register
GPIOB_PEREN	$3	Peripheral Enable Register
GPIOB_IASSRT	$4	Interrupt Assert Register
GPIOB_IEN	$5	Interrupt Enable Register
GPIOB_IEPOL	$6	Interrupt Edge Polarity Register
GPIOB_IPEND	$7	Interrupt Pending Register
GPIOB_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOB_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOB_RDATA	$A	Raw Data Input Register
GPIOB_DRIVE	$B	Output Drive Strength Control Register

5.3.1 Normal Interrupt Handling

Once the INTC has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the Vector Base Address (VBA) and the vector number to determine the vector address, generating an offset into the vector table for each interrupt.

5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The 56800E core controls the masking of interrupt priority levels it will accept by setting the I0 and I1 bits in its status register.

Table 5-1 Interrupt Mask Bit Definition

SR[9] (I1)	SR[8] (I0)	Exceptions Permitted	Exceptions Masked
0	0	Priorities 0, 1, 2, 3	None
0	1	Priorities 1, 2, 3	Priority 0
1	0	Priorities 2, 3	Priorities 0, 1
1	1	Priority 3	Priorities 0, 1, 2

The IPIC bits of the ICTRL register reflect the state of the priority level being presented to the 56800E core.

Table 5-2 Interrupt Priority Encoding

IPIC_VALUE[1:0]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3
11	Priority 2 or 3	Priority 3

5.3.3 Fast Interrupt Handling

Fast interrupts are described in the **DSP56800E Reference Manual**. The interrupt controller recognizes Fast Interrupts before the core does.

A Fast Interrupt is defined (to the ITCN) by:

1. Setting the priority of the interrupt as level 2, with the appropriate field in the IPR registers
2. Setting the FIM*n* register to the appropriate vector number
3. Setting the FIVAL*n* and FIVAH*n* registers with the address of the code for the Fast Interrupt

5.6.3.5 GPIOA Interrupt Priority Level (GPIOA IPL)—Bits 5–4

This field is used to set the interrupt priority level for the GPIOA IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.6 GPIOB Interrupt Priority Level (GPIOB IPL)—Bits 3–2

This field is used to set the interrupt priority level for the GPIOB IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.7 GPIOC Interrupt Priority Level (GPIOC IPL)—Bits 1–0

This field is used to set the interrupt priority level for the GPIOC IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4 Interrupt Priority Register 3 (IPR3)

Base + $3	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	I2C_ERR IPL		0	0	0	0	0	0	0	0	QSCI0_RCV IPL		QSCI0_RERR IPL		QSCI0_TIDL IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-6 Interrupt Priority Register 3 (IPR3)

5.6.4.1 I^2C Error Interrupt Priority Level (I2C_ERR IPL)—Bits 15–14

This field is used to set the interrupt priority level for the I^2C Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.1 Timer A, Channel 3 Interrupt Priority Level (TMRA_3 IPL)—Bits 15–14

This field is used to set the interrupt priority level for the Timer A, Channel 3 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.2 Timer A, Channel 2 Interrupt Priority Level (TMRA_2 IPL)—Bits 13–12

This field is used to set the interrupt priority level for the Timer A, Channel 2 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.3 Timer A, Channel 1 Interrupt Priority Level (TMRA_1 IPL)—Bits 11–10

This field is used to set the interrupt priority level for the Timer A, Channel 1 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.4 Timer A, Channel 0 Interrupt Priority Level (TMRA_0 IPL)—Bits 9–8

This field is used to set the interrupt priority level for the Timer A, Channel 0 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.5 I²C Status Interrupt Priority Level (I2C_STAT IPL)—Bits 7–6

This field is used to set the interrupt priority level for the I²C Status IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.6 I²C Transmit Interrupt Priority Level (I2C_TX IPL)—Bits 5–4

This field is used to set the interrupt priority level for the I²C Transmit IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.7 I²C Receive Interrupt Priority Level (I2C_RX IPL)— Bits 3–2

This field is used to set the interrupt priority level for the I²C Receiver IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.5.8 I²C General Call Interrupt Priority Level (I2C_GEN IPL)—Bits 1–0

This field is used to set the interrupt priority level for the I²C General Call IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.6 Interrupt Priority Register 5 (IPR5)

Base + $5	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PIT1 IPL		PIT0 IPL		COMPB IPL		COMPA IPL		0	0	0	0	0	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-8 Interrupt Priority Register 5 (IPR6)

6.3 Register Descriptions

A write to an address without an associated register is an NOP. A read from an address without an associated register returns unknown data.

Table 6-1 SIM Registers (SIM_BASE = $00 F100)

Register Acronym	Base Address +	Register Name	Section Location
CTRL	$0	Control Register	6.3.1
RSTAT	$1	Reset Status Register	6.3.2
SWC0	$2	Software Control Register 0	6.3.3
SWC1	$3	Software Control Register 1	6.3.3
SWC2	$4	Software Control Register 2	6.3.3
SWC3	$5	Software Control Register 3	6.3.3
MSHID	$6	Most Significant Half of JTAG ID	6.3.4
LSHID	$7	Least Significant Half of JTAG ID	6.3.5
PWR	$8	Power Control Register	6.3.6
		Reserved	
CLKOUT	$A	CLKO Select Register	6.3.7
PCR	$B	Peripheral Clock Rate Register	6.3.8
PCE0	$C	Peripheral Clock Enable Register 0	6.3.9
PCE1	$D	Peripheral Clock Enable Register 0	6.3.10
SD0	$E	Stop Disable Register 0	6.3.11
SD1	$F	Stop Disable Register 1	6.3.12
IOSAHI	$10	I/O Short Address Location High Register	6.3.13
IOSALO	$11	I/O Short Address Location Low Register	6.3.14
PROT	$12	Protection Register	6.3.15
GPSA0	$13	GPIO Peripheral Select Register 0 for GPIOA	6.3.16
GPSA1	$14	GPIO Peripheral Select Register 1 for GPIOA	6.3.17
GPSB0	$15	GPIO Peripheral Select Register 0 for GPIOB	6.3.18
GPSB1	$16	GPIO Peripheral Select Register 1 for GPIOB	6.3.19
GPSCD	$17	GPIO Peripheral Select Register for GPIOC and GPIOD	6.3.20
IPS0	$18	Internal Peripheral Source Select Register 0 for PWM	6.3.21
IPSS1	$19	Internal Peripheral Source Select Register 1 for DACs	6.3.22
IPSS2	$1A	Internal Peripheral Source Select Register 2 for Quad Timer A	6.3.23
		Reserved	

6.3.1 SIM Control Register (SIM_CTRL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	ONCE EBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-2 SIM Control Register (SIM_CTRL)

6.3.1.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

6.3.1.2 OnCE Enable (ONCEEBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

Note: Using default state “0” is recommended.

6.3.1.3 Software Reset (SWRST)—Bit 4

- Writing 1 to this field will cause the device to reset
- Read is 0

6.3.1.4 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 = Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 = The 56800E STOP instruction will not cause entry into Stop mode
- 10 = Stop mode will be entered when the 56800E core executes a STOP instruction and the STOP_DISABLE field is write-protected until the next reset
- 11 = The 56800E STOP instruction will not cause entry into Stop mode and the STOP_DISABLE field is write-protected until the next reset

6.3.1.5 Wait Disable (WAIT_DISABLE)—Bits 1–0

- 00 = Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 = The 56800E WAIT instruction will not cause entry into Wait mode
- 10 = Wait mode will be entered when the 56800E core executes a WAIT instruction and the WAIT_DISABLE field is write-protected until the next reset
- 11 = The 56800E WAIT instruction will not cause entry into Wait mode and the WAIT_DISABLE field is write-protected until the next reset

6.3.2 SIM Reset Status Register (SIM_RSTAT)

This read-only register is updated upon any system reset and indicates the cause of the most recent reset. It indicates whether the COP reset vector or regular reset vector (including Power-On Reset, External Reset, Software Reset) in the vector table is used. This register is asynchronously reset during Power-On Reset and subsequently is synchronously updated based on the precedence level of reset inputs. Only the

6.3.8.2 Quad Timer A Clock Rate (TMRA_CR)—Bit 14

This bit selects the clock speed for the Quad Timer A module.

- 0 = Quad Timer A clock rate equals the system clock rate, to a maximum 32MHz (default)
- 1 = Quad Timer A clock rate equals 3X system clock rate, to a maximum 96MHz

6.3.8.3 Pulse Width Modulator Clock Rate (PWM_CR)—Bit 13

This bit selects the clock speed for the PWM module.

- 0 = PWM module clock rate equals the system clock rate, to a maximum 32MHz (default)
- 1 = PWM module clock rate equals 3X system clock rate, to a maximum 96MHz

6.3.8.4 Inter-Integrated Circuit Run Clock Rate (I2C_CR)—Bit 12

This bit selects the clock speed for the I^2C run clock.

- 0 = I^2C module run clock rate equals the system clock rate, to a maximum 32MHz (default)
- 1 = I^2C module run clock rate equals 3X system clock rate, to a maximum 96MHz

6.3.8.5 Reserved—Bits 11–0

This bit field is reserved. Each bit must be set to 0.

6.3.9 Peripheral Clock Enable Register 0 (SIM_PCE0)

The Peripheral Clock Enable register enables or disables clocks to the peripherals as a power savings feature. Significant power savings are achieved by enabling only the peripheral clocks that are in use. When a peripheral's clock is disabled, that peripheral is in Stop mode. Accesses made to a module that has its clock disabled will have no effect. The corresponding peripheral should itself be disabled while its clock is shut off. IPBus writes are not possible.

Setting the PCE bit does not guarantee that the peripheral's clock is running. Enabled peripheral clocks will still become disabled in Stop mode, unless the peripheral's Stop Disable control in the SD*n* register is set to 1.

Note: The MSCAN module supports extended power management capabilities, including Sleep, Stop-in-Wait, and Disable modes. MSCAN clocks are selected by MSCAN control registers. Refer to the **56F802X and 56F803XPeripheral Reference Manual** for details.

Base + $C	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	CMPB	CMPA	DAC1	DAC0	0	ADC	0	0	0	I2C	0	QSCI0	0	QSPI0	0	PWM
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-10 Peripheral Clock Enable Register 0 (SIM_PCE0)

6.3.9.1 Comparator B Clock Enable (CMPB)—Bit 15

- 0 = The clock is not provided to the Comparator B module (the Comparator B module is disabled)
- 1 = The clock is enabled to the Comparator B module

6.3.9.2 Comparator A Clock Enable (CMPA)—Bit 14

- 0 = The clock is not provided to the Comparator A module (the Comparator A module is disabled)
- 1 = The clock is enabled to the Comparator A module

6.3.9.3 Digital-to-Analog Clock Enable 1 (DAC1)—Bit 13

- 0 = The clock is not provided to the DAC1 module (the DAC1 module is disabled)
- 1 = The clock is enabled to the DAC1 module

6.3.9.4 Digital-to-Analog Clock Enable 0 (DAC0)—Bit 12

- 0 = The clock is not provided to the DAC0 module (the DAC0 module is disabled)
- 1 = The clock is enabled to the DAC0 module

6.3.9.5 Reserved—Bit 11

This bit field is reserved. It must be set to 0.

6.3.9.6 Analog-to-Digital Converter Clock Enable (ADC)—Bit 10

- 0 = The clock is not provided to the ADC module (the ADC module is disabled)
- 1 = The clock is enabled to the ADC module

6.3.9.7 Reserved—Bits 9–7

This bit field is reserved. It must be set to 0.

6.3.9.8 Inter-Integrated Circuit IPBus Clock Enable (I2C)—Bit 6

- 0 = The clock is not provided to the I^2C module (the I^2C module is disabled)
- 1 = The clock is enabled to the I^2C module

6.3.9.9 Reserved—Bit 5

This bit field is reserved. It must be set to 0.

6.3.9.10 QSCI 0 Clock Enable (QSCI0)—Bit 4

- 0 = The clock is not provided to the QSCI0 module (the QSCI0 module is disabled)
- 1 = The clock is enabled to the QSCI0 module

6.3.9.11 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

6.3.9.12 QSPI 0 Clock Enable (QSPI0)—Bit 2

- 0 = The clock is not provided to the QSPI0 module (the QSPI0 module is disabled)
- 1 = The clock is enabled to the QSPI0 module

6.3.9.13 Reserved—Bit 1

This bit field is reserved. It must be set to 0.

6.3.9.14 PWM Clock Enable (PWM)—Bit 0

- 0 = The clock is not provided to the PWM module (the PWM module is disabled)
- 1 = The clock is enabled to the PWM module

6.3.10 Peripheral Clock Enable Register 1 (SIM_PCE1)

See **Section 6.3.9** for general information about Peripheral Clock Enable registers.

Base + $D	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	PIT2	PIT1	PIT0	0	0	0	0	0	0	0	0	TA3	TA2	TA1	TA0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-11 Peripheral Clock Enable Register 1 (SIM_PCE1)

6.3.10.1 Reserved—Bit 15

This bit field is reserved. It must be set to 0.

6.3.10.2 Programmable Interval Timer 2 Clock Enable (PIT2)—Bit 14

- 0 = The clock is not provided to the PIT2 module (the PIT2 module is disabled)
- 1 = The clock is enabled to the PIT2 module

6.3.10.3 Programmable Interval Timer 1 Clock Enable (PIT1)—Bit 13

- 0 = The clock is not provided to the PIT1 module (the PIT1 module is disabled)
- 1 = The clock is enabled to the PIT1 module

6.3.10.4 Programmable Interval Timer 0 Clock Enable (PIT0)—Bit 12

- 0 = The clock is not provided to the PIT0 module (the PIT0 module is disabled)
- 1 = The clock is enabled to the PIT0 module

6.3.10.5 Reserved—Bits 11–4

This bit field is reserved. Each bit must be set to 0.

6.3.10.6 Quad Timer A, Channel 3 Clock Enable (TA3)—Bit 3

- 0 = The clock is not provided to the Timer A3 module (the Timer A3 module is disabled)
- 1 = The clock is enabled to the Timer A3 module

6.3.10.7 Quad Timer A, Channel 2 Clock Enable (TA2)—Bit 2

- 0 = The clock is not provided to the Timer A2 module (the Timer A2 module is disabled)
- 1 = The clock is enabled to the Timer A2 module

6.3.10.8 Quad Timer A, Channel 1 Clock Enable (TA1)—Bit 1

- 0 = The clock is not provided to the Timer A1 module (the Timer A1 module is disabled)
- 1 = The clock is enabled to the Timer A1 module

10.1.1 ElectroStatic Discharge (ESD) Model

Table 10-2 56F8036 ESD Protection

Characteristic	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	750	—	—	V

Table 10-3 LQFP Package Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value (LQFP)	Unit	Notes
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	41	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	34	°C/W	1, 2
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	34	°C/W	2
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	29	°C/W	1, 2
Junction to board		$R_{\theta JB}$	24	°C/W	4
Junction to case		$R_{\theta JC}$	8	°C/W	3
Junction to package top	Natural Convection	Ψ_{JT}	2	°C/W	5

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$), was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p, where “s” is the number of signal layers and “p” is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the “case” temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Junction to board thermal resistance, Theta-JB ($R_{\theta JB}$), is a metric of the thermal resistance from the junction to the printed circuit board determined per JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal Characterization Parameter, Psi-JT (Y_{JT}), is the “resistance” from junction to reference point thermocouple on top center of case as defined in JESD51-2. Y_{JT} is a useful value to use to estimate junction temperature in steady state customer environments.
6. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
7. See **Section 12.1** for more details on thermal design considerations.

Table 10-4 Recommended Operating Conditions
($V_{REFL\ x}$= 0V, V_{SSA} = 0V, V_{SS} = 0V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High	V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 1 0		 32 32	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	-0.3		0.8	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DDA} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -4 -8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature (Extended Industrial)	T_A		-40		105	°C
Flash Endurance (Program Erase Cycles)	N_F	T_A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention	T_R	T_J <= 85°C avg	15		—	years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	years

1. Total chip source or sink current cannot exceed 75mA

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC and Comparator Analog Inputs

Pin Group 4: XTAL, EXTAL

Table 10-6 Current Consumption per Power Supply Pin (Continued)

Mode	Conditions	Typical @ 3.3V, 25°C		Maximum@ 3.6V, 25°C	
		I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
STANDBY > STOP	100kHz Device Clock Relaxation Oscillator in Standby mode PLL powered off Processor Core in STOP state All peripheral module and core clocks are off ADC/DAC/Comparator powered off Voltage regulator in Standby mode	540µA	0µA	650µA	1µA
POWERDOWN	Device Clock is off Relaxation Oscillator powered off PLL powered off Processor Core in STOP state All peripheral module and core clocks are off ADC /DAC/Comparator powered off Voltage Regulator in Standby mode	440µA	0µA	550µA	1µA

1. No Output Switching
   All ports configured as inputs
   All inputs Low
   No DC Loads

Table 10-7 Power-On Reset Low-Voltage Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Voltage Interrupt for 3.3V supply[1]	$V_{EI3.3}$	2.58	2.7	—	V
Low-Voltage Interrupt for 2.5V supply[2]	$V_{E12.5}$	—	2.15	—	V
Low-Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power-On Reset[3]	POR	—	1.8	1.9	V

1. When V_{DD} drops below $V_{EI3.3}$, an interrupt is generated.
2. When V_{DD} drops below $V_{EI32.5}$, an interrupt is generated.
3. Power-On Reset occurs whenever the internally regulated 2.5V digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 2.15V or the 3.3V 1/O voltage is below 2.7V, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

10.2.1 Voltage Regulator Specifications

The 56F8036 has two on-chip regulators. One supplies the PLL and relaxation oscillator. It has no external pins and therefore has no external characteristics which must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.5V to the 56F8036's core logic. This regulator requires an external 4.4µF, or greater, capacitor for proper operation. Ceramic and tantalum

10.11 Serial Communication Interface (SCI) Timing

Table 10-16 SCI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud Rate[2]	BR	—	(f_{MAX}/16)	Mbps	—
RXD[3] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns	10-12
TXD[4] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns	10-13
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. Parameters listed are guaranteed by design.
2. f_{MAX} is the frequency of operation of the system clock in MHz, which is 32MHz for the 56F8036 device.
3. The RXD pin in QSCI0 is named RXD0.
4. The TXD pin in QSCI0 is named TXD0.

Figure 10-12 RXD Pulse Width

Figure 10-13 TXD Pulse Width

10.12 Freescale's Scalable Controller Area Network (MSCAN) Timing

Table 10-17 MSCAN Timing[1]

Characteristic	Symbol	Min	Max	Unit
Baud rate	BR_{CAN}	—	1	Mbps
Bus wake-up detection	T_{WAKEUP}	T_{IPBUS}	—	µs

1. Parameters listed are guaranteed by design

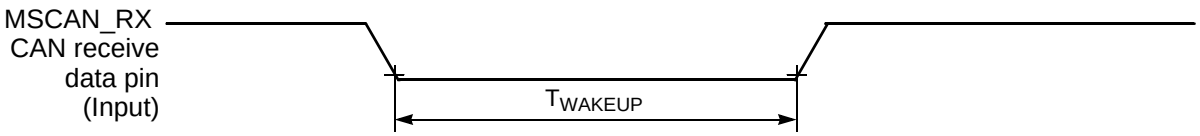

Figure 10-14 Bus Wake-up Detection

10.13 Inter-Integrated Circuit Interface (I^2C) Timing

Table 10-18 I^2C Timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	0[1]	0.9[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250[3]	—	100[3, 4]	—	ns