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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101rct6

Contents

2.1 Device overview

The STM32F101xx high-density access line family offers devices in 3 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

Figure 1 shows the general block diagram of the device family.

Table 2. STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts

Peripherals		STM32F101Rx			STM32F101Vx			STM32F101Zx		
Flash memory in Kbytes		256	384	512	256	384	512	256	384	512
SRAM in Kbytes		32	48		32	48		32	48	
FSMC		No			Yes(1)			Yes		
Timers	General-purpose	4								
	Basic	2								
Comm	SPI	3								
	I^2C	2								
	USART	5								
GPIOs		51			80			112		
12-bit ADC Number of channels		Yes 16			Yes 16			Yes 16		
12-bit DAC Number of channels		1 2								
CPU frequency		36 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperatures		Ambient temperature: –40 to +85 °C (see *Table 10*) Junction temperature: –40 to +105 °C (see *Table 10*)								
Package		LQFP64			LQFP100			LQFP144		

1. For the LQFP100 package, only FSMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.

2.3.11 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 9: Power supply scheme*.

2.3.12 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

2.3.13 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.3.14 Low-power modes

The STM32F101xC, STM32F101xD and STM32F101xE access line supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

2.3.26 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
37	17	26	PA3	I/O	-	PA3	USART2_RX(8)/ TIM5_CH4 / ADC_IN3/ TIM2_CH4(8)	-
38	18	27	V_{SS_4}	S	-	V_{SS_4}	-	-
39	19	28	V_{DD_4}	S	-	V_{DD_4}	-	-
40	20	29	PA4	I/O	-	PA4	SPI1_NSS/ DAC_OUT1 ADC_IN4 / USART2_CK(8)	-
41	21	30	PA5	I/O	-	PA5	SPI1_SCK/ DAC_OUT2/ADC_IN5	-
42	22	31	PA6	I/O	-	PA6	SPI1_MISO / ADC_IN6 / TIM3_CH1(8)	-
43	23	32	PA7	I/O	-	PA7	SPI1_MOSI / ADC_IN7/ TIM3_CH2(8)	-
44	24	33	PC4	I/O	-	PC4	ADC_IN14	-
45	25	34	PC5	I/O	-	PC5	ADC_IN15	-
46	26	35	PB0	I/O	-	PB0	ADC_IN8 / TIM3_CH3(8)	-
47	27	36	PB1	I/O	-	PB1	ADC_IN9/TIM3_CH4(8)	-
48	28	37	PB2	I/O	FT	PB2/BOOT1	-	-
49	-	-	PF11	I/O	FT	PF11	FSMC_NIOS16	-
50	-	-	PF12	I/O	FT	PF12	FSMC_A6	-
51	-	-	V_{SS_6}	S	-	V_{SS_6}	-	-
52	-	-	V_{DD_6}	S	-	V_{DD_6}	-	-
53	-	-	PF13	I/O	FT	PF13	FSMC_A7	-
54	-	-	PF14	I/O	FT	PF14	FSMC_A8	-
55	-	-	PF15	I/O	FT	PF15	FSMC_A9	-
56	-	-	PG0	I/O	FT	PG0	FSMC_A10	-
57	-	-	PG1	I/O	FT	PG1	FSMC_A11	-
58	-	38	PE7	I/O	FT	PE7	FSMC_D4	-
59	-	39	PE8	I/O	FT	PE8	FSMC_D5	-
60	-	40	PE9	I/O	FT	PE9	FSMC_D6	-
61	-	-	V_{SS_7}	S	-	V_{SS_7}	-	-

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
140	62	96	PB9	I/O	FT	PB9	TIM4_CH4 (8)	I2C1_SDA
141	-	97	PE0	I/O	FT	PE0	TIM4_ETR(8)/ FSMC_NBL0	-
142	-	98	PE1	I/O	FT	PE1	FSMC_NBL1	-
143	63	99	V_{SS_3}	S	-	V_{SS_3}	-	-
144	64	100	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and LQFP144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual
8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
9. For devices delivered in LQFP64 packages, the FSMC function is not available.

Table 14. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1) T_A = 85 °C	Unit
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	36 MHz	39	mA
			24 MHz	27	
			16 MHz	20	
			8 MHz	11	
		External clock (2), all peripherals disabled	36 MHz	22	
			24 MHz	16.5	
			16 MHz	12.5	
			8 MHz	8	

1. Guaranteed by characterization results, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15. Maximum current consumption in Run mode, code with data processing running from RAM

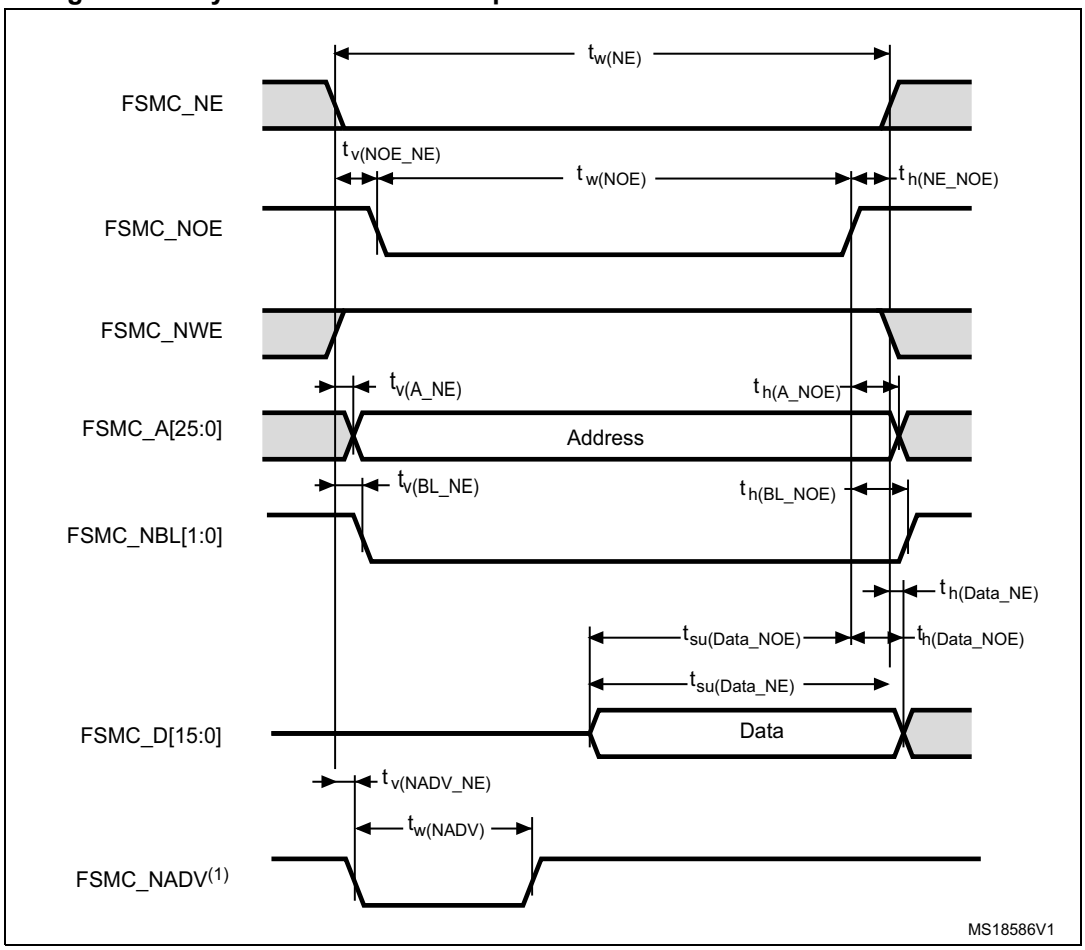
Symbol	Parameter	Conditions	f_{HCLK}	Max(1) T_A = 85 °C	Unit
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	36 MHz	34	mA
			24 MHz	24	
			16 MHz	17	
			8 MHz	10	
		External clock(2) all peripherals disabled	36 MHz	18	
			24 MHz	13	
			16 MHz	10	
			8 MHz	6	

1. Guaranteed by characterization results, tested in production at V_{DD} max, f_{HCLK} max.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 20. Peripheral current consumption(1)

Peripherals		µA/MHz
AHB (up to36 MHz)	DMA1	20.42
	DMA2	19.03
	FSMC	52.36
	CRC	2.36
	BusMatrix(2)	9.72
APB1 (up to 18 MHz)	APB1-Bridge	7.78
	TIM2	33.06
	TIM3	31.94
	TIM4	31.67
	TIM5	31.94
	TIM6	8.06
	TIM7	8.06
	SPI2/I2S2(3)	8.33
	SPI3/I2S3(3)	8.33
	USART2	12.22
	USART3	12.22
	UART4	12.22
	UART5	12.22
	I2C1	10.28
	I2C2	10.00
	USB	18.06
	DAC(4)	8.06
	WWDG	3.89
	PWR	1.11
	BKP	1.11
	IWDG	5.28

Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Note: FSMC_BusTurnAroundDuration = 0.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK} - 1.5$	$5t_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$5t_{HCLK} - 1.5$	$5t_{HCLK} + 1.5$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0.1	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2t_{HCLK} + 25$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$2t_{HCLK} + 25$	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

Table 33. Asynchronous multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	t_{HCLK}	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2t_{HCLK}$ + 24	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 26. Synchronous multiplexed PSRAM write timings

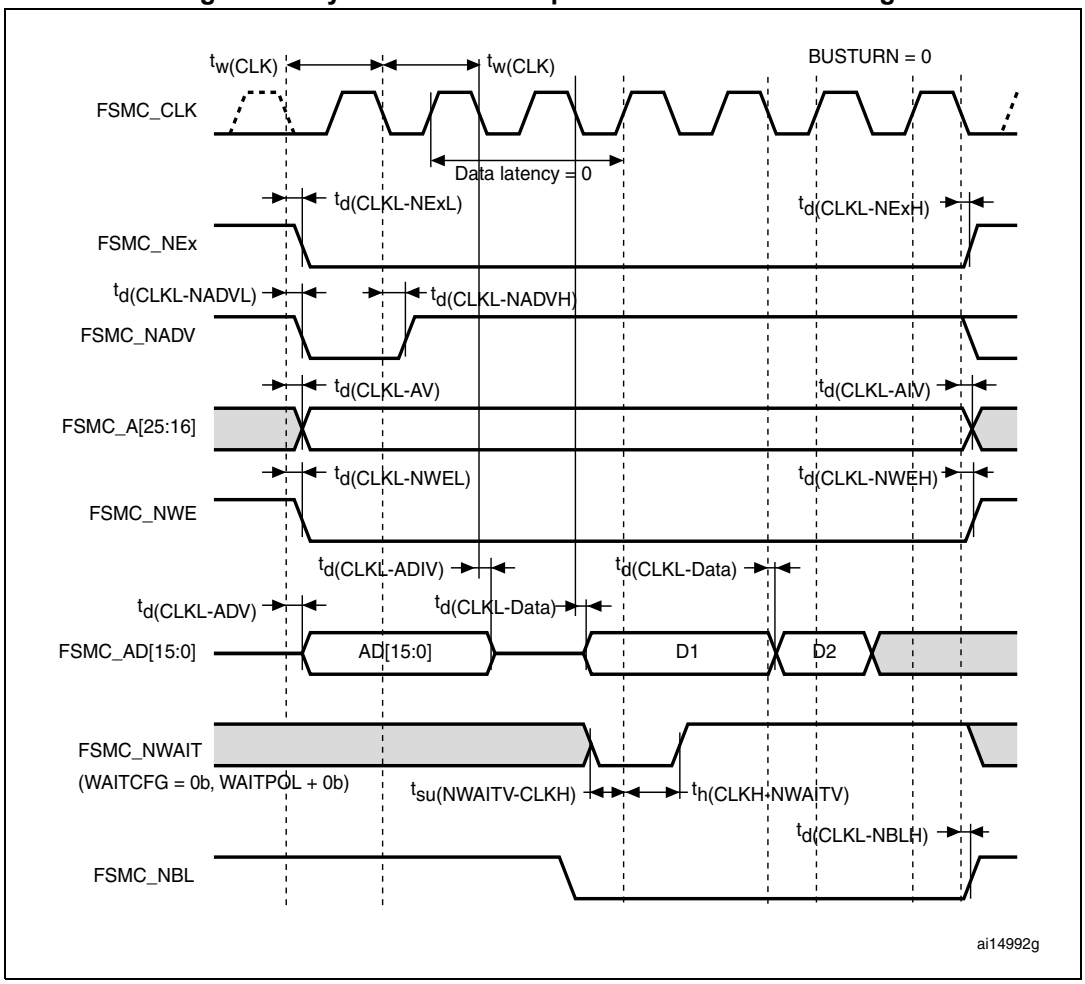


Table 36. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	55.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_Nex low (x = 0...2)	-	2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	3	-	ns
$t_{d(CLKL-Data)}$	FSMC_A/D[15:0] valid after FSMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.

Table 39. Switching characteristics for PC Card/CF read and write cycles(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	$13t_{HCLK}$	-	ns
$t_{w(NIOWR)}$	FSMC_NIOWR low width	$8t_{HCLK}$ + 3	-	ns
$t_{v(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	$5t_{HCLK}$ +1	ns
$t_{h(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	$11t_{HCLK}$	-	ns
$t_{d(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	$5t_{HCLK}$+3ns	ns
$t_{h(NCEx-NIOWR)}$ $t_{h(NCE4\_1-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid	$5t_{HCLK}$ – 5	-	ns
$t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4\_1)}$	FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid	-	$5t_{HCLK}$ + 2.5	ns
$t_{h(NCEx-NIORD)}$ $t_{h(NCE4\_1-NIORD)}$	FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid	$5t_{HCLK}$ – 5	-	ns
$t_{su(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	4.5	-	ns
$t_{d(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	9	-	ns
$t_{w(NIORD)}$	FSMC_NIORD low width	$8t_{HCLK}$ + 2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.

NAND controller waveforms and timings

Figure 35 through *Figure 38* represent synchronous waveforms and *Table 40* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x01;
- COM.FSMC_WaitSetupTime = 0x03;
- COM.FSMC_HoldSetupTime = 0x02;
- COM.FSMC_HiZSetupTime = 0x01;
- ATT.FSMC_SetupTime = 0x01;
- ATT.FSMC_WaitSetupTime = 0x03;
- ATT.FSMC_HoldSetupTime = 0x02;
- ATT.FSMC_HiZSetupTime = 0x01;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 38. NAND controller waveforms for common memory write access

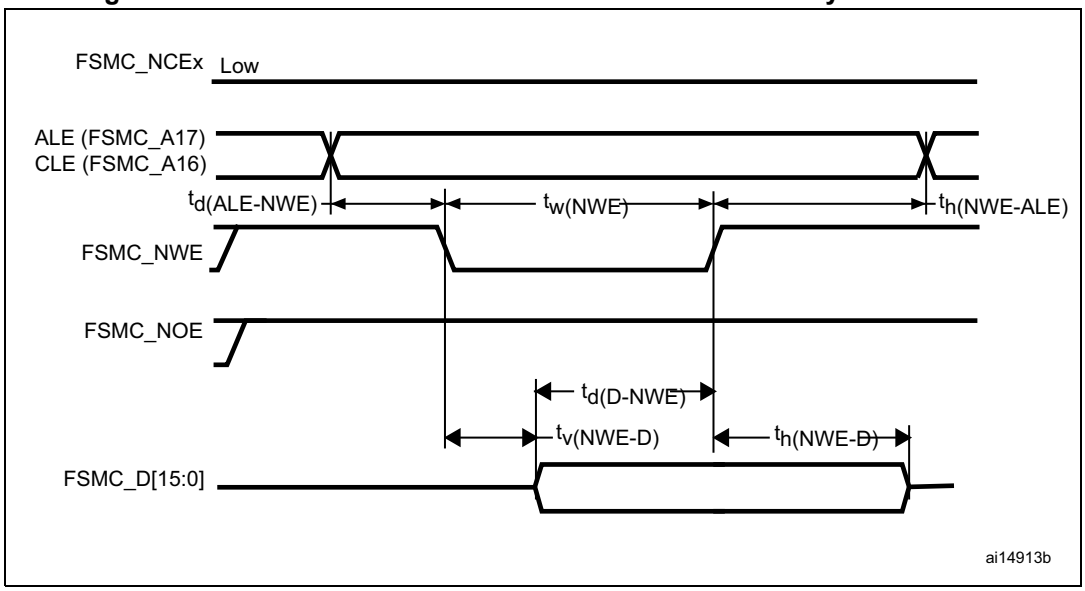


Table 40. Switching characteristics for NAND Flash read and write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$(2)	FSMC_D[15:0] valid before FSMC_NWE high	$5t_{HCLK}$ + 12	-	ns
$t_{w(NOE)}$(2)	FSMC_NOE low width	$4t_{HCLK}$ – 1.5	$4t_{HCLK}$ + 1.5	ns
$t_{su(D-NOE)}$(2)	FSMC_D[15:0] valid data before FSMC_NOE high	25	-	ns
$t_{h(NOE-D)}$(2)	FSMC_D[15:0] valid data after FSMC_NOE high	7	-	ns
$t_{w(NWE)}$(2)	FSMC_NWE low width	$4t_{HCLK}$ – 1	$4t_{HCLK}$ + 2.5	ns
$t_{v(NWE-D)}$(2)	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$(2)	FSMC_NWE high to FSMC_D[15:0] invalid	$2t_{HCLK}$ + 4ns	-	ns
$t_{d(ALE-NWE)}$(3)	FSMC_ALE valid before FSMC_NWE low	-	$3t_{HCLK}$ + 1.5	ns
$t_{h(NWE-ALE)}$(3)	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK}$ + 4.5	-	ns
$t_{d(ALE-NOE)}$(3)	FSMC_ALE valid before FSMC_NOE low	-	$3t_{HCLK}$ + 2	ns
$t_{h(NOE-ALE)}$(3)	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK}$ + 4.5	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 45*

Table 45. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Figure 46. SPI timing diagram - slave mode and CPHA=0

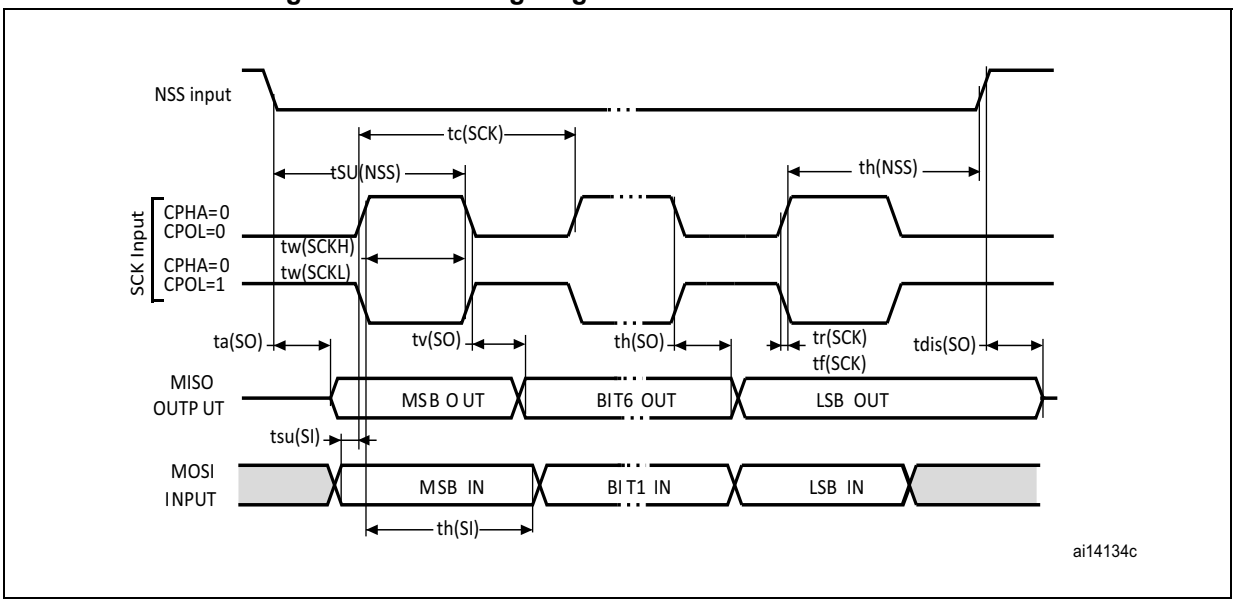
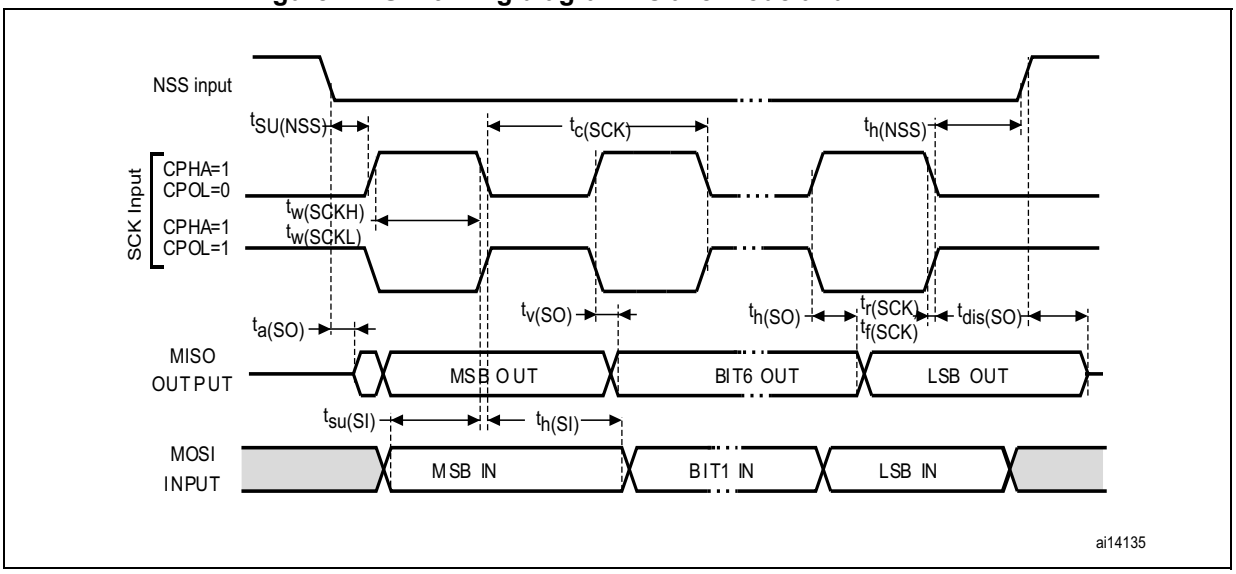
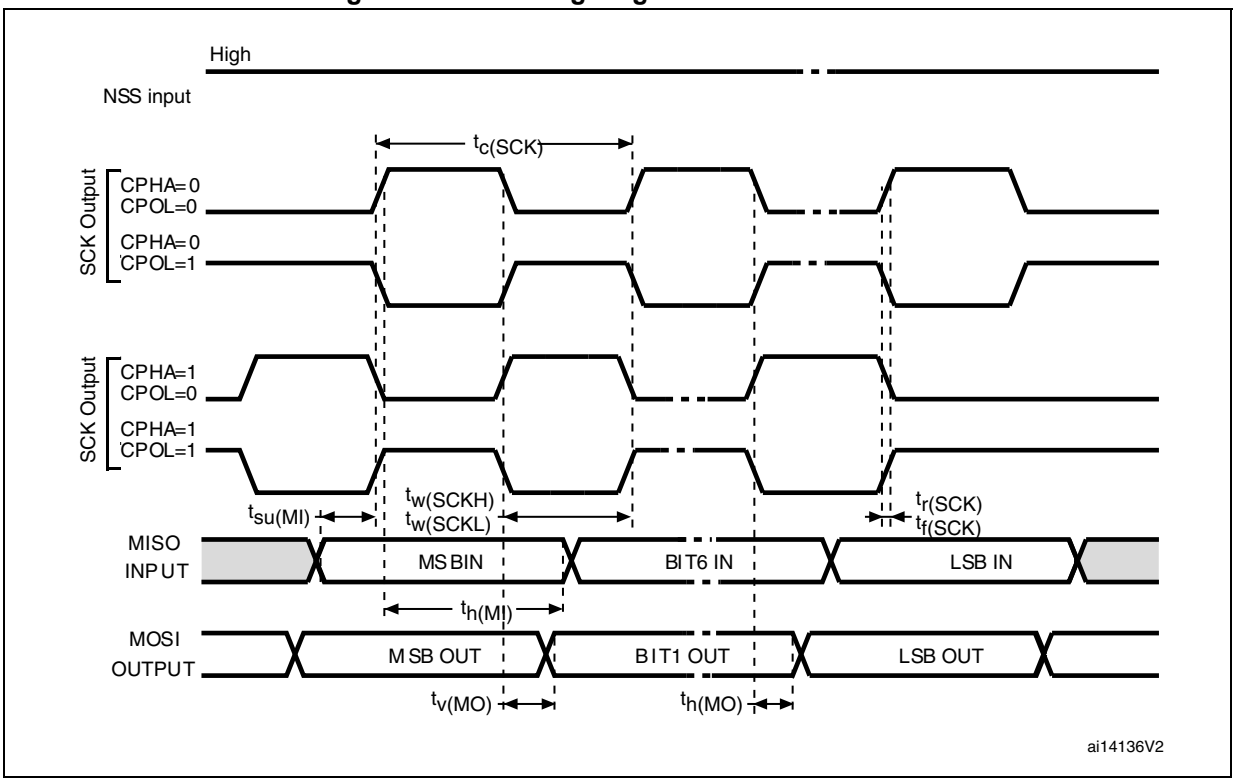


Figure 47. SPI timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 48. SPI timing diagram - master mode(1)



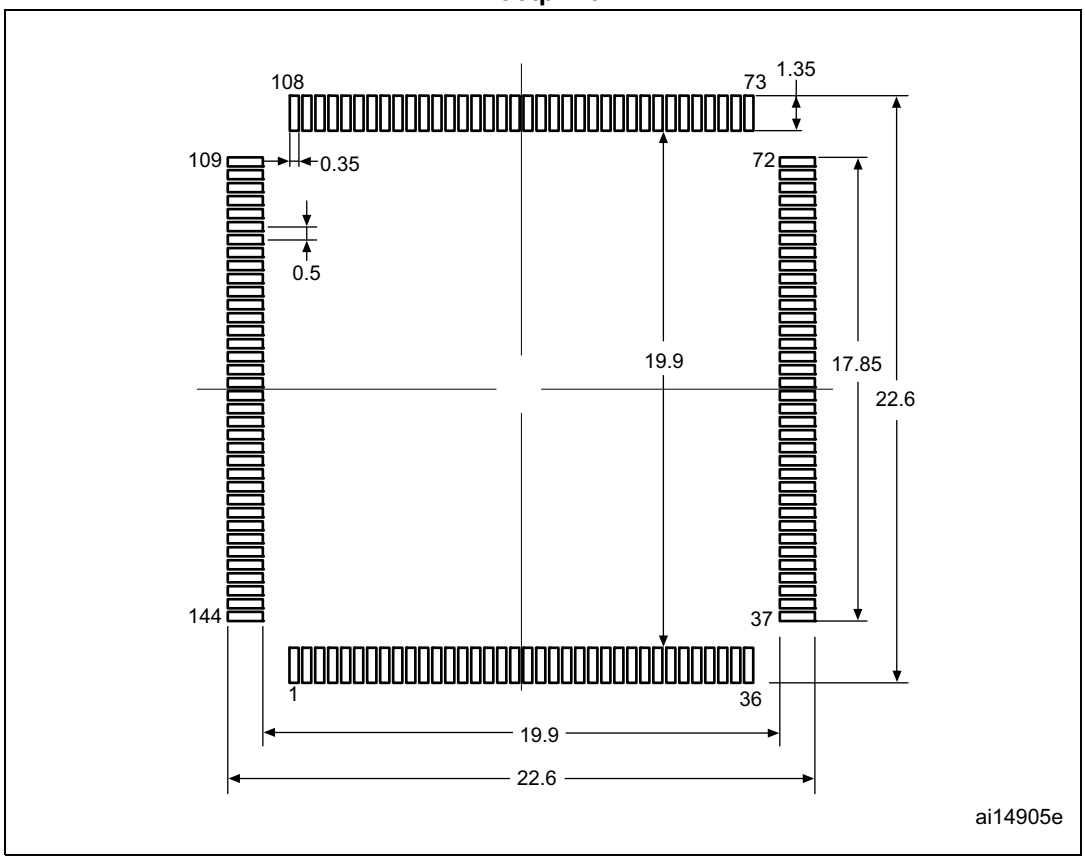
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.18 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 55* are valuesderived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 10*.

Note: It is recommended to perform a calibration after each power-up.

Figure 55. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package footprint



1. Dimensions are expressed in millimeters.

Table 66. Document revision history (continued)

Date	Revision	Changes
21-Jul-2008	3	Document status promoted from Preliminary Data to full datasheet. *FSMC (flexible static memory controller) on page 15* modified. *Power supply supervisor on page 17* modified and V_{DDA} added to *Table 10: General operating conditions on page 40*. Table notes revised in *Section 5: Electrical characteristics*. Capacitance modified in *Figure 9: Power supply scheme on page 37*. *Table 52: SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)* updated. *Table 54: SPI characteristics* modified, $t_{h(NSS)}$ modified in *Figure 46: SPI timing diagram - slave mode and CPHA=0 on page 94*. Minimum SDA and SCL fall time value for Fast mode removed from *Table 51: I^2C characteristics on page 90*, note 1 modified. I_{DD_VBAT} values added to *Table 17: Typical and maximum current consumptions in Stop and Standby modes on page 45*. *Table 30: Flash memory endurance and data retention on page 59* updated. f_{HCLK} corrected in *Table 41: EMS characteristics*. $t_{su(NSS)}$ modified in *Table 54: SPI characteristics*. EO corrected in *Table 58: ADC accuracy on page 98*, f_{PCLK2} corrected in *Table 57: ADC accuracy - limited test conditions* and *Table 58: ADC accuracy*. *Figure 50: Typical connection diagram using the ADC on page 99* and note below corrected. Typical T_{S_temp} value removed from *Table 60: TS characteristics on page 102*. *Section 6.1: LQFP144 package information on page 103* updated, Small text changes.
12-Dec-2008	4	*General-purpose timers (TIMx) on page 19* updated, *Table 3: STM32F101xx family* updated to show the low-density family, *Table 4: Timer feature comparison* added *Figure 1: STM32F101xC, STM32F101xD and STM32F101xE access line block diagram* updated. *Note 9* added, main function after reset and *Note 5* updated in *Table 5: STM32F101xC/STM32F101xD/STM32F101xE pin definitions*. *Note 2* modified below *Table 7: Voltage characteristics on page 38*, $\lvert\Delta V_{DDx}\rvert$ min and $\lvert\Delta V_{DDx}\rvert$ min removed. Measurement conditions specified in *Section 5.3.5: Supply current characteristics on page 42*. *General input/output characteristics on page 82* modified. Max values at T_A = 85 °C updated in *Table 17: Typical and maximum current consumptions in Stop and Standby modes on page 45*. *Section 5.3.10: FSMC characteristics on page 59* revised. Values added to *Table 42: EMI characteristics on page 80*. I_{VREF} added to *Table 55: ADC characteristics on page 96*. *Table 64: Package thermal characteristics on page 113* updated, Small text changes.