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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101rdt6

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2.3.7 Nested vectored interrupt controller (NVIC)

The STM32F101xC, STM32F101xD and STM32F101xE access line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers are used to configure the AHB frequency, the high-speed APB (APB2) domain and the low-speed APB (APB1) domain. The maximum frequency of the AHB and APB domains is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The bootloader is located in system memory. It is used to reprogram the Flash memory by using USART1.

Table 6. FSMC pin definition (continued)

Pins	FSMC					LQFP100(1)
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11	-	-	A16	A16	CLE	Yes
PD12	-	-	A17	A17	ALE	Yes
PD13	-	-	A18	A18		Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2	-	-	A12	-	-	-
PG3	-	-	A13	-	-	-
PG4	-	-	A14	-	-	-
PG5	-	-	A15	-	-	-
PG6	-	-	-	-	INT2	-
PG7	-	-	-	-	INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3	-	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	-	NE1	NE1	NCE2	Yes
PG9	-	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	NCE4_2	-	-	-	-
PG12	-	-	NE4	NE4	-	-
PG13	-	-	A24	A24	-	-
PG14	-	-	A25	A25	-	-
PB7	-	-	NADV	NADV	-	Yes
PE0	-	-	NBL0	NBL0	-	Yes
PE1	-	-	NBL1	NBL1	-	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Sleep mode	External clock(2) all peripherals enabled	36 MHz	24	mA
			24 MHz	17	
			16 MHz	12.5	
			8 MHz	8	
		External clock(2), all peripherals disabled	36 MHz	6	
			24 MHz	5	
			16 MHz	4.5	
			8 MHz	4	

1. Guaranteed by characterization results, tested in production at V_{DD} max, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max	Unit
			V_{DD}/ V_{BAT} = 2.0 V	V_{DD}/ V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	34.5	35	379	µA
		Regulator in Low-power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	24.5	25	365	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	3	3.8	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.8	3.6	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.9	2.1	5(2)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.05	1.1	1.4	2(2)	

1. Typical values are measured at T_A = 25 °C.
2. Guaranteed by characterization results, not tested in production.

Figure 13. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

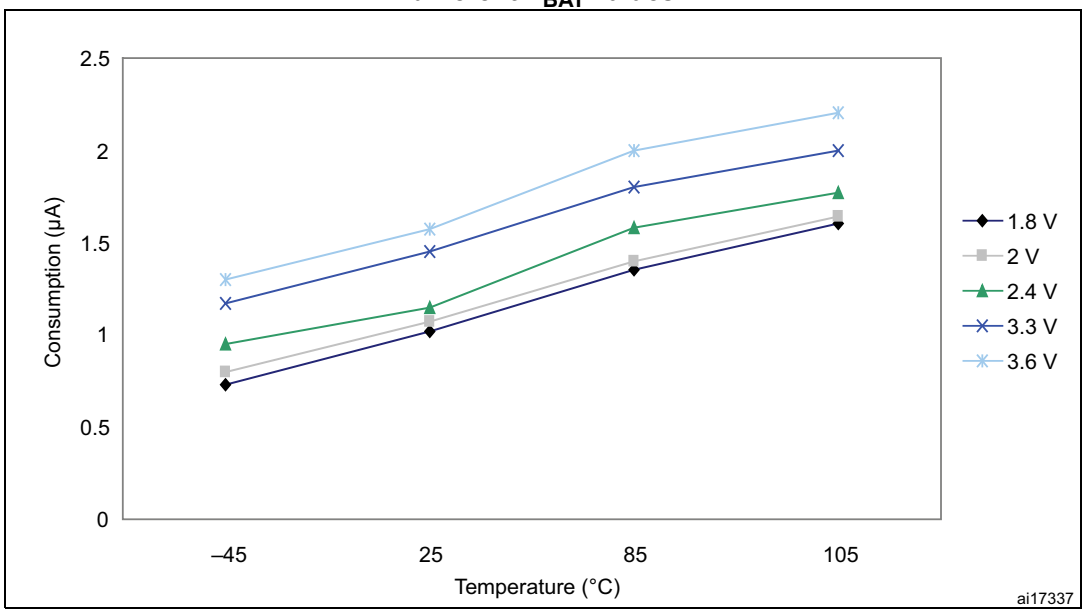


Figure 14. Typical current consumption in Stop mode with regulator in run mode versus temperature at different V_{DD} values

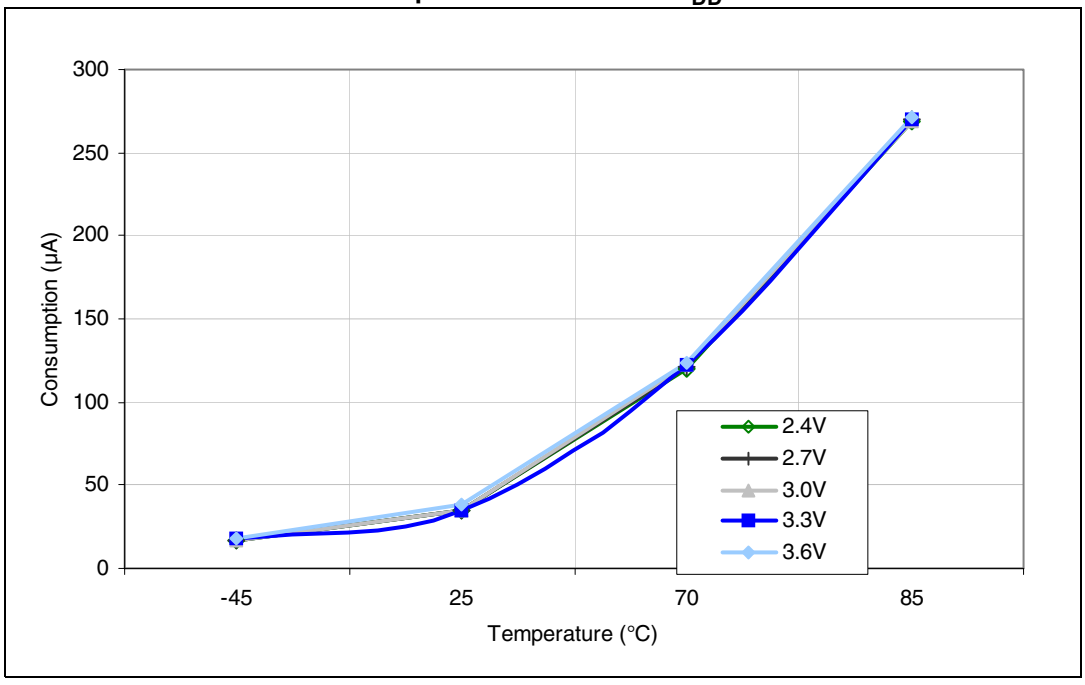


Table 20. Peripheral current consumption(1)

Peripherals		µA/MHz
AHB (up to36 MHz)	DMA1	20.42
	DMA2	19.03
	FSMC	52.36
	CRC	2.36
	BusMatrix(2)	9.72
APB1 (up to 18 MHz)	APB1-Bridge	7.78
	TIM2	33.06
	TIM3	31.94
	TIM4	31.67
	TIM5	31.94
	TIM6	8.06
	TIM7	8.06
	SPI2/I2S2(3)	8.33
	SPI3/I2S3(3)	8.33
	USART2	12.22
	USART3	12.22
	UART4	12.22
	UART5	12.22
	I2C1	10.28
	I2C2	10.00
	USB	18.06
	DAC(4)	8.06
	WWDG	3.89
	PWR	1.11
	BKP	1.11
	IWDG	5.28

Table 20. Peripheral current consumption(1) (continued)

Peripherals		µA/MHz
APB2 (up to 36 MHz)	APB2-Bridge	4.17
	GPIOA	8.47
	GPIOB	8.47
	GPIOC	6.53
	GPIOD	8.47
	GPIOE	6.53
	GPIOF	6.53
	GPIOG	6.11
	SPI1	4.72
	USART1	12.50
	TIM1	22.92
	TIM8	22.92
	ADC1(5)(6)	17.32

1. f_{HCLK} = 36 MHz, $f_{APB1} = f_{HCLK/2}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master peripheral is ON.
3. When the I2S is enabled, a current consumption of 0.02 mA must be added.
4. When DAC_OUT1 or DAC_OUT2 is enabled, a current consumption of 0.36 mA must be added.
5. Specific conditions for ADC: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK/2}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$. When ADON bit in the ADC_CR2 register is set to 1, the current consumption is equal to 0.54 mA.
6. When the ADC is enabled, a current consumption of 0.08 mA must be added.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Table 21. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	

5.3.8 PLL characteristics

The parameters given in *Table 28* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 28. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	36	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Guaranteed by characterization results, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 85 °C unless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +85 °C	40	52.5	70	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +85 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +85 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 36 MHz with 1 wait state, V_{DD} = 3.3 V	-	-	28	mA
		Write mode f_{HCLK} = 36 MHz, V_{DD} = 3.3 V	-	-	7	mA
		Erase mode f_{HCLK} = 36 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage		2	-	3.6	V

1. Guaranteed by design, not tested in production.

Table 33. Asynchronous multiplexed NOR/PSRAM read timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	t_{HCLK}	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2t_{HCLK}$ + 24	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 24. Asynchronous multiplexed NOR/PSRAM write waveforms

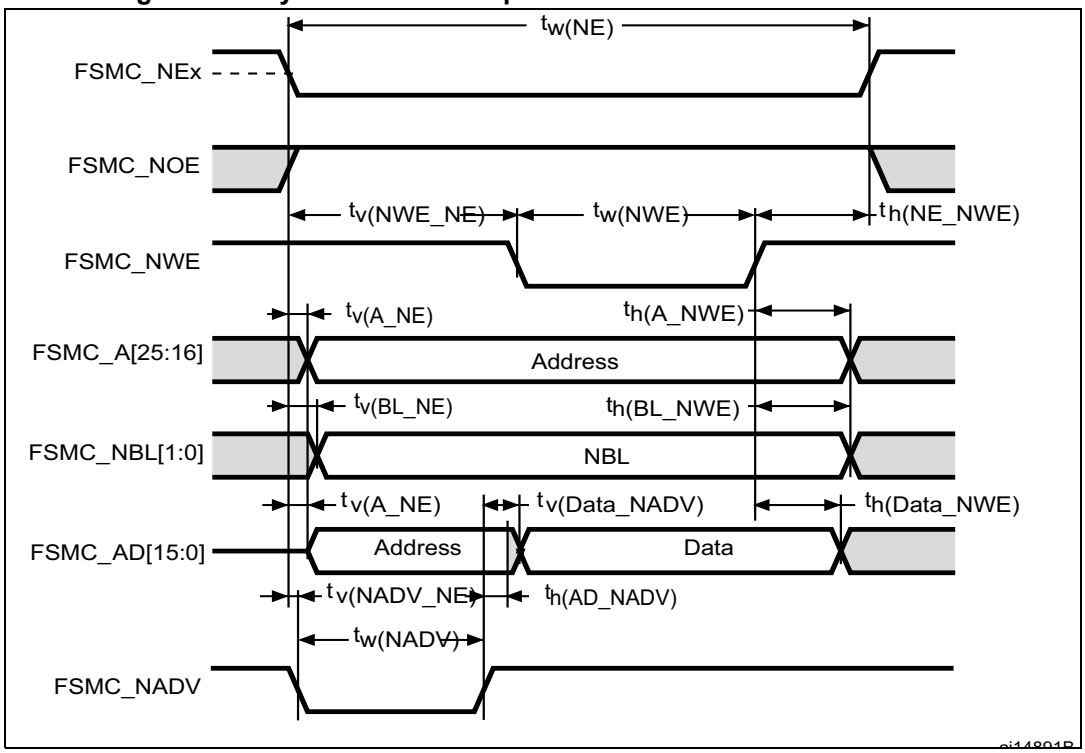


Table 34. Asynchronous multiplexed NOR/PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK} - 1$	$5t_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$1t_{HCLK}$	$1t_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$3t_{HCLK} - 1$	2	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$t_{HCLK} - 1$	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	$t_{HCLK} - 1$	$t_{HCLK} + 1$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$t_{HCLK} - 3$	-	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$1t_{HCLK}$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.6	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$t_{HCLK} - 1.5$	-	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	$t_{HCLK} + 1.5$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$t_{HCLK} - 5$	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production..

Figure 26. Synchronous multiplexed PSRAM write timings

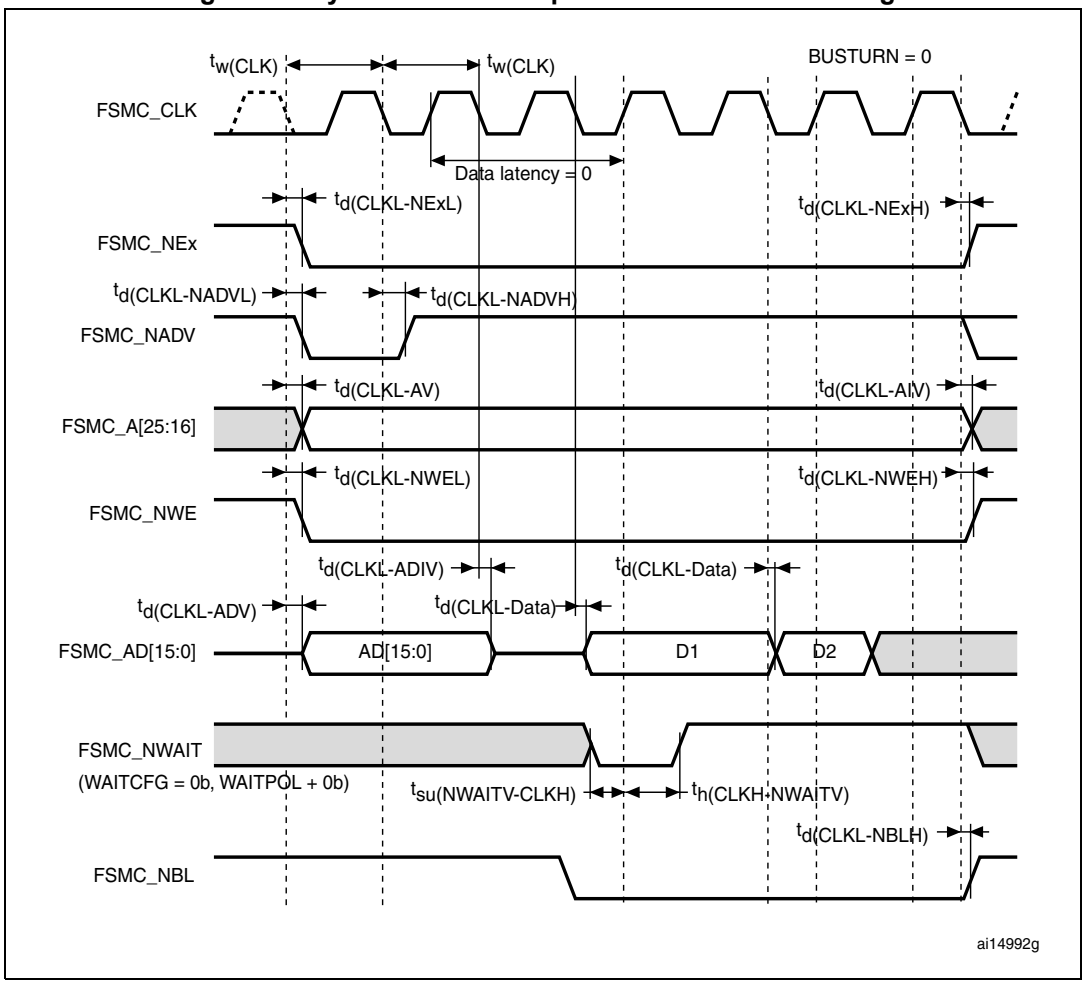


Figure 27. Synchronous non-multiplexed NOR/PSRAM read timings

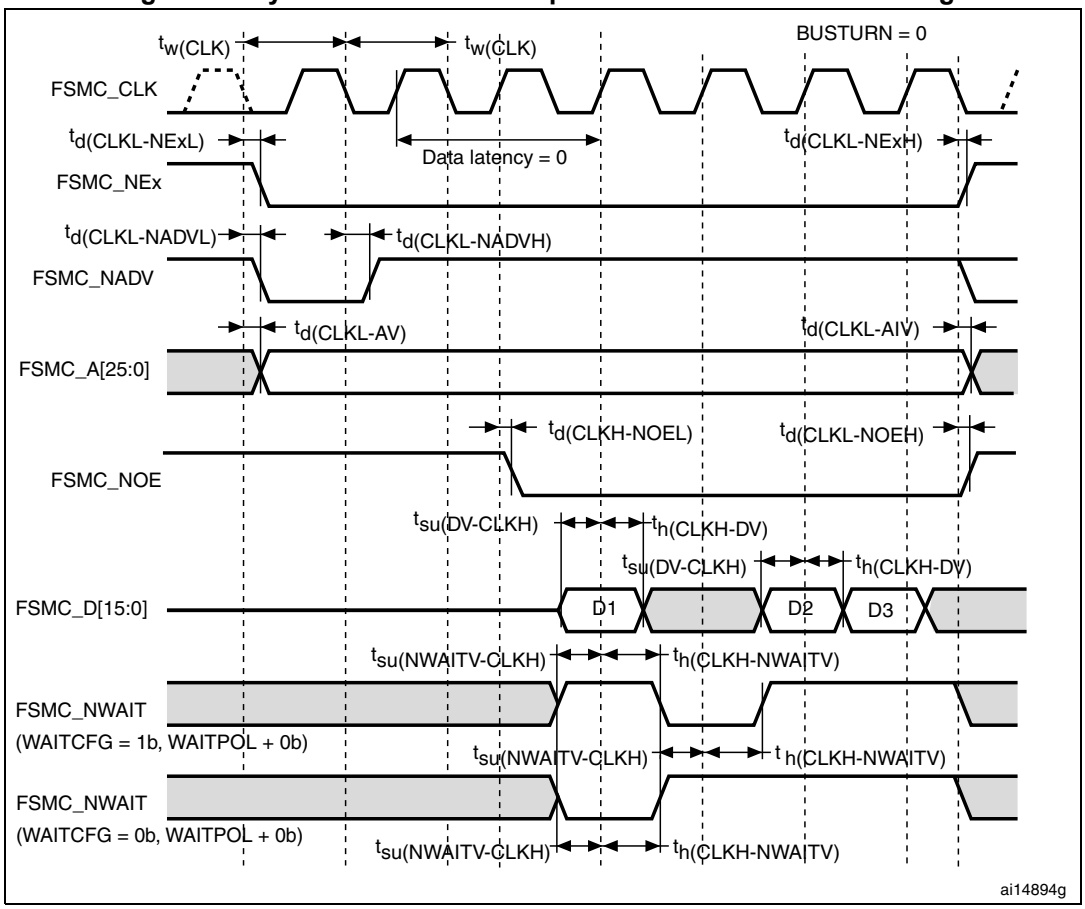


Table 37. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	55.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 0...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 0...25)	4	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1.5	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	6.5	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	7	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_SMCLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.

2. Guaranteed by characterization results, not tested in production.

Figure 28. Synchronous non-multiplexed PSRAM write timings

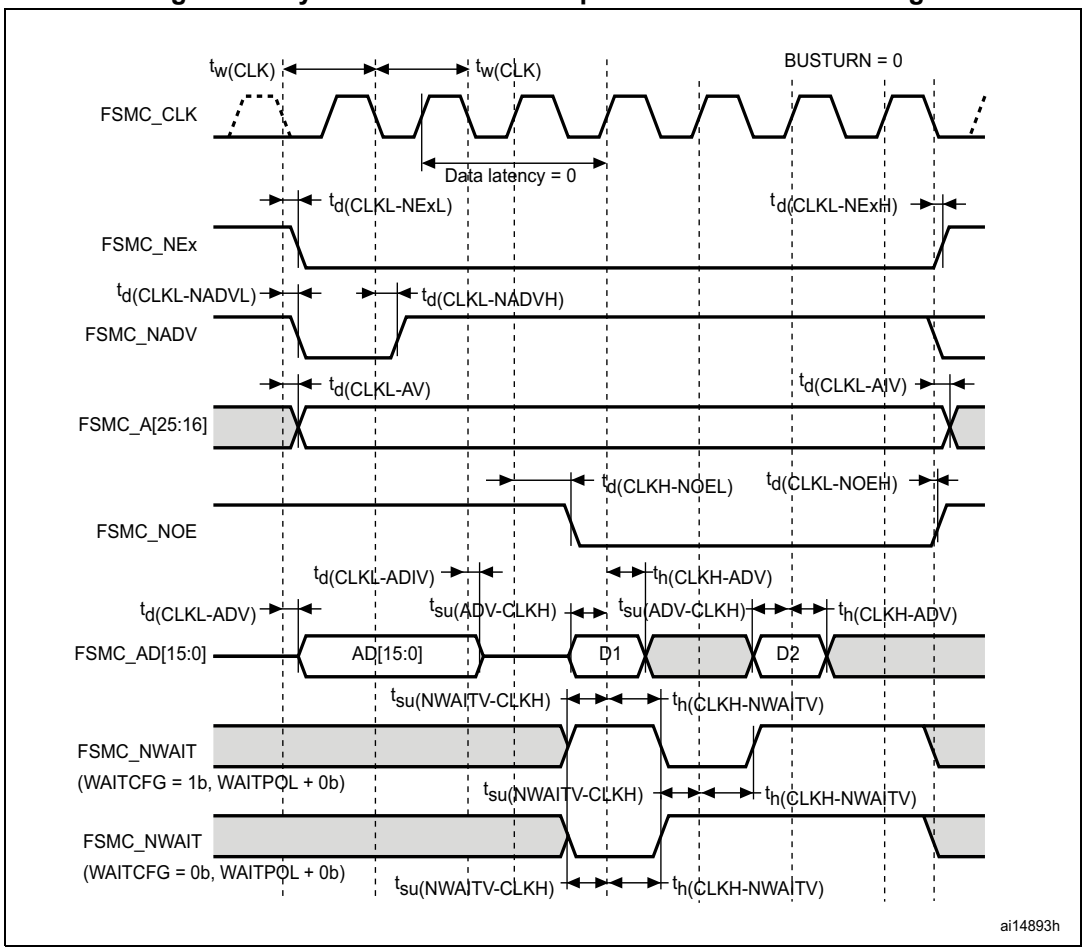


Table 38. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	55.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns

Figure 38. NAND controller waveforms for common memory write access

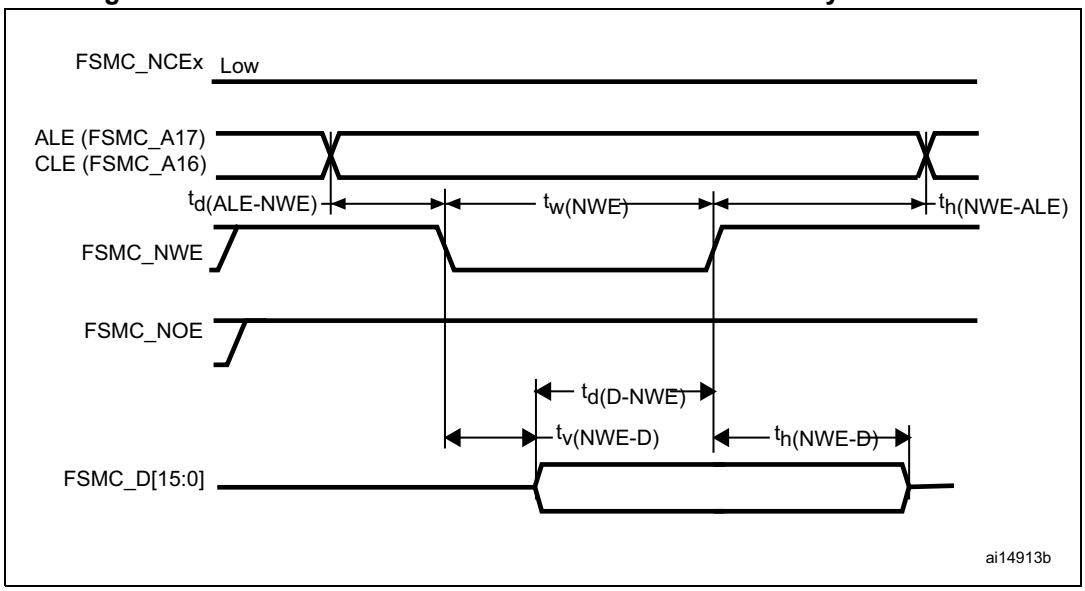


Table 40. Switching characteristics for NAND Flash read and write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$(2)	FSMC_D[15:0] valid before FSMC_NWE high	$5t_{HCLK}$ + 12	-	ns
$t_{w(NOE)}$(2)	FSMC_NOE low width	$4t_{HCLK}$ – 1.5	$4t_{HCLK}$ + 1.5	ns
$t_{su(D-NOE)}$(2)	FSMC_D[15:0] valid data before FSMC_NOE high	25	-	ns
$t_{h(NOE-D)}$(2)	FSMC_D[15:0] valid data after FSMC_NOE high	7	-	ns
$t_{w(NWE)}$(2)	FSMC_NWE low width	$4t_{HCLK}$ – 1	$4t_{HCLK}$ + 2.5	ns
$t_{v(NWE-D)}$(2)	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$(2)	FSMC_NWE high to FSMC_D[15:0] invalid	$2t_{HCLK}$ + 4ns	-	ns
$t_{d(ALE-NWE)}$(3)	FSMC_ALE valid before FSMC_NWE low	-	$3t_{HCLK}$ + 1.5	ns
$t_{h(NWE-ALE)}$(3)	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK}$ + 4.5	-	ns
$t_{d(ALE-NOE)}$(3)	FSMC_ALE valid before FSMC_NOE low	-	$3t_{HCLK}$ + 2	ns
$t_{h(NOE-ALE)}$(3)	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK}$ + 4.5	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Figure 41. 5 V tolerant I/O input characteristics - CMOS port

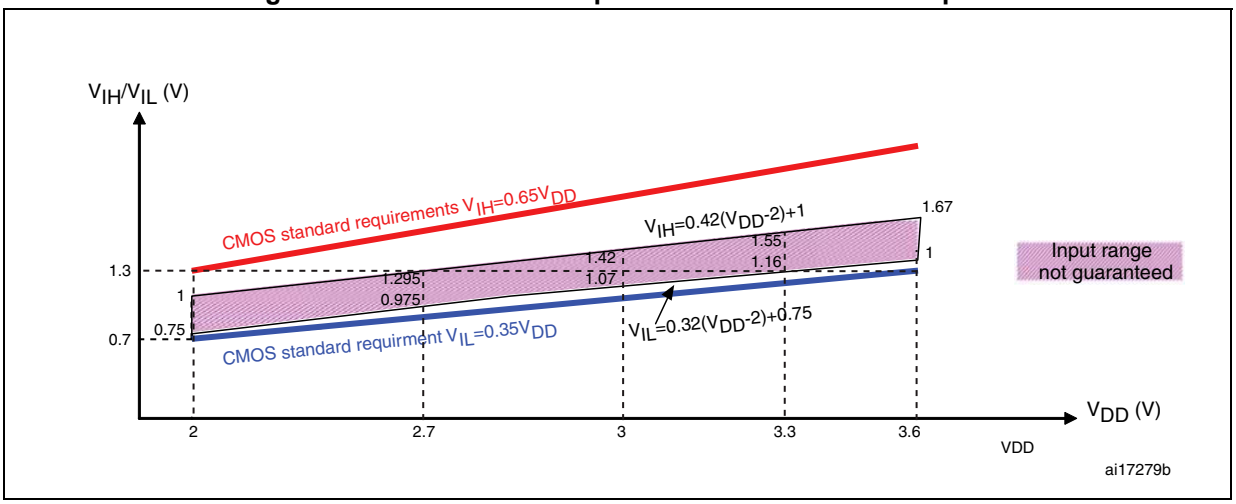
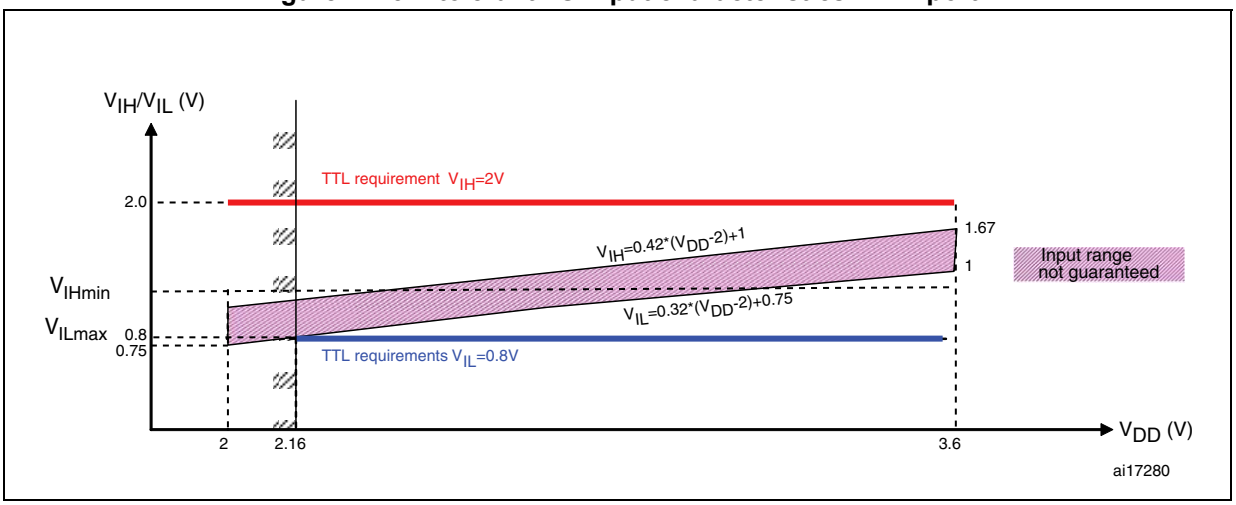


Figure 42. 5 V tolerant I/O input characteristics - TTL port



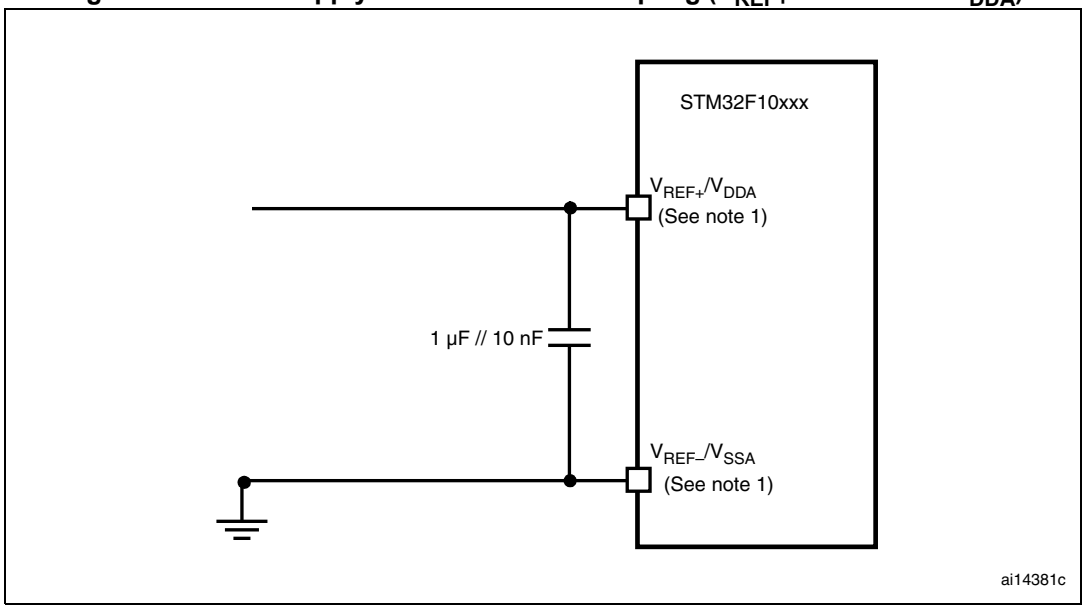
Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxedV_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3 mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 8*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 8*).

Figure 52. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.19 DAC electrical specifications

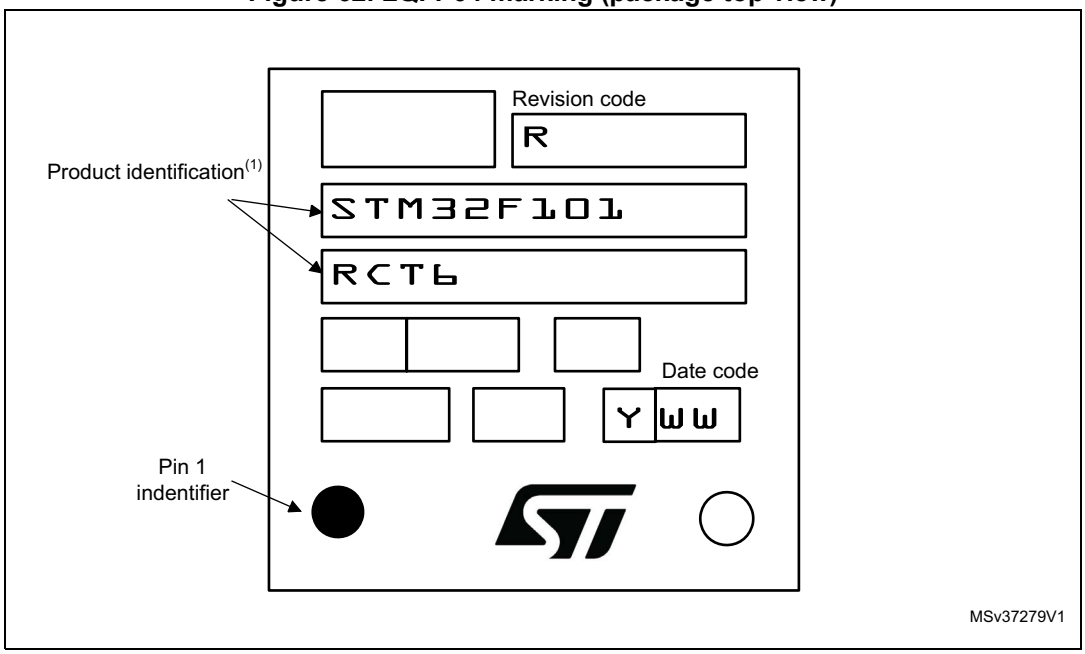
Table 59. DAC characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	
V_{REF+}	Reference supply voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) and (0xEAB) at V_{REF+} = 2.4 V.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-		V_{REF+} – 1LSB	V	

Device marking for LQFP64

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 62. LQFP64 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7 Part numbering

Table 65. Ordering information scheme

Example: STM32 F 101 R C T 6 xxx

Device family

STM32 = ARM® -based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

101 = access line

Pin count

R = 64 pins
V = 100 pins
Z = 144 pins

Flash memory size

C = 256 Kbytes of Flash memory
D = 384 Kbytes of Flash memory
E = 512 Kbytes of Flash memory

Package

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

Options

xxx = programmed parts
TR = tape and real

For a list of available options (speed, package, etc..) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 66. Document revision history (continued)

Date	Revision	Changes
30-Mar-2009	5	I/O information clarified on cover page, Number of ADC peripherals corrected in *Table 2: STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts*. In *Table 5: STM32F101xC/STM32F101xD/STM32F101xE pin definitions*: – I/O level of pins PF11, PF12, PF13, PF14, PF15, G0, G1 and G15 updated – PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column. PG14 pin description modified in *Table 6: FSMC pin definition*, *Figure 6: Memory map on page 35* modified. Note modified in *Table 14: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 16: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 14*, *Figure 15* and *Figure 16* show typical curves (titles changed). *Table 21: High-speed external user clock characteristics* and *Table 22: Low-speed user external clock characteristics* modified. ACC_{HSI} max values modified in *Table 25: HSI oscillator characteristics* FSMC configuration modified for *Asynchronous waveforms and timings*. Notes modified below *Figure 21: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms* and *Figure 22: Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms*. $t_{w(NADV)}$ values modified in *Table 31: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings* and *Table 34: Asynchronous multiplexed NOR/PSRAM write timings*. $t_{h(Data\_NWE)}$ modified in *Table 32: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings*. In *Table 36: Synchronous multiplexed PSRAM write timings* and *Table 38: Synchronous non-multiplexed PSRAM write timings*: – $t_{v(Data-CLK)}$ renamed as $t_{d(CLKL-Data)}$ – $t_{d(CLKL-Data)}$ min value removed and max value added – $t_{h(CLKL-DV)}$ / $t_{h(CLKL-ADV)}$ removed *Figure 25: Synchronous multiplexed NOR/PSRAM read timings*. *Figure 26: Synchronous multiplexed PSRAM write timings* and *Figure 28: Synchronous non-multiplexed PSRAM write timings* modified, Small text changes.