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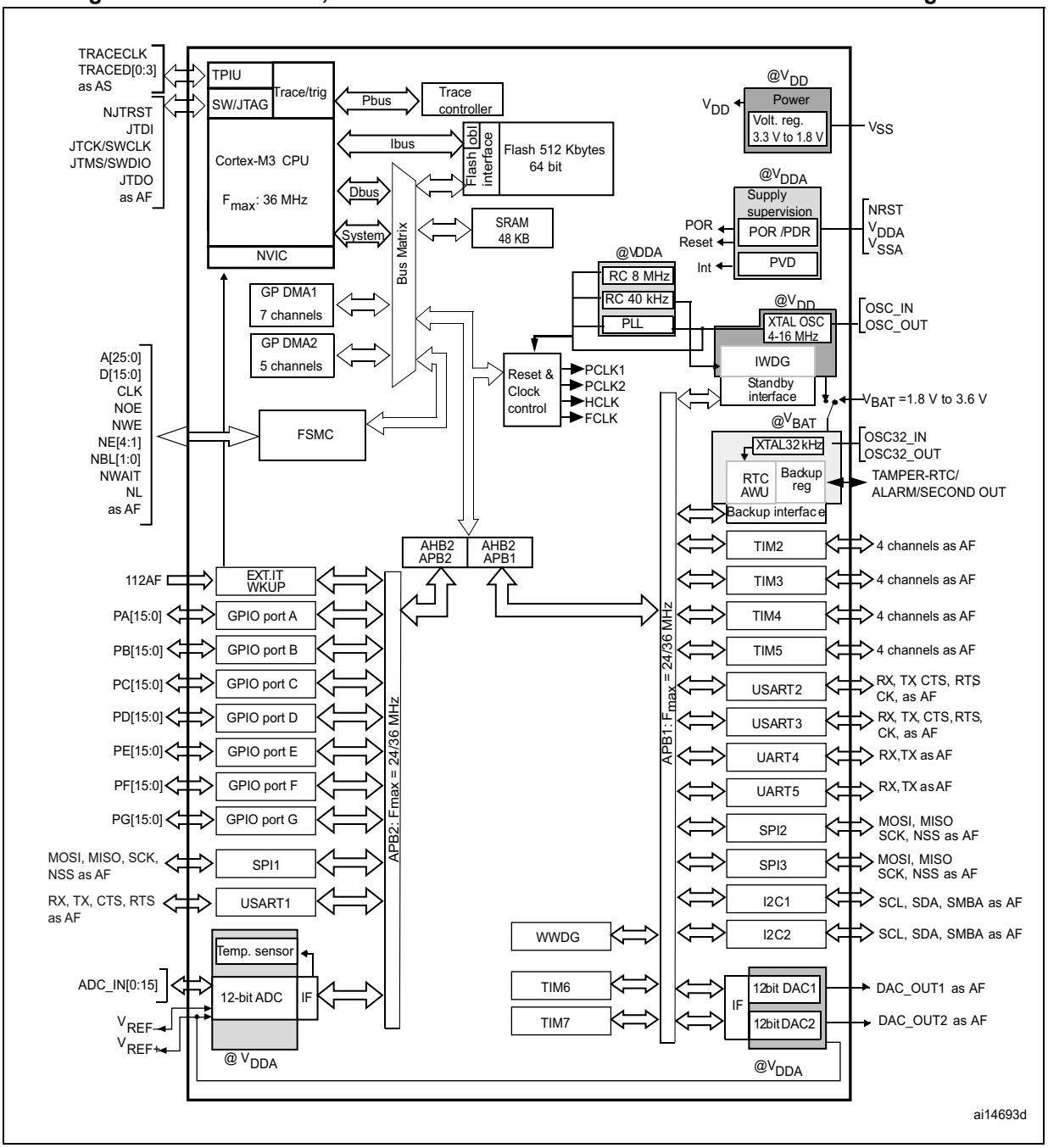
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

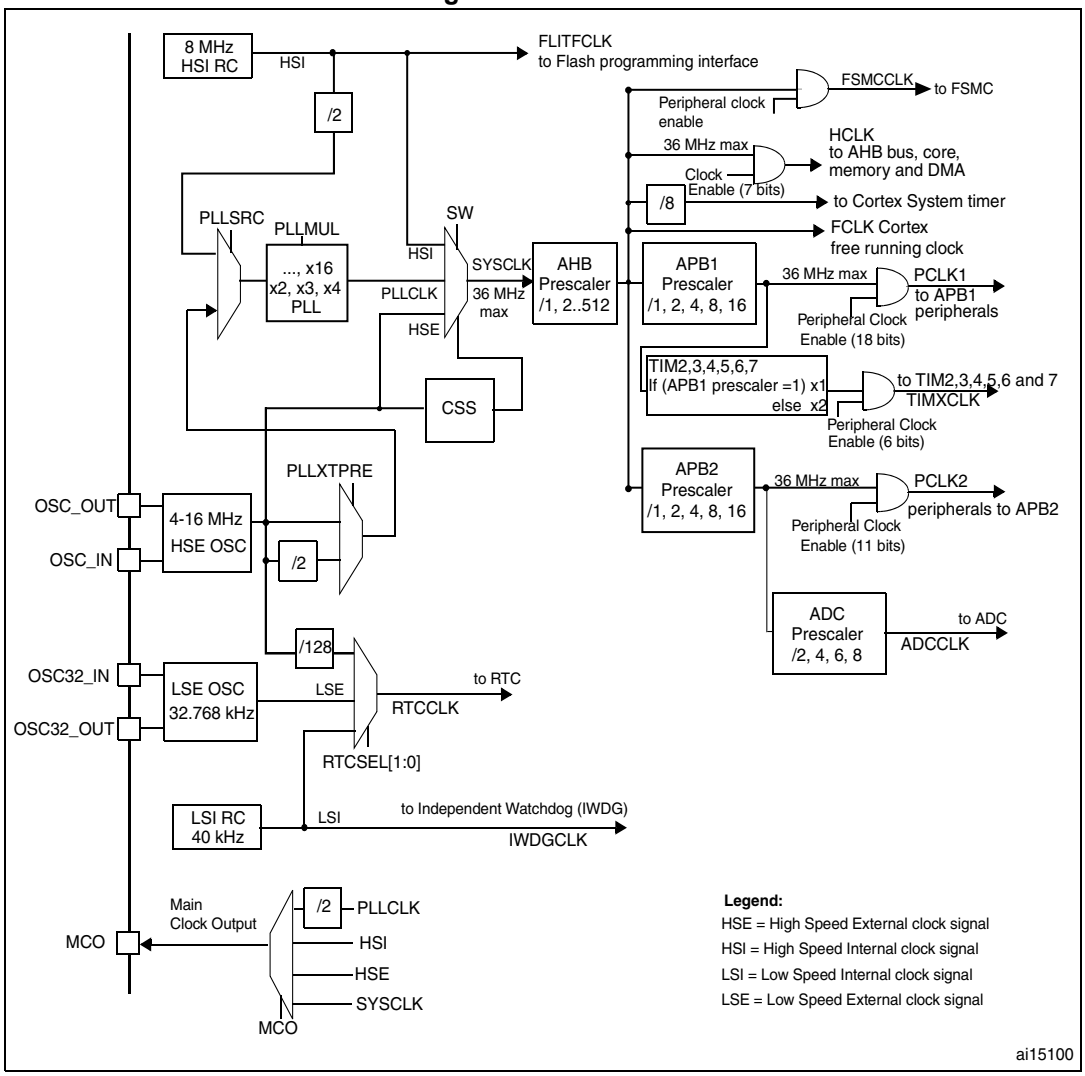
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101rdt6tr

Figure 1. STM32F101xC, STM32F101xD and STM32F101xE access line block diagram



1. T_A = –40 °C to +85 °C (junction temperature up to 105 °C).
2. AF = alternate function on I/O port pin.

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 36 MHz.
2. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz or 28 MHz.

2.2 Full compatibility throughout the family

The STM32F101xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F101x4 and STM32F101x6 are identified as low-density devices, the STM32F101x8 and STM32F101xB are referred to as medium-density devices, and the STM32F101xC, STM32F101xD and STM32F101xE are referred to as high-density devices .

Low- and high-density devices are an extension of the STM32F101x8/B medium-density devices, they are specified in the STM32F101x4/6 and STM32F101xC/D/E datasheets, respectively.

Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM densities, and additional peripherals like FSMC and DAC, while remaining fully compatible with the other members of the family.

The STM32F101x4, STM32F101x6, STM32F101xC, STM32F101xD and STM32F101xE are a drop-in replacement for the STM32F101x8/B devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F101xx access line family is fully compatible with all existing STM32F103xx performance line and STM32F102xx USB access line devices.

Table 3. STM32F101xx family

<table>
<tr><th rowspan="4">Pinout</th><th colspan="7">Memory size</th></tr>
<tr><th colspan="2">Low-density devices</th><th colspan="2">Medium-density devices</th><th colspan="3">High-density devices</th></tr>
<tr><th>16 KB Flash</th><th>32 KB Flash(1)</th><th>64 KB Flash</th><th>128 KB Flash</th><th>256 KB Flash</th><th>384 KB Flash</th><th>512 KB Flash</th></tr>
<tr><th>4 KB RAM</th><th>6 KB RAM</th><th>10 KB RAM</th><th>16 KB RAM</th><th>32 KB RAM</th><th>48 KB RAM</th><th>48 KB RAM</th></tr>
<tr><td>144</td><td colspan="4" rowspan="2"></td><td colspan="3" rowspan="2">5 × USARTs
4 × 16-bit timers. 2 × basic timers
3 × SPIs, 2 × I2Cs, 1 × ADC. 2 × DACs
FSMC (100 and 144 pins)</td></tr>
<tr><td>100</td><td colspan="2" rowspan="2">3 × USARTs
3 × 16-bit timers
2 × SPIs, 2 × I2Cs,
1 × ADC</td></tr>
<tr><td>64</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I2C
1 × ADC</td><td colspan="3" rowspan="2"></td></tr>
<tr><td>48</td></tr>
<tr><td>36</td><td colspan="5"></td></tr>
</table>

1. For orderable part numbers that do not show the A internal code after the temperature range code (6), the reference datasheet for electrical characteristics is that of the STM32F101x8/B medium-density devices.

2.3 Overview

2.3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while

2.3.11 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 9: Power supply scheme*.

2.3.12 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

2.3.13 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.3.14 Low-power modes

The STM32F101xC, STM32F101xD and STM32F101xE access line supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

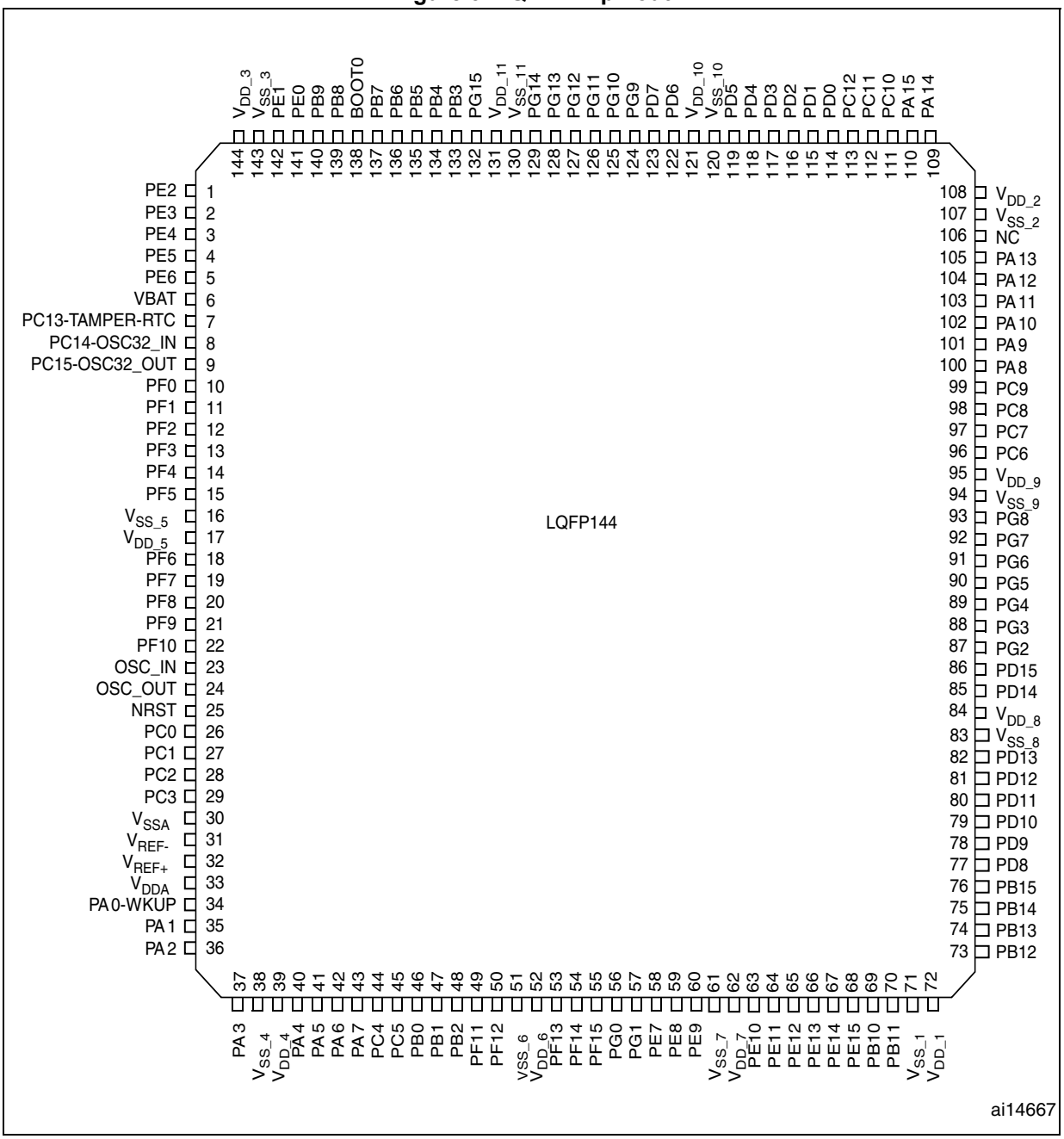
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

3 Pinouts and pin descriptions

Figure 3. LQFP144 pinout



1. The above figure shows the package top view.

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
62	-	-	V_{DD_7}	S	-	V_{DD_7}	-	-
63	-	41	PE10	I/O	FT	PE10	FSMC_D7	-
64	-	42	PE11	I/O	FT	PE11	FSMC_D8	-
65	-	43	PE12	I/O	FT	PE12	FSMC_D9	-
66	-	44	PE13	I/O	FT	PE13	FSMC_D10	-
67	-	45	PE14	I/O	FT	PE14	FSMC_D11	-
68	-	46	PE15	I/O	FT	PE15	FSMC_D12	-
69	29	47	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(8)	TIM2_CH3
70	30	48	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(8)	TIM2_CH4
71	31	49	V_{SS_1}	S	-	V_{SS_1}	-	-
72	32	50	V_{DD_1}	S	-	V_{DD_1}	-	-
73	33	51	PB12	I/O	FT	PB12	SPI2_NSS(8)/ I2C2_SMBA USART3_CK(8)	-
74	34	52	PB13	I/O	FT	PB13	SPI2_SCK(8)/ USART3_CTS(8)	-
75	35	53	PB14	I/O	FT	PB14	SPI2_MISO(8)/ USART3_RTS(8)	-
76	36	54	PB15	I/O	FT	PB15	SPI2_MOSI(8)	-
77	-	55	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
78	-	56	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
79	-	57	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
80	-	58	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
81	-	59	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
82	-	60	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
83	-	-	V_{SS_8}	S	-	V_{SS_8}	-	-
84	-	-	V_{DD_8}	S	-	V_{DD_8}	-	-
85	-	61	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
86	-	62	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
87	-	-	PG2	I/O	FT	PG2	FSMC_A12	-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions

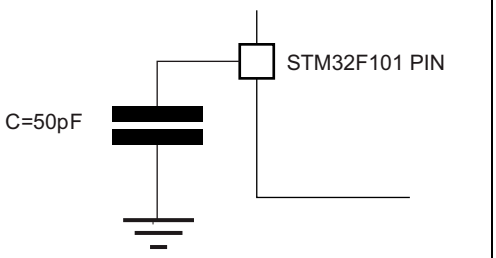
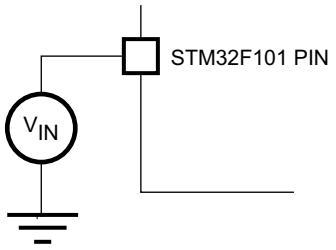
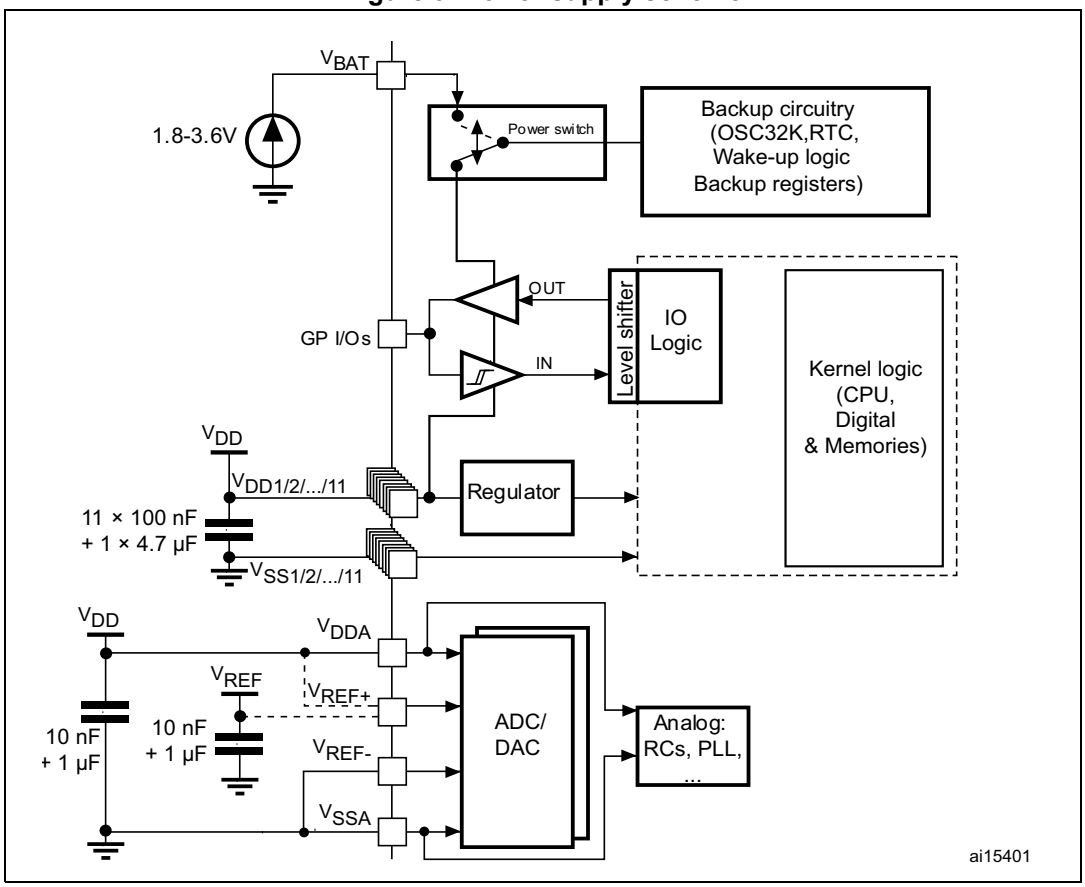


Figure 8. Pin input voltage



5.1.6 Power supply scheme

Figure 9. Power supply scheme



Caution: In *Figure 9*, the 4.7 µF capacitor must be connected to V_{DD3}.

Figure 11. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

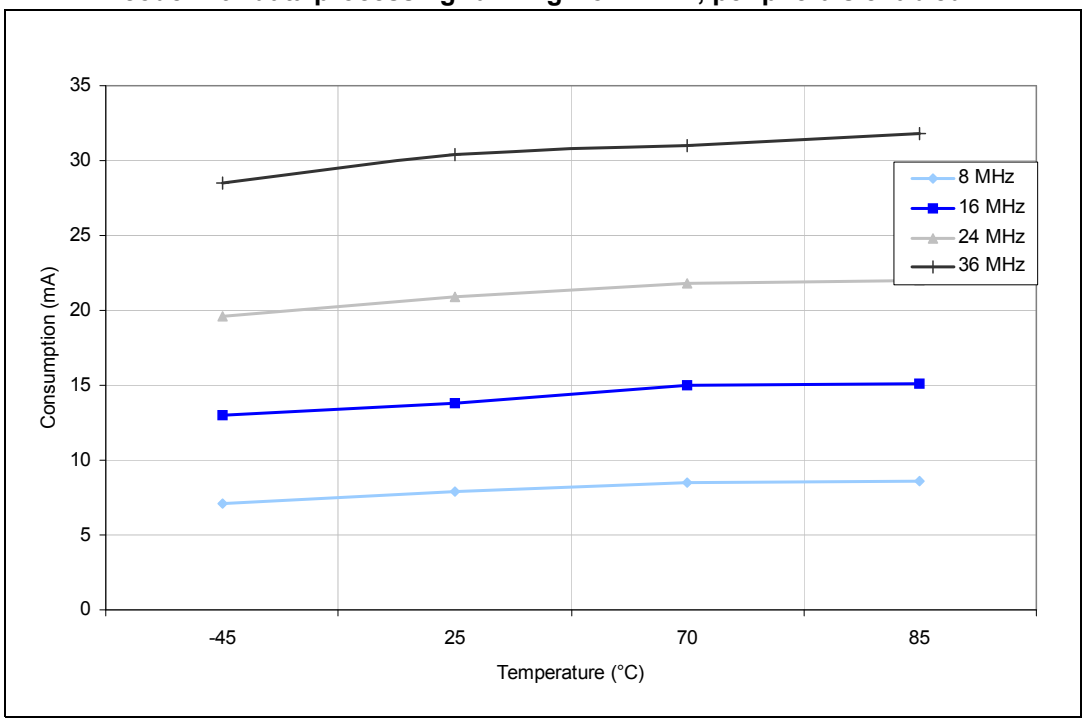


Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

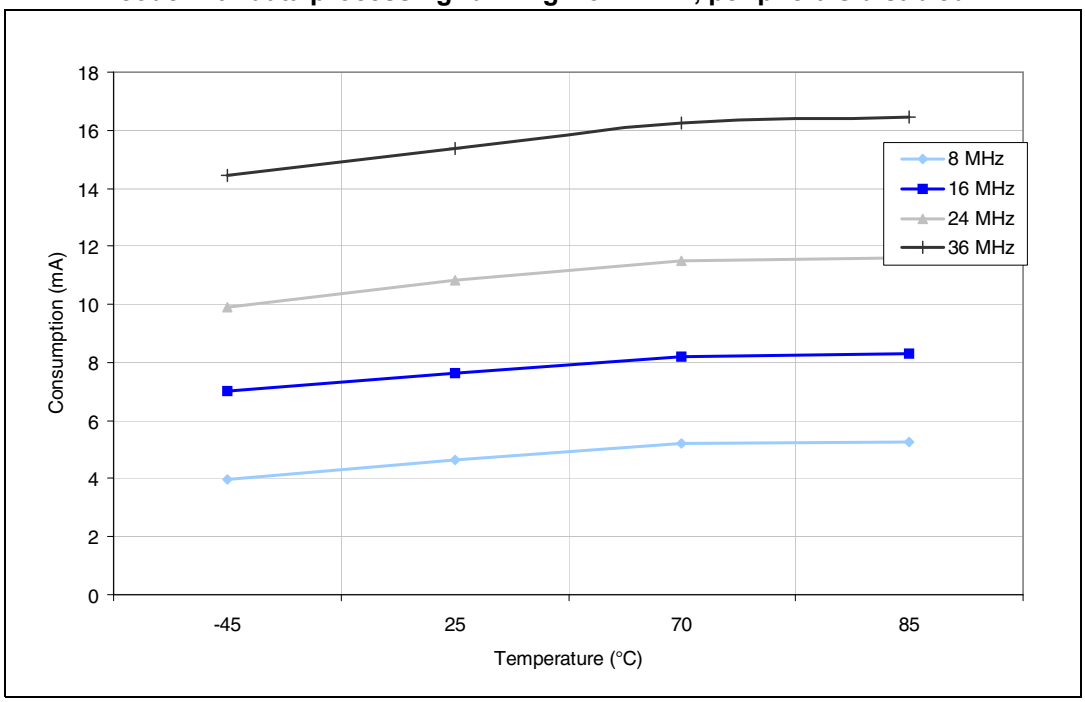
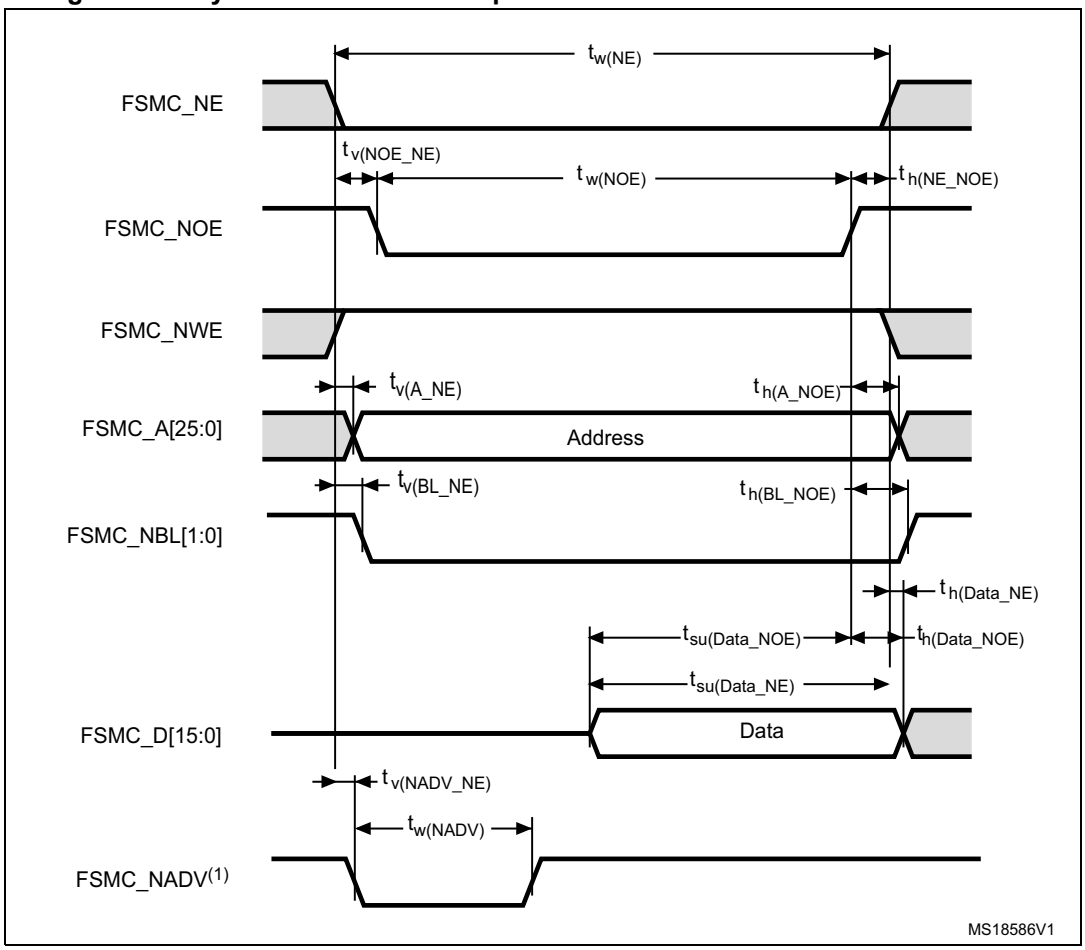


Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Note: FSMC_BusTurnAroundDuration = 0.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1) (2)

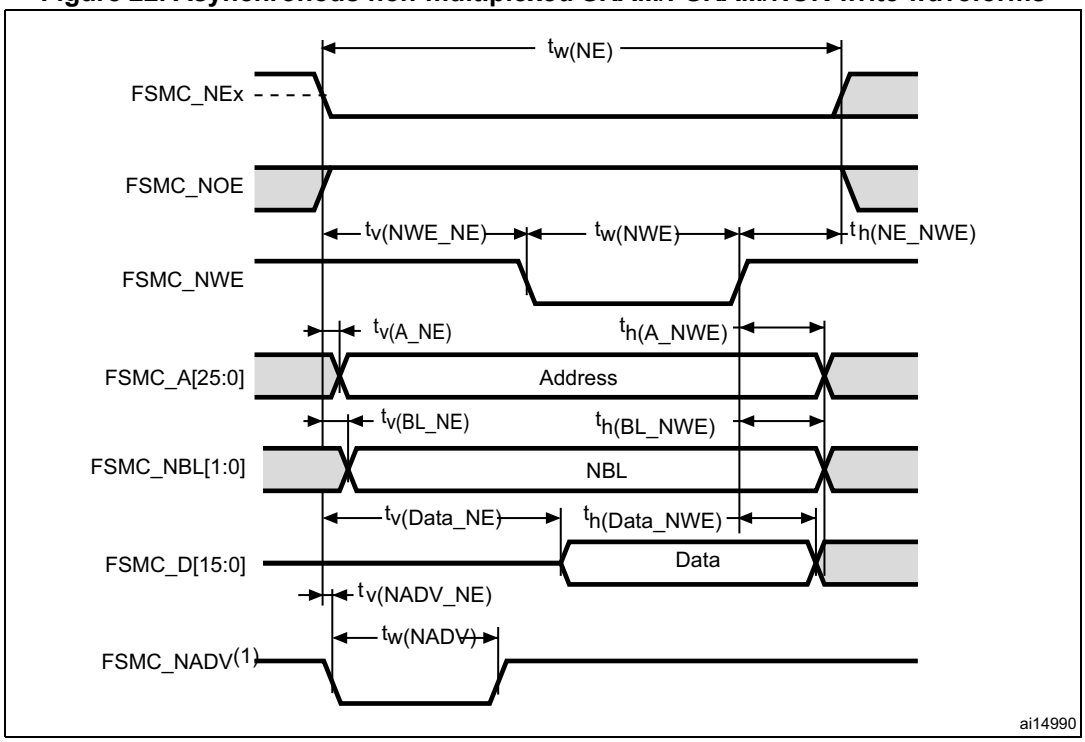
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK} - 1.5$	$5t_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$5t_{HCLK} - 1.5$	$5t_{HCLK} + 1.5$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0.1	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2t_{HCLK} + 25$	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$2t_{HCLK} + 25$	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	t_{HCLK} + 1.5	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 32. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

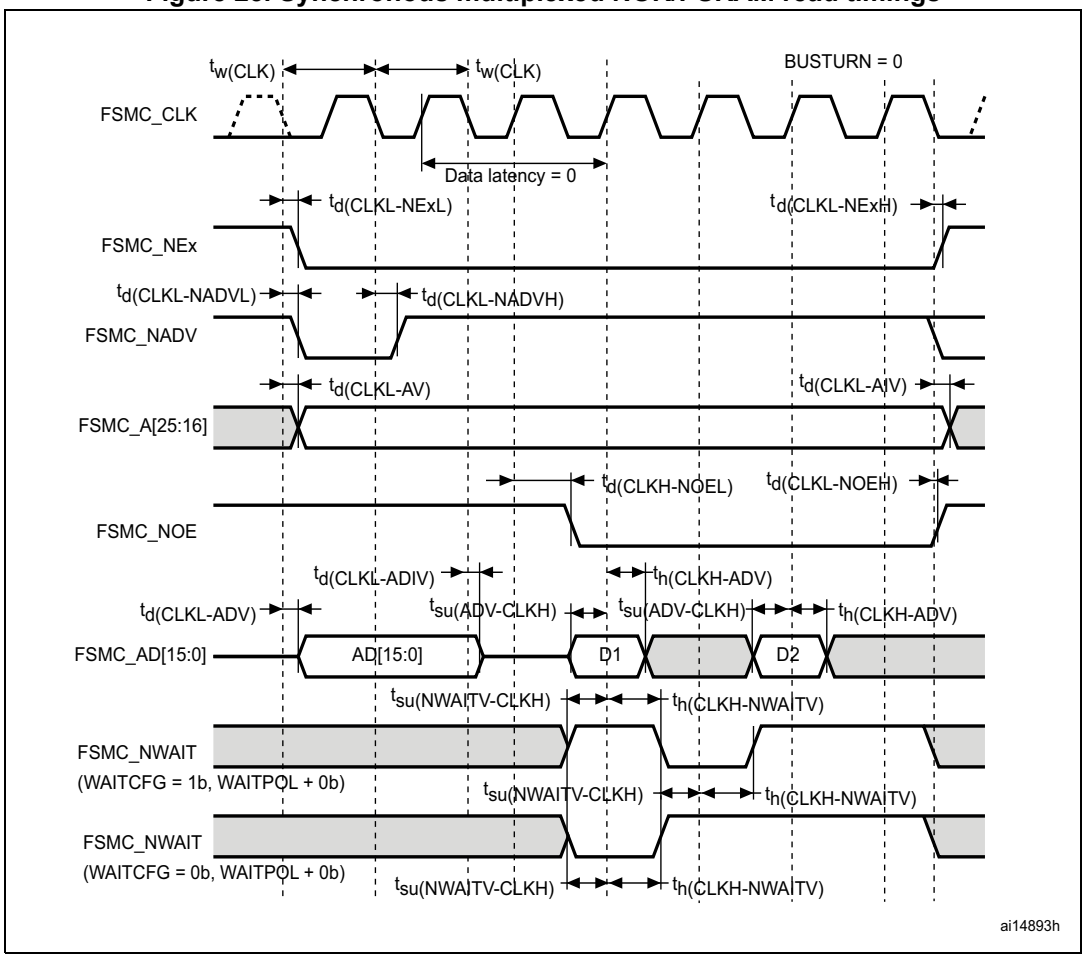
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3t_{HCLK} - 1$	$3t_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$t_{HCLK} - 0.5$	$t_{HCLK} + 1.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$t_{HCLK} - 0.5$	$t_{HCLK} + 1.5$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	t_{HCLK}	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7.5	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	t_{HCLK}	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$t_{HCLK} - 0.5$	-	ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid	-	$t_{HCLK} + 7$	ns

Synchronous waveforms and timings

Figure 25 through *Figure 28* represent synchronous waveforms and *Table 36* through *Table 38* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F10xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 25. Synchronous multiplexed NOR/PSRAM read timings



5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 45*

Table 45. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 43* and *Table 48*, respectively.

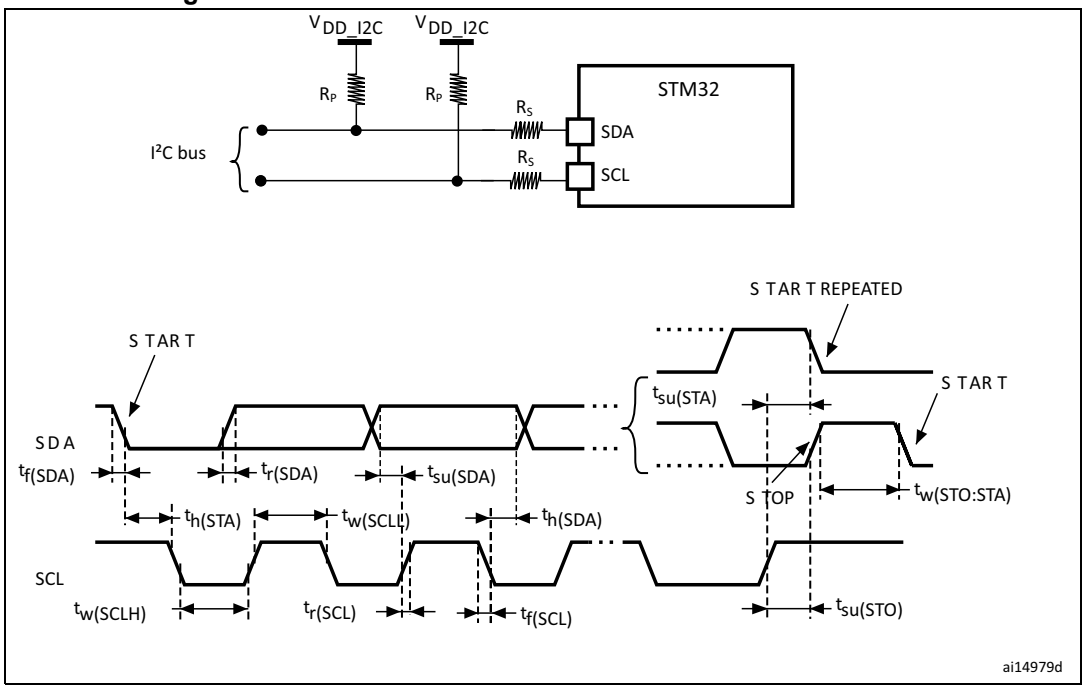
Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 48. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$F_{max(IO)out}$	Maximum Frequency(2)	C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 43*.
3. Guaranteed by design, not tested in production.

Figure 45. I²C bus AC waveforms and measurement circuit(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.

Table 52. SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 56. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 57. ADC accuracy - limited test conditions(1)(2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V, T_A = 25 °C Measurements made after ADC calibration V_{REF+} = V_{DDA}	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.
3. Guaranteed by characterization results, not tested in production.

Table 58. ADC accuracy(1) (2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.
4. Guaranteed by characterization results, not tested in production.

Figure 49. ADC accuracy characteristics

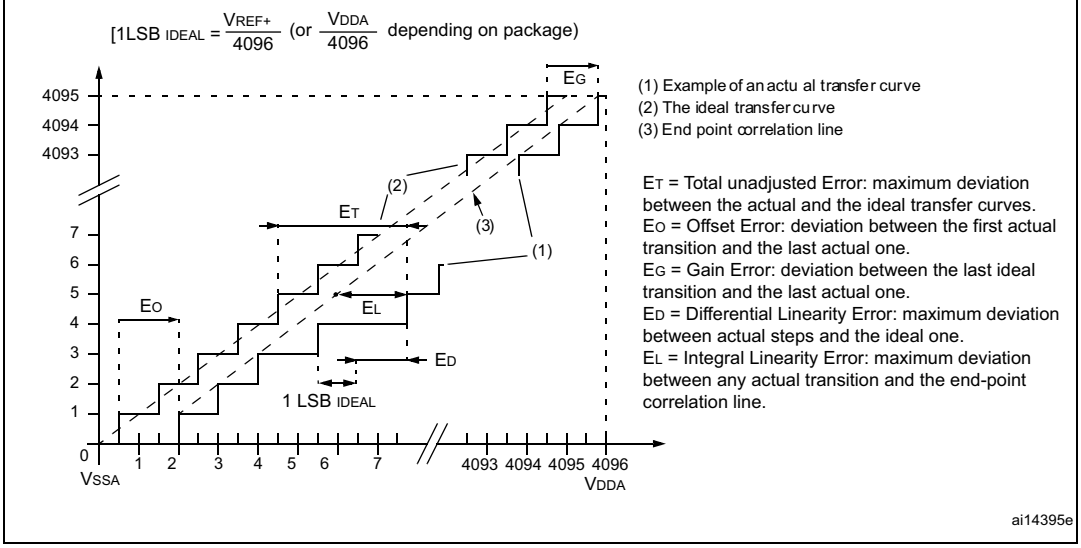


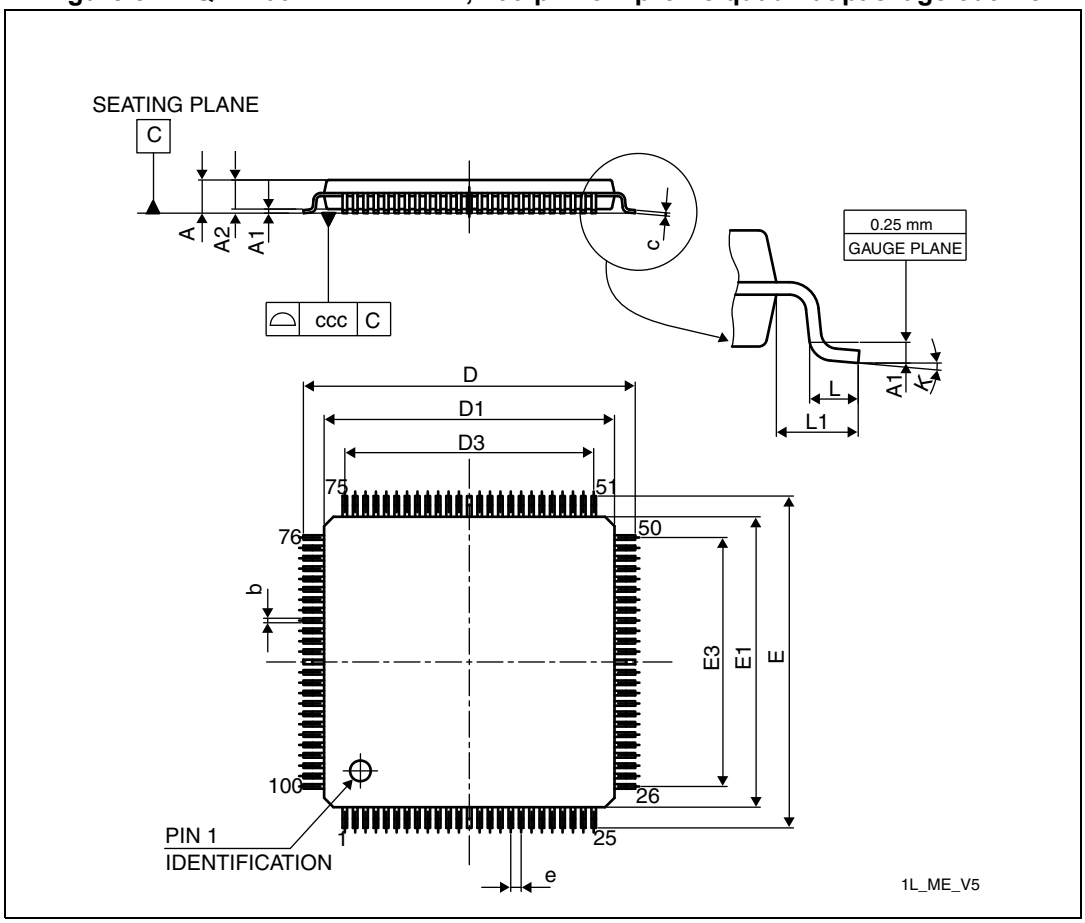
Table 59. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs.
I_{DDA}	DAC DC current consumption in quiescent mode(3)	-	-	380	µA	With no load, middle code (0x800) on the inputs.
		-	-	480	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs.
DNL(1)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(1)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset(1)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±10	mV	
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V.
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V.
Gain error(1)	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration.
$t_{SETTLINGV}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
Update rate(1)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
t_{WAKEUP}(1)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. Quiescent mode refers to the state of the DAC when a steady value is kept on the output so that no dynamic consumption is involved.

6.2 LQFP100 package information

Figure 57. LQFP100 – 14 x 14 mm, 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 62. LQPF100 – 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.622	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.622	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591

Table 66. Document revision history (continued)

Date	Revision	Changes
19-Apr-2011	8	Updated footnotes below *Table 7: Voltage characteristics on page 38* and *Table 8: Current characteristics on page 39* Updated tw min in *Table 21: High-speed external user clock characteristics on page 51* Updated startup time in *Table 24: LSE oscillator characteristics (f_{LSE} = 32.768 kHz) on page 55* Updated *Table 31: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings on page 60* Updated FSMC sync data latency in *Figure 25* thru *Figure 28* Updated *Figure 38: NAND controller waveforms for common memory write access* and *Table 40: Switching characteristics for NAND Flash read and write cycles on page 78* Updated *Figure 44: Recommended NRST pin protection* Added *Section 5.3.13: I/O current injection characteristics* Updated *Section 5.3.13: I/O current injection characteristics* Updated note 2 in *Table 51: I^2C characteristics on page 90* Updated *Figure 45: I^2C bus AC waveforms and measurement circuit(1)*
15-May-2015	9	Added OSC_IN/OSC_OUT remap functions and updated PD0/PD1 in *Table 5: STM32F101xC/STM32F101xD/STM32F101xE pin definitions*. Modified *Section 2.3.21: GPIOs (general-purpose inputs/outputs) on page 20*. Updated notes related to parameters not tested in production in the whole document. Updated *Table 20: Peripheral current consumption on page 50*. Updated CDM standard and values in *Section : Electrostatic discharge (ESD)*. Modified *Section : Output driving current on page 84*. Updated *Figure 43: I/O AC characteristics definition*. Updated conditions related to *Section : I^2C interface characteristics*. Modified *Table 51: I^2C characteristics on page 90*, updated *Figure 45: I^2C bus AC waveforms and measurement circuit(1)* and V_{DD}/V_{DD_I2C} conditions in *Table 52: SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = V_{DD_I2C} = 3.3 V) on page 91*. Modified *Figure 48: SPI timing diagram - master mode(1) on page 95*. Modified note 3 in *Table 58: ADC accuracy on page 98*. Updated I_{DDA} definition in *Table 59: DAC characteristics on page 100* and removed comment related to the offset parameter for ±10 mV. Corrected “CLKL-NOEL” in *Section 5.3.10: FSMC characteristics on page 59*. *Updated Section 6.1: LQFP144 package information on page 103 and added Section : Device marking for LQFP144 on page 106.* *Updated Section 6.2: LQFP100 package information on page 107 and added Section : Device marking for LQFP100 on page 109.* *Updated Section 6.3: LQFP64 information on page 110 and added Section : Device marking for LQFP64 on page 112.*