Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101vdt6tr

Contents

1 **Introduction 9**

2 **Description 10**

2.1 Device overview 11

2.2 Full compatibility throughout the family 14

2.3 Overview 14

2.3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM 14

2.3.2 Embedded Flash memory 15

2.3.3 CRC (cyclic redundancy check) calculation unit 15

2.3.4 Embedded SRAM 15

2.3.5 FSMC (flexible static memory controller) 15

2.3.6 LCD parallel interface 15

2.3.7 Nested vectored interrupt controller (NVIC) 16

2.3.8 External interrupt/event controller (EXTI) 16

2.3.9 Clocks and startup 16

2.3.10 Boot modes 16

2.3.11 Power supply schemes 17

2.3.12 Power supply supervisor 17

2.3.13 Voltage regulator 17

2.3.14 Low-power modes 17

2.3.15 DMA 18

2.3.16 RTC (real-time clock) and backup registers 18

2.3.17 Timers and watchdogs 18

2.3.18 I²C bus 20

2.3.19 Universal synchronous/asynchronous receiver transmitters (USARTs) . 20

2.3.20 Serial peripheral interface (SPI) 20

2.3.21 GPIOs (general-purpose inputs/outputs) 20

2.3.22 ADC (analog to digital converter) 21

2.3.23 DAC (digital-to-analog converter) 21

2.3.24 Temperature sensor 21

2.3.25 Serial wire JTAG debug port (SWJ-DP) 21

2.3.26 Embedded Trace Macrocell™ 22

3 **Pinouts and pin descriptions 23**

Table 46. I/O static characteristics . . . 82
Table 47. Output voltage characteristics . . . 85
Table 48. I/O AC characteristics . . . 86
Table 49. NRST pin characteristics . . . 87
Table 50. TIMx characteristics . . . 89
Table 51. I^2C characteristics . . . 90
Table 52. SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = V_{DD_I2C} = 3.3 V) . . . 91
Table 53. STM32F10xxx SPI characteristics . . . 92
Table 54. SPI characteristics . . . 93
Table 55. ADC characteristics . . . 96
Table 56. R_{AIN} max for f_{ADC} = 14 MHz . . . 97
Table 57. ADC accuracy - limited test conditions . . . 97
Table 58. ADC accuracy . . . 98
Table 59. DAC characteristics . . . 100
Table 60. TS characteristics . . . 102
Table 61. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data . . . 104
Table 62. LQPF100 – 14 x 14 mm, 100-pin low-profile quad flat package mechanical data . . . 107
Table 63. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package mechanical data . . . 110
Table 64. Package thermal characteristics . . . 113
Table 65. Ordering information scheme . . . 115

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101xC, STM32F101xD and STM32F101xE high-densityaccess line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The high-density STM32F101xx datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website.

2.2 Full compatibility throughout the family

The STM32F101xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F101x4 and STM32F101x6 are identified as low-density devices, the STM32F101x8 and STM32F101xB are referred to as medium-density devices, and the STM32F101xC, STM32F101xD and STM32F101xE are referred to as high-density devices .

Low- and high-density devices are an extension of the STM32F101x8/B medium-density devices, they are specified in the STM32F101x4/6 and STM32F101xC/D/E datasheets, respectively.

Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM densities, and additional peripherals like FSMC and DAC, while remaining fully compatible with the other members of the family.

The STM32F101x4, STM32F101x6, STM32F101xC, STM32F101xD and STM32F101xE are a drop-in replacement for the STM32F101x8/B devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F101xx access line family is fully compatible with all existing STM32F103xx performance line and STM32F102xx USB access line devices.

Table 3. STM32F101xx family

<table>
<tr><th rowspan="4">Pinout</th><th colspan="7">Memory size</th></tr>
<tr><th colspan="2">Low-density devices</th><th colspan="2">Medium-density devices</th><th colspan="3">High-density devices</th></tr>
<tr><th>16 KB Flash</th><th>32 KB Flash(1)</th><th>64 KB Flash</th><th>128 KB Flash</th><th>256 KB Flash</th><th>384 KB Flash</th><th>512 KB Flash</th></tr>
<tr><th>4 KB RAM</th><th>6 KB RAM</th><th>10 KB RAM</th><th>16 KB RAM</th><th>32 KB RAM</th><th>48 KB RAM</th><th>48 KB RAM</th></tr>
<tr><td>144</td><td colspan="4" rowspan="2"></td><td colspan="3" rowspan="2">5 × USARTs
4 × 16-bit timers. 2 × basic timers
3 × SPIs, 2 × I2Cs, 1 × ADC. 2 × DACs
FSMC (100 and 144 pins)</td></tr>
<tr><td>100</td><td colspan="2" rowspan="2">3 × USARTs
3 × 16-bit timers
2 × SPIs, 2 × I2Cs,
1 × ADC</td></tr>
<tr><td>64</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I2C
1 × ADC</td><td colspan="3" rowspan="2"></td></tr>
<tr><td>48</td></tr>
<tr><td>36</td><td colspan="5"></td></tr>
</table>

1. For orderable part numbers that do not show the A internal code after the temperature range code (6), the reference datasheet for electrical characteristics is that of the STM32F101x8/B medium-density devices.

2.3 Overview

2.3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while

2.3.7 Nested vectored interrupt controller (NVIC)

The STM32F101xC, STM32F101xD and STM32F101xE access line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers are used to configure the AHB frequency, the high-speed APB (APB2) domain and the low-speed APB (APB1) domain. The maximum frequency of the AHB and APB domains is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The bootloader is located in system memory. It is used to reprogram the Flash memory by using USART1.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.15 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose and basic timers TIMx, DAC and ADC.

2.3.16 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.17 Timers and watchdogs

The high-density STM32F101xx access line devices include up to four general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the general-purpose and basic timers.

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
12	-	-	PF2	I/O	FT	PF2	FSMC_A2	-
13	-	-	PF3	I/O	FT	PF3	FSMC_A3	-
14	-	-	PF4	I/O	FT	PF4	FSMC_A4	-
15	-	-	PF5	I/O	FT	PF5	FSMC_A5	-
16	-	10	V_{SS_5}	S	-	V_{SS_5}	-	-
17	-	11	V_{DD_5}	S	-	V_{DD_5}	-	-
18	-	-	PF6	I/O	-	PF6	FSMC_NIORD	-
19	-	-	PF7	I/O	-	PF7	FSMC_NREG	-
20	-	-	PF8	I/O	-	PF8	FSMC_NIOWR	-
21	-	-	PF9	I/O	-	PF9	FSMC_CD	-
22	-	-	PF10	I/O	-	PF10	FSMC_INTR	-
23	5	12	OSC_IN	I	-	OSC_IN	-	PD0(7)
24	6	13	OSC_OUT	O	-	OSC_OUT	-	PD1(7)
25	7	14	NRST	I/O	-	NRST	-	-
26	8	15	PC0	I/O	-	PC0	ADC_IN10	-
27	9	16	PC1	I/O	-	PC1	ADC_IN11	-
28	10	17	PC2	I/O	-	PC2	ADC_IN12	-
29	11	18	PC3	I/O	-	PC3	ADC_IN13	-
30	12	19	V_{SSA}	S	-	V_{SSA}	-	-
31	-	20	V_{REF-}	S	-	V_{REF-}	-	-
32	-	21	V_{REF+}	S	-	V_{REF+}	-	-
33	13	22	V_{DDA}	S	-	V_{DDA}	-	-
34	14	23	PA0-WKUP	I/O	-	PA0	WKUP/ USART2_CTS(8)/ ADC_IN0/TIM5_CH1/ TIM2_CH1_ETR(8)	-
35	15	24	PA1	I/O	-	PA1	USART2_RTS(8)/ ADC_IN1/TIM5_CH2 TIM2_CH2(8)	-
36	16	25	PA2	I/O	-	PA2	USART2_TX(8)/ TIM5_CH3/ADC_IN2/ TIM2_CH3(8)	-

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
88	-	-	PG3	I/O	FT	PG3	FSMC_A13	-
89	-	-	PG4	I/O	FT	PG4	FSMC_A14	-
90	-	-	PG5	I/O	FT	PG5	FSMC_A15	-
91	-	-	PG6	I/O	FT	PG6	FSMC_INT2	-
92	-	-	PG7	I/O	FT	PG7	FSMC_INT3	-
93	-	-	PG8	I/O	FT	PG8	-	-
94	-	-	V_{SS_9}	S	-	V_{SS_9}	-	-
95	-	-	V_{DD_9}	S	-	V_{DD_9}	-	-
96	37	63	PC6	I/O	FT	PC6	-	TIM3_CH1
97	38	64	PC7	I/O	FT	PC7	-	TIM3_CH2
98	39	65	PC8	I/O	FT	PC8	-	TIM3_CH3
99	40	66	PC9	I/O	FT	PC9	-	TIM3_CH4
100	41	67	PA8	I/O	FT	PA8	USART1_CK/ MCO	-
101	42	68	PA9	I/O	FT	PA9	USART1_TX(8)	-
102	43	69	PA10	I/O	FT	PA10	USART1_RX(8)	-
103	44	70	PA11	I/O	FT	PA11	USART1_CTS	-
104	45	71	PA12	I/O	FT	PA12	USART1_RTS	-
105	46	72	PA13	I/O	FT	JTMS-SWDIO	-	PA13
106	-	73	Not connected					
107	47	74	V_{SS_2}	S	-	V_{SS_2}	-	-
108	48	75	V_{DD_2}	S	-	V_{DD_2}	-	-
109	49	76	PA14	I/O	FT	JTCK-SWCLK	-	PA14
110	50	77	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR/ PA15 /SPI1_NSS
111	51	78	PC10	I/O	FT	PC10	UART4_TX	USART3_TX
112	52	79	PC11	I/O	FT	PC11	UART4_RX	USART3_RX
113	53	80	PC12	I/O	FT	PC12	UART5_TX	USART3_CK
114	-	81	PD0	I/O	FT	OSC_IN(8)	FSMC_D2(9)	-
115	-	82	PD1	I/O	FT	OSC_OUT(8)	FSMC_D3(9)	-

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 12. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(2)	Reset temporization	-	1.5	2.5	3.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Sleep mode	External clock(2) all peripherals enabled	36 MHz	24	mA
			24 MHz	17	
			16 MHz	12.5	
			8 MHz	8	
		External clock(2), all peripherals disabled	36 MHz	6	
			24 MHz	5	
			16 MHz	4.5	
			8 MHz	4	

1. Guaranteed by characterization results, tested in production at V_{DD} max, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max	Unit
			V_{DD}/ V_{BAT} = 2.0 V	V_{DD}/ V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	34.5	35	379	µA
		Regulator in Low-power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	24.5	25	365	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	3	3.8	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.8	3.6	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.9	2.1	5(2)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.05	1.1	1.4	2(2)	

1. Typical values are measured at T_A = 25 °C.
2. Guaranteed by characterization results, not tested in production.

Figure 13. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

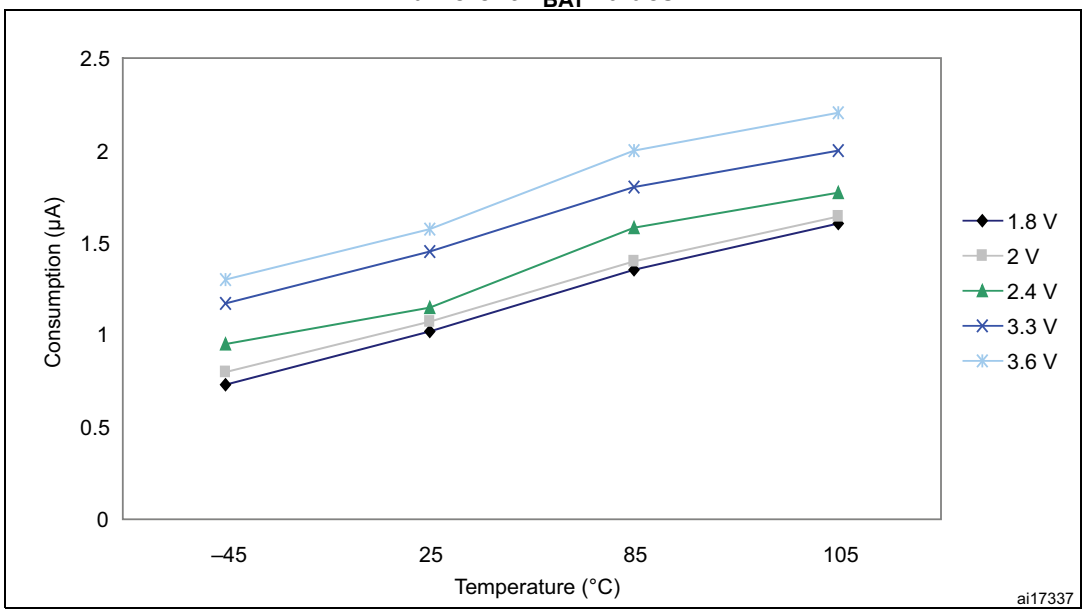


Figure 14. Typical current consumption in Stop mode with regulator in run mode versus temperature at different V_{DD} values

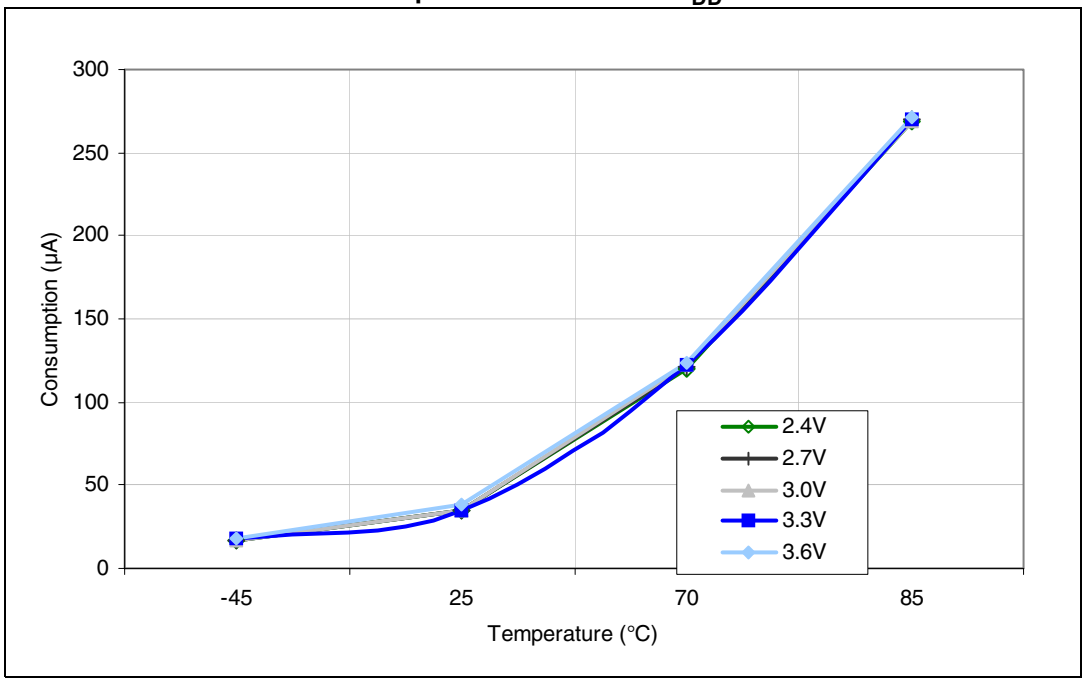


Table 19. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)	Typ(1)	Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	36 MHz	15.1	3.6	mA
			24 MHz	10.4	2.6	
			16 MHz	7.2	2	
			8 MHz	3.9	1.3	
			4 MHz	2.6	1.2	
			2 MHz	1.85	1.15	
			1 MHz	1.5	1.1	
			500 kHz	1.3	1.05	
			125 kHz	1.2	1.05	
		Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	14.5	3	
			24 MHz	9.8	2	
			16 MHz	6.6	1.4	
			8 MHz	3.3	0.7	
			4 MHz	2	0.6	
			2 MHz	1.25	0.55	
			1 MHz	0.9	0.5	
			500 kHz	0.7	0.45	
			125 kHz	0.6	0.45	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 20*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 7*.

Table 36. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	55.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_Nex low (x = 0...2)	-	2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	3	-	ns
$t_{d(CLKL-Data)}$	FSMC_A/D[15:0] valid after FSMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 43* and *Table 48*, respectively.

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 48. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$F_{max(IO)out}$	Maximum Frequency(2)	C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 43*.
3. Guaranteed by design, not tested in production.

Table 55. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 56* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 3: Pinouts and pin descriptions* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 55*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

Table 58. ADC accuracy(1) (2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.
4. Guaranteed by characterization results, not tested in production.

Figure 49. ADC accuracy characteristics

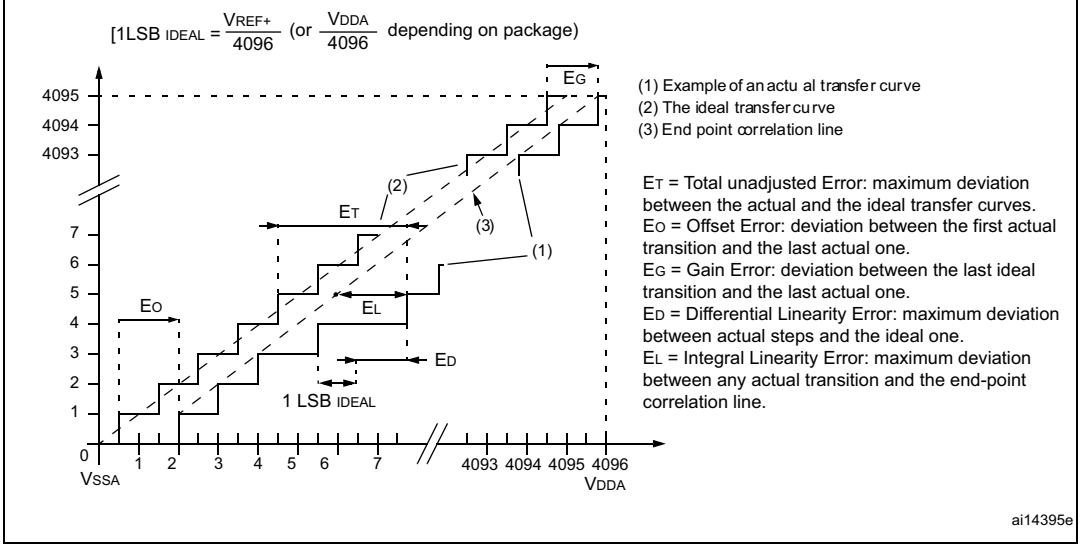
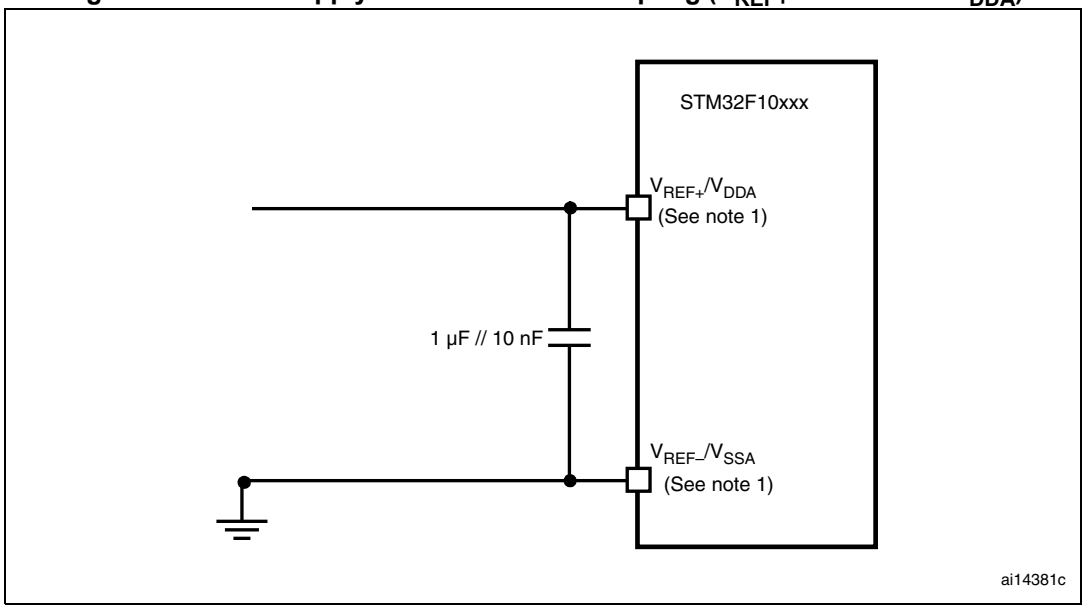


Figure 52. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.19 DAC electrical specifications

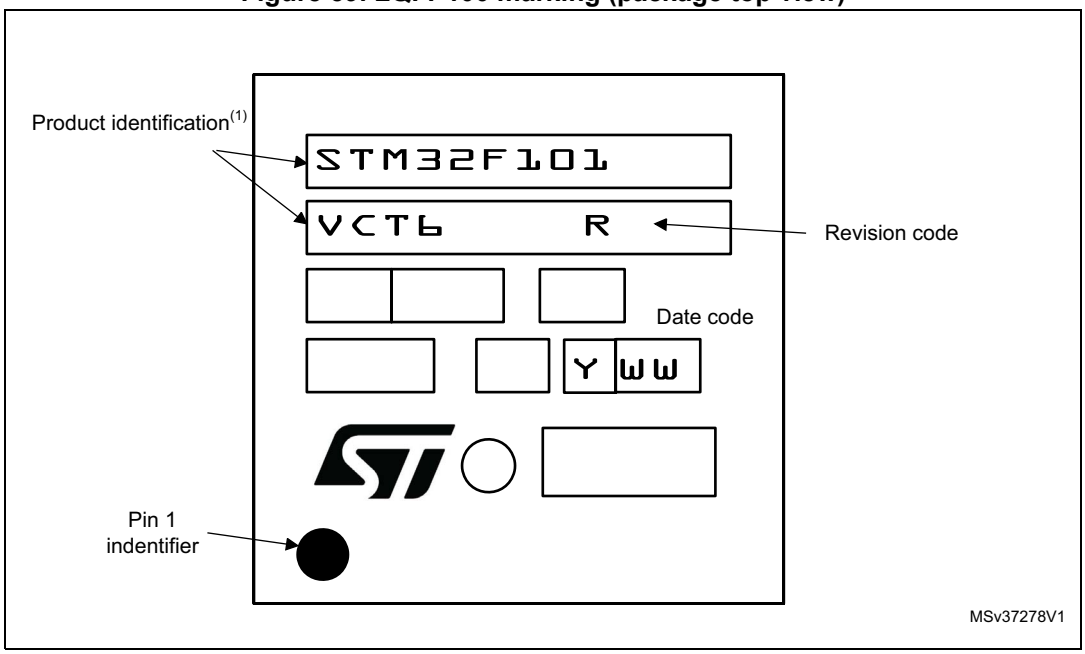
Table 59. DAC characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	
V_{REF+}	Reference supply voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	
R_{LOAD}(2)	Resistive load with buffer ON	5	-	-	kΩ	
R_O(2)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(2)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) and (0xEAB) at V_{REF+} = 2.4 V.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(2)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(2)	Higher DAC_OUT voltage with buffer OFF	-		V_{REF+} – 1LSB	V	

Device marking for LQFP100

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 59. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.4.2 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 65: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F10xxx junction temperature range.

Example: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 65* T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

T_{Jmax} = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the junction temperature range of the STM32F10xxx (–40 < T_J < 105 °C).

Figure 63. LQFP64 P_D max vs. T_A

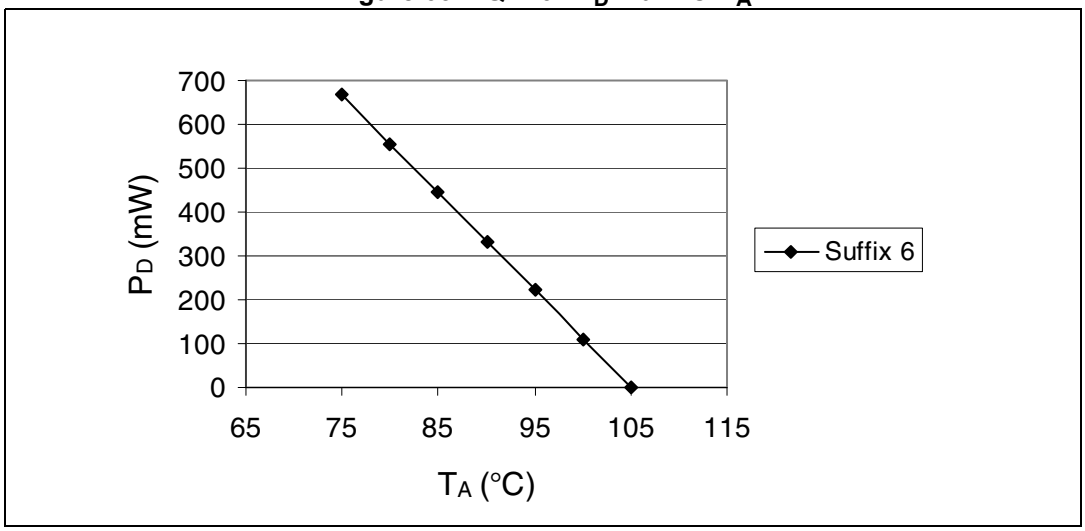


Table 66. Document revision history (continued)

Date	Revision	Changes
30-Mar-2009	5	I/O information clarified on cover page, Number of ADC peripherals corrected in *Table 2: STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts*. In *Table 5: STM32F101xC/STM32F101xD/STM32F101xE pin definitions*: – I/O level of pins PF11, PF12, PF13, PF14, PF15, G0, G1 and G15 updated – PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column. PG14 pin description modified in *Table 6: FSMC pin definition*, *Figure 6: Memory map on page 35* modified. Note modified in *Table 14: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 16: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 14*, *Figure 15* and *Figure 16* show typical curves (titles changed). *Table 21: High-speed external user clock characteristics* and *Table 22: Low-speed user external clock characteristics* modified. ACC_{HSI} max values modified in *Table 25: HSI oscillator characteristics* FSMC configuration modified for *Asynchronous waveforms and timings*. Notes modified below *Figure 21: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms* and *Figure 22: Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms*. $t_{w(NADV)}$ values modified in *Table 31: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings* and *Table 34: Asynchronous multiplexed NOR/PSRAM write timings*. $t_{h(Data\_NWE)}$ modified in *Table 32: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings*. In *Table 36: Synchronous multiplexed PSRAM write timings* and *Table 38: Synchronous non-multiplexed PSRAM write timings*: – $t_{v(Data-CLK)}$ renamed as $t_{d(CLKL-Data)}$ – $t_{d(CLKL-Data)}$ min value removed and max value added – $t_{h(CLKL-DV)}$ / $t_{h(CLKL-ADV)}$ removed *Figure 25: Synchronous multiplexed NOR/PSRAM read timings*. *Figure 26: Synchronous multiplexed PSRAM write timings* and *Figure 28: Synchronous non-multiplexed PSRAM write timings* modified, Small text changes.