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What is "Embedded - Microcontrollers"?

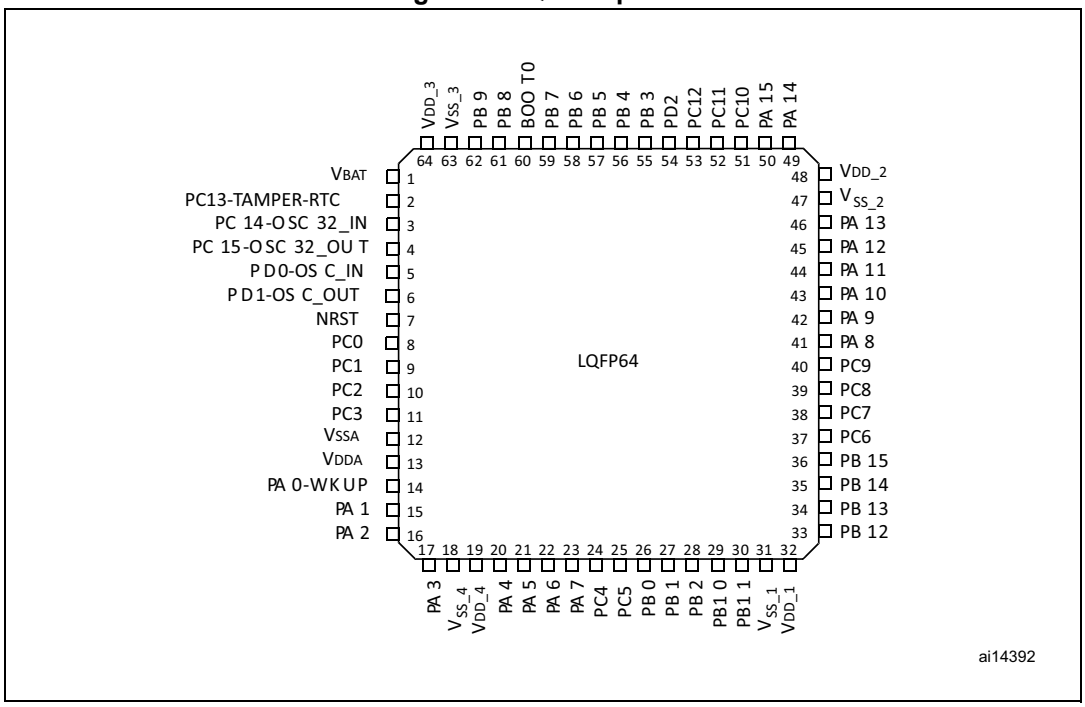
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101vet6

Contents

Figure 5. LQFP64 pinout



1. The above figure shows the package top view.

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
1	-	1	PE2	I/O	FT	PE2	TRACECLK/ FSMC_A23	-
2	-	2	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	-
3	-	3	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	-
4	-	4	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	-
5	-	5	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	-
6	1	6	V_{BAT}	S	-	V_{BAT}	-	-
7	2	7	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
8	3	8	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
9	4	9	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
10	-	-	PF0	I/O	FT	PF0	FSMC_A0	-
11	-	-	PF1	I/O	FT	PF1	FSMC_A1	-

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
88	-	-	PG3	I/O	FT	PG3	FSMC_A13	-
89	-	-	PG4	I/O	FT	PG4	FSMC_A14	-
90	-	-	PG5	I/O	FT	PG5	FSMC_A15	-
91	-	-	PG6	I/O	FT	PG6	FSMC_INT2	-
92	-	-	PG7	I/O	FT	PG7	FSMC_INT3	-
93	-	-	PG8	I/O	FT	PG8	-	-
94	-	-	V_{SS_9}	S	-	V_{SS_9}	-	-
95	-	-	V_{DD_9}	S	-	V_{DD_9}	-	-
96	37	63	PC6	I/O	FT	PC6	-	TIM3_CH1
97	38	64	PC7	I/O	FT	PC7	-	TIM3_CH2
98	39	65	PC8	I/O	FT	PC8	-	TIM3_CH3
99	40	66	PC9	I/O	FT	PC9	-	TIM3_CH4
100	41	67	PA8	I/O	FT	PA8	USART1_CK/ MCO	-
101	42	68	PA9	I/O	FT	PA9	USART1_TX(8)	-
102	43	69	PA10	I/O	FT	PA10	USART1_RX(8)	-
103	44	70	PA11	I/O	FT	PA11	USART1_CTS	-
104	45	71	PA12	I/O	FT	PA12	USART1_RTS	-
105	46	72	PA13	I/O	FT	JTMS-SWDIO	-	PA13
106	-	73	Not connected					
107	47	74	V_{SS_2}	S	-	V_{SS_2}	-	-
108	48	75	V_{DD_2}	S	-	V_{DD_2}	-	-
109	49	76	PA14	I/O	FT	JTCK-SWCLK	-	PA14
110	50	77	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR/ PA15 /SPI1_NSS
111	51	78	PC10	I/O	FT	PC10	UART4_TX	USART3_TX
112	52	79	PC11	I/O	FT	PC11	UART4_RX	USART3_RX
113	53	80	PC12	I/O	FT	PC12	UART5_TX	USART3_CK
114	-	81	PD0	I/O	FT	OSC_IN(8)	FSMC_D2(9)	-
115	-	82	PD1	I/O	FT	OSC_OUT(8)	FSMC_D3(9)	-

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
116	54	83	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX	-
117	-	84	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
118	-	85	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
119	-	86	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
120	-	-	V_{SS_10}	S	-	V_{SS_10}	-	-
121	-	-	V_{DD_10}	S	-	V_{DD_10}	-	-
122	-	87	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
123	-	88	PD7	I/O	FT	PD7	FSMC_NE1/ FSMC_NCE2	USART2_CK
124	-	-	PG9	I/O	FT	PG9	FSMC_NE2/ FSMC_NCE3	-
125	-	-	PG10	I/O	FT	PG10	FSMC_NE3/ FSMC_NCE4_1	-
126	-	-	PG11	I/O	FT	PG11	FSMC_NCE4_2	-
127	-	-	PG12	I/O	FT	PG12	FSMC_NE4	-
128	-	-	PG13	I/O	FT	PG13	FSMC_A24	-
129	-	-	PG14	I/O	FT	PG14	FSMC_A25	-
130	-	-	V_{SS_11}	S	-	V_{SS_11}	-	-
131	-	-	V_{DD_11}	S	-	V_{DD_11}	-	-
132	-	-	PG15	I/O	FT	PG15	-	-
133	55	89	PB3	I/O	FT	JTDO	SPI3_SCK	TIM2_CH2 /PB3 TRACESWO SPI1_SCK
134	56	90	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 / TIM3_CH1 SPI1_MISO
135	57	91	PB5	I/O		PB5	I2C1_SMBA/ SPI3_MOSI	TIM3_CH2 / SPI1_MOSI
136	58	92	PB6	I/O	FT	PB6	I2C1_SCL/ TIM4_CH1(8)	USART1_TX
137	59	93	PB7	I/O	FT	PB7	I2C1_SDA/FSMC_NADV TIM4_CH2(8)	USART1_RX
138	60	94	BOOT0	I	-	BOOT0	-	-
139	61	95	PB8	I/O	FT	PB8	TIM4_CH3 (8)	I2C1_SCL

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
140	62	96	PB9	I/O	FT	PB9	TIM4_CH4 (8)	I2C1_SDA
141	-	97	PE0	I/O	FT	PE0	TIM4_ETR(8)/ FSMC_NBL0	-
142	-	98	PE1	I/O	FT	PE1	FSMC_NBL1	-
143	63	99	V_{SS_3}	S	-	V_{SS_3}	-	-
144	64	100	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and LQFP144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual
8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
9. For devices delivered in LQFP64 packages, the FSMC function is not available.

5.3.4 Embedded reference voltage

The parameters given in *Table 13* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 13. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	100	ppm/ °C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 14* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A = 85 °C	
I_{DD}	Supply current in Sleep mode	External clock(2) all peripherals enabled	36 MHz	24	mA
			24 MHz	17	
			16 MHz	12.5	
			8 MHz	8	
		External clock(2), all peripherals disabled	36 MHz	6	
			24 MHz	5	
			16 MHz	4.5	
			8 MHz	4	

1. Guaranteed by characterization results, tested in production at V_{DD} max, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max	Unit
			V_{DD}/ V_{BAT} = 2.0 V	V_{DD}/ V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	34.5	35	379	µA
		Regulator in Low-power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	24.5	25	365	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	3	3.8	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.8	3.6	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.9	2.1	5(2)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.05	1.1	1.4	2(2)	

1. Typical values are measured at T_A = 25 °C.
2. Guaranteed by characterization results, not tested in production.

Table 32. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	t_{HCLK}	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	5.5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	t_{HCLK} + 1.5	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 23. Asynchronous multiplexed NOR/PSRAM read waveforms

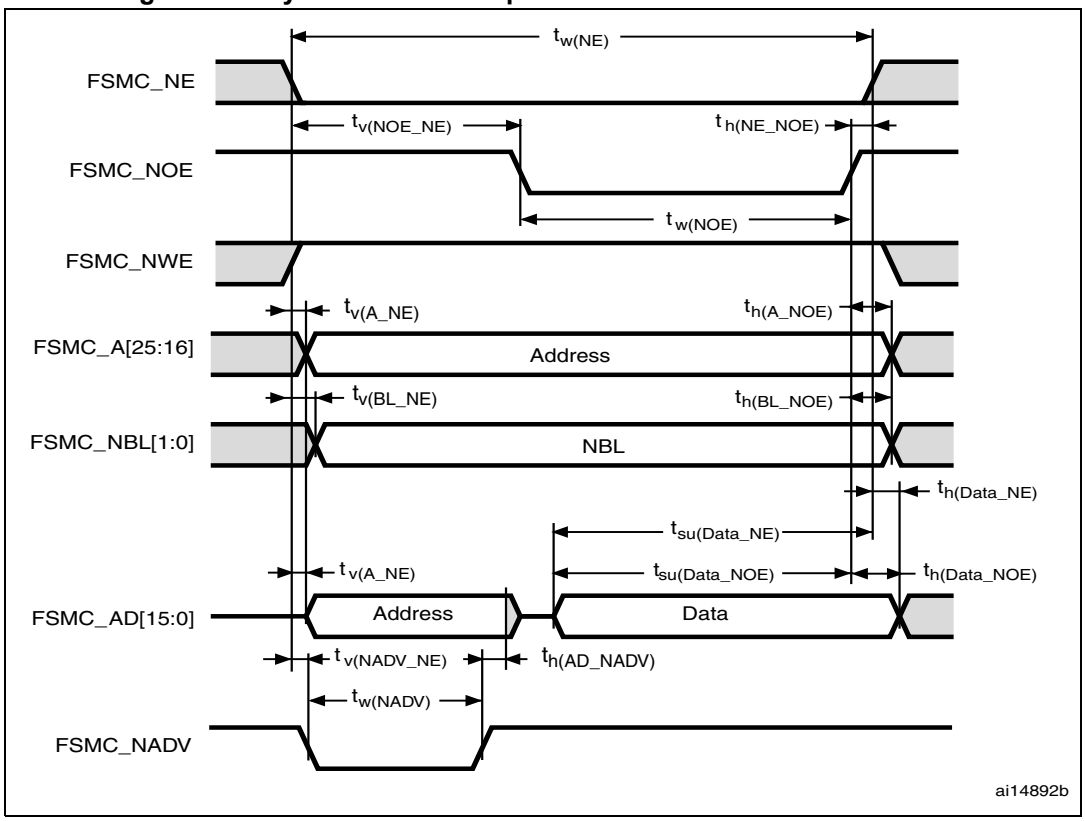


Table 33. Asynchronous multiplexed NOR/PSRAM read timings(1)(2)

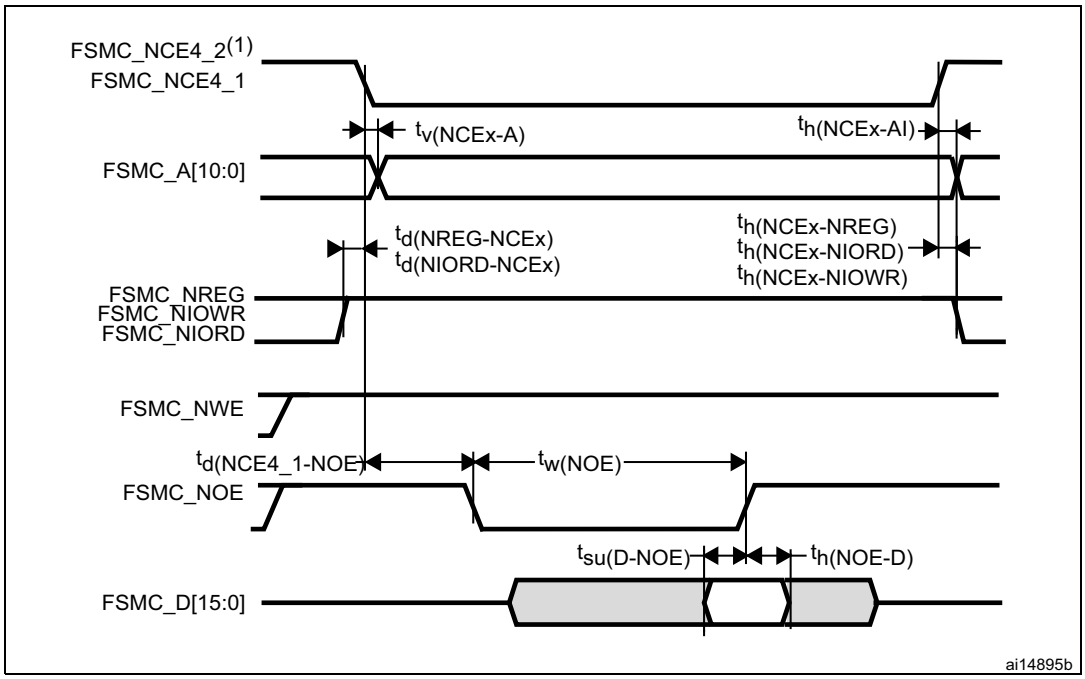
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7t_{HCLK} - 2$	$7t_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK} - 0.5$	$3t_{HCLK} + 1.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4t_{HCLK} - 1$	$4t_{HCLK} + 2$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	–1	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	3	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	t_{HCLK} –1.5	t_{HCLK} + 1.5	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK}	-	ns

Table 35. Synchronous multiplexed NOR/PSRAM read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	55.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKH-NOEL)}$	FSMC_CLK high to FSMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	0.5	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	FSMC_A/D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production..

Figure 29. PC Card/CompactFlash controller waveforms for common memory read access



1. FSMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 30. PC Card/CompactFlash controller waveforms for common memory write access

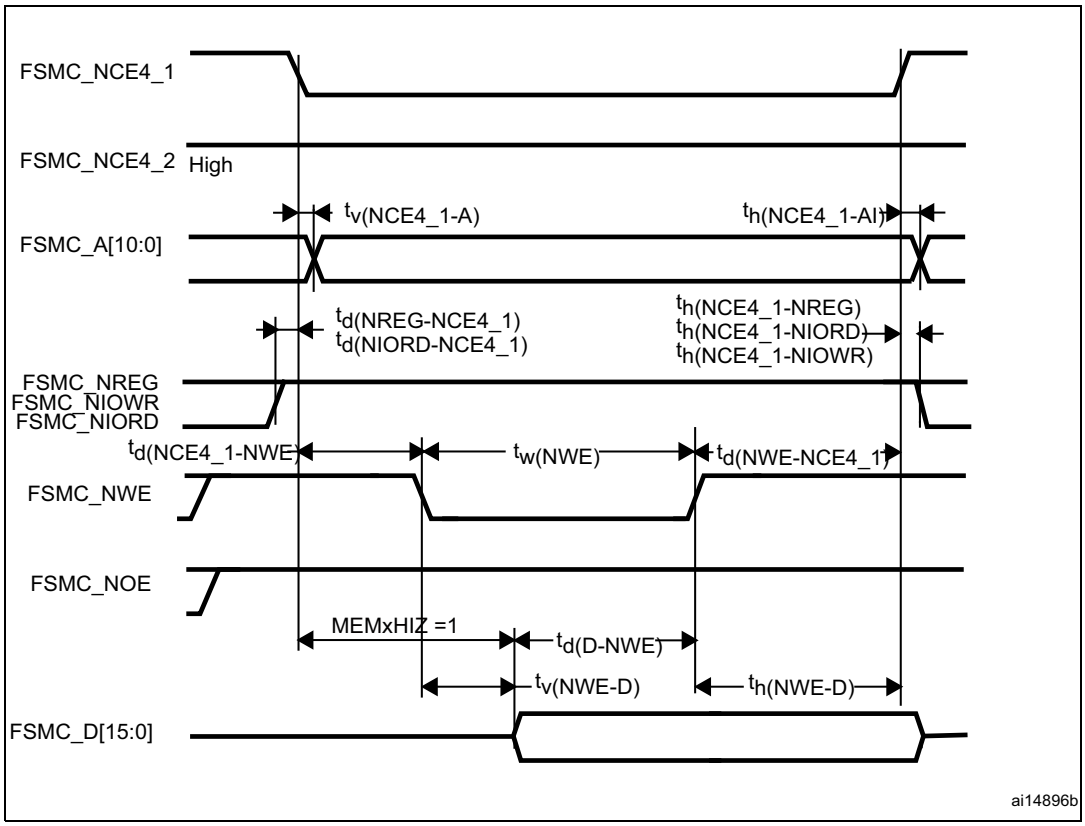


Figure 39. Standard I/O input characteristics - CMOS port

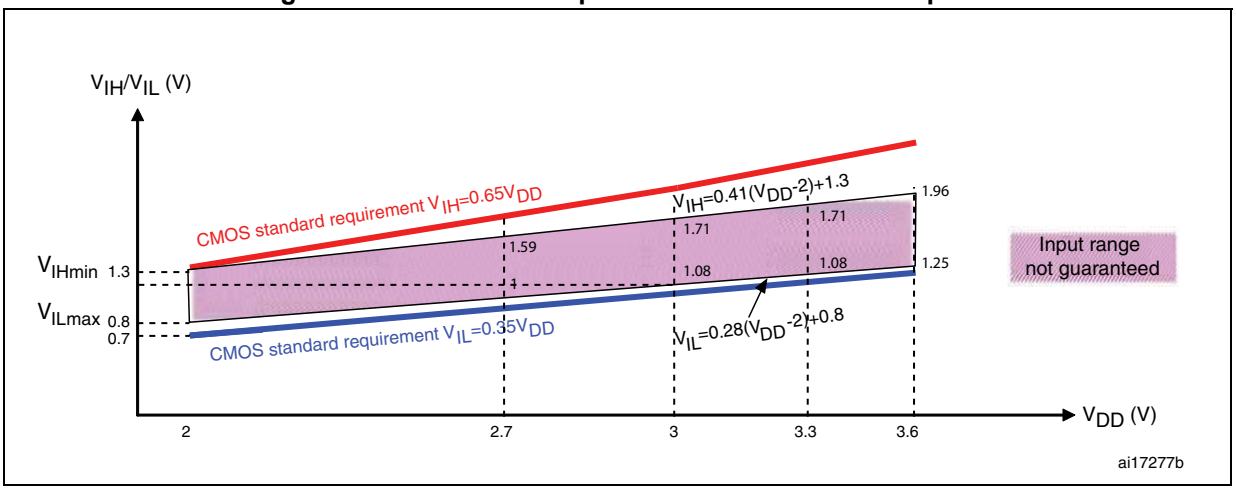
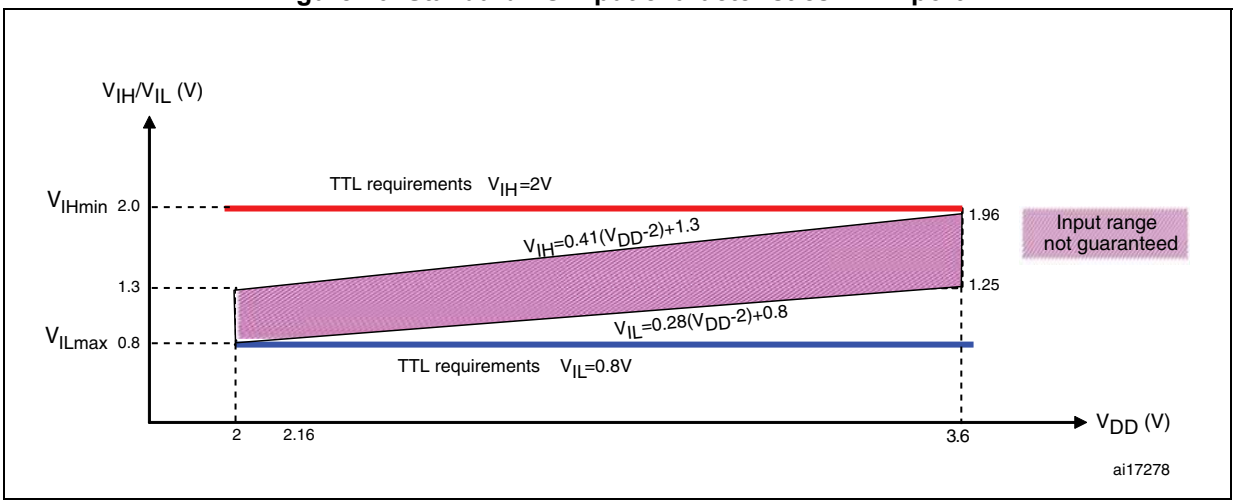


Figure 40. Standard I/O input characteristics - TTL port



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 43* and *Table 48*, respectively.

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 48. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$F_{max(IO)out}$	Maximum Frequency(2)	C_L= 30 pF, V_{DD} = 2.7 V to 3.6 V	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 43*.
3. Guaranteed by design, not tested in production.

Figure 46. SPI timing diagram - slave mode and CPHA=0

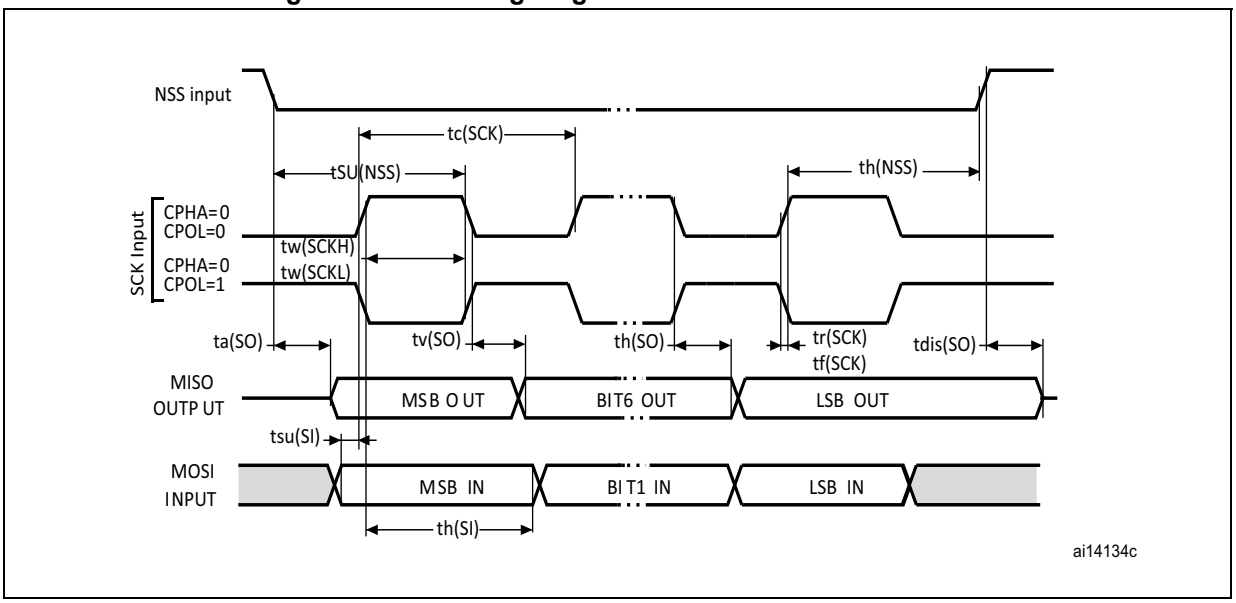
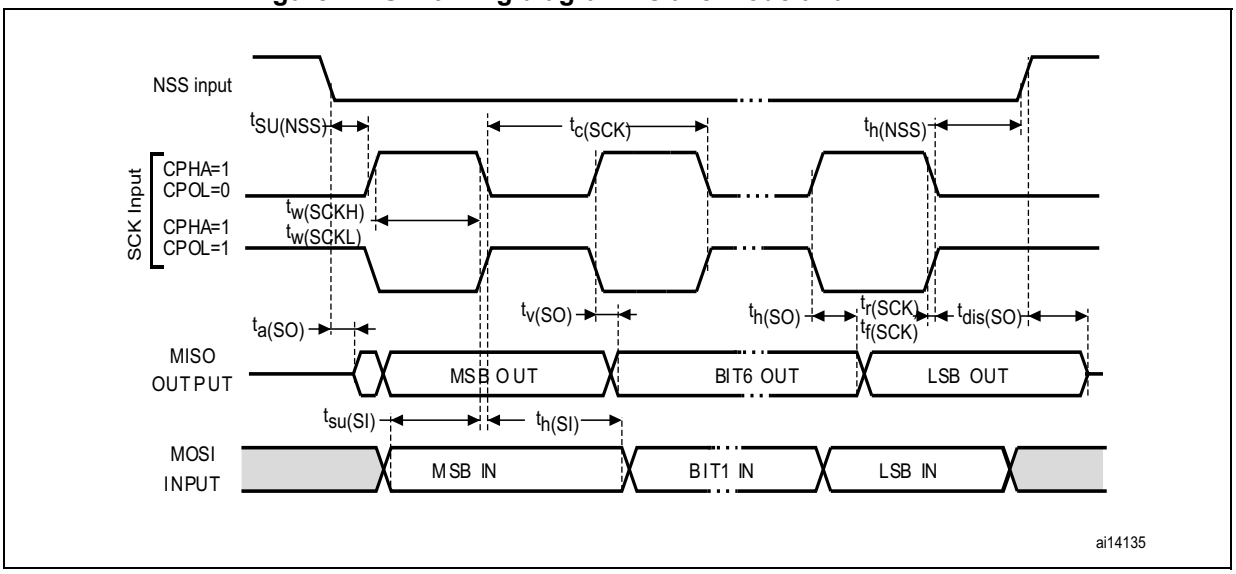


Figure 47. SPI timing diagram - slave mode and CPHA=1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 55. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 56* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 3: Pinouts and pin descriptions* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 55*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 56. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 57. ADC accuracy - limited test conditions(1)(2)

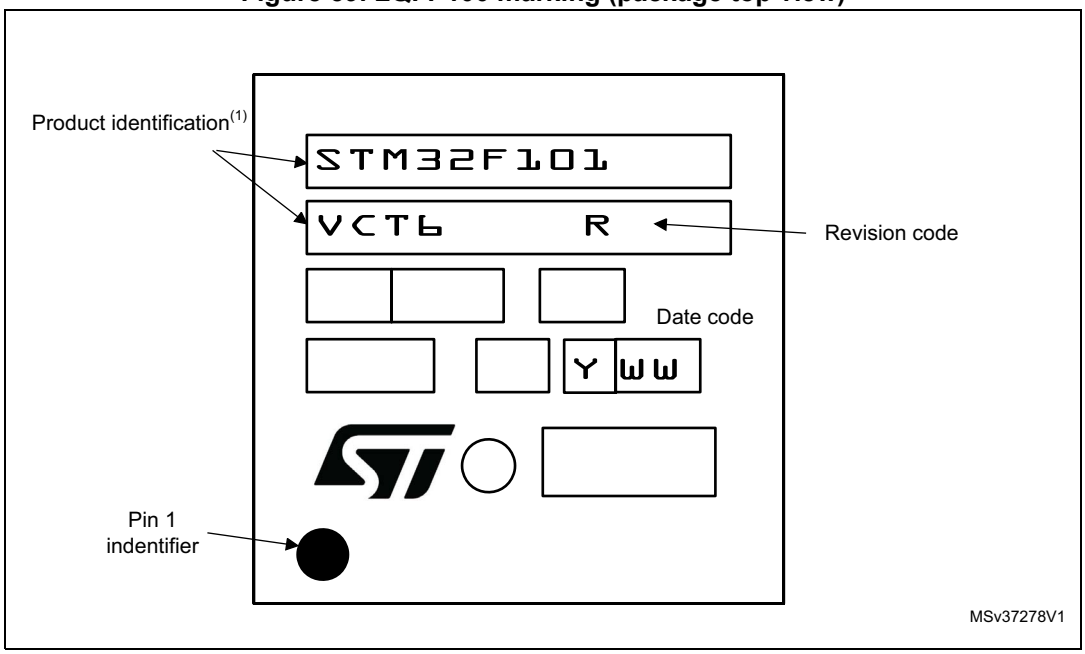
Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V, T_A = 25 °C Measurements made after ADC calibration V_{REF+} = V_{DDA}	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.
3. Guaranteed by characterization results, not tested in production.

Device marking for LQFP100

The following figure gives an example of topside marking and pin 1 position identifier location.

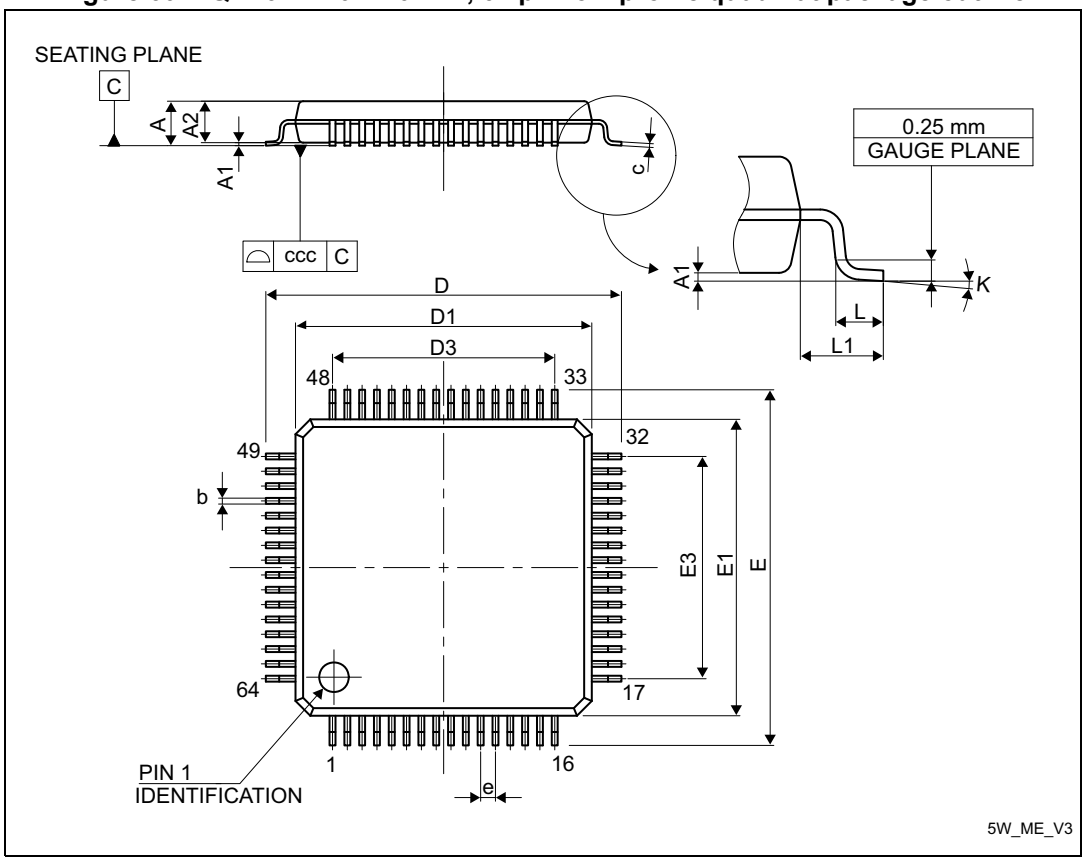
Figure 59. LQFP100 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.3 LQFP64 information

Figure 60. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 63. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-

Table 66. Document revision history (continued)

Date	Revision	Changes
21-Jul-2009	6	*Figure 1: STM32F101xC, STM32F101xD and STM32F101xE access line block diagram* modified. *Note 5* updated and *Note 4* added in *Table 5: STM32F101xC/STM32F101xD/STM32F101xE pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 13: Embedded internal reference voltage*. f_{HSE_ext} min modified in *Table 21: High-speed external user clock characteristics*. *Table 23: HSE 4-16 MHz oscillator characteristics* modified. *Note 1* modified below *Figure 19: Typical application with an 8 MHz crystal*. *Figure 44: Recommended NRST pin protection* modified. C_{L1} and C_{L2} replaced by C in *Table 23: HSE 4-16 MHz oscillator characteristics* and *Table 24: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)*, notes modified and moved below the tables. *Table 25: HSI oscillator characteristics* modified. Conditions removed from *Table 27: Low-power mode wakeup timings*. Jitter added to *Table 28: PLL characteristics*. In *Table 31: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings*: $t_{h(BL\_NOE)}$ and $t_{h(A\_NOE)}$ modified. In *Table 32: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings*: $t_{h(A\_NWE)}$ and $t_{h(Data\_NWE)}$ modified. In *Table 33: Asynchronous multiplexed NOR/PSRAM read timings*: $t_{h(AD\_NADV)}$ and $t_{h(A\_NOE)}$ modified. In *Table 34: Asynchronous multiplexed NOR/PSRAM write timings*: $t_{h(A\_NWE)}$ modified. In *Table 35: Synchronous multiplexed NOR/PSRAM read timings*: $t_{h(CLKH-NWAITV)}$ modified. In *Table 40: Switching characteristics for NAND Flash read and write cycles*: $t_{h(NOE-D)}$ modified. *Table 54: SPI characteristics* modified. C_{ADC} and R_{AIN} parameters modified in *Table 55: ADC characteristics*. R_{AIN} max values modified in *Table 56: R_{AIN} max for f_{ADC} = 14 MHz*. *Table 59: DAC characteristics* modified. *Figure 53: 12-bit buffered /non-buffered DAC* added.
24-Sep-2009	7	Number of DACs corrected in *Table 3: STM32F101xx family*. I_{DD_VBAT} updated in *Table 17: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 13: Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values* added. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section : on page 78*. *Table 59: DAC characteristics* modified. Small text changes.