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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101vet6tr

2.3.11 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 9: Power supply scheme*.

2.3.12 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

2.3.13 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.3.14 Low-power modes

The STM32F101xC, STM32F101xD and STM32F101xE access line supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 I²C bus

Up to two I²C bus interfaces can operate in multi-master and slave modes. They support standard and fast modes.
They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.19 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F101xC, STM32F101xD and STM32F101xE access line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The five interfaces are able to communicate at speeds of up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.20 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

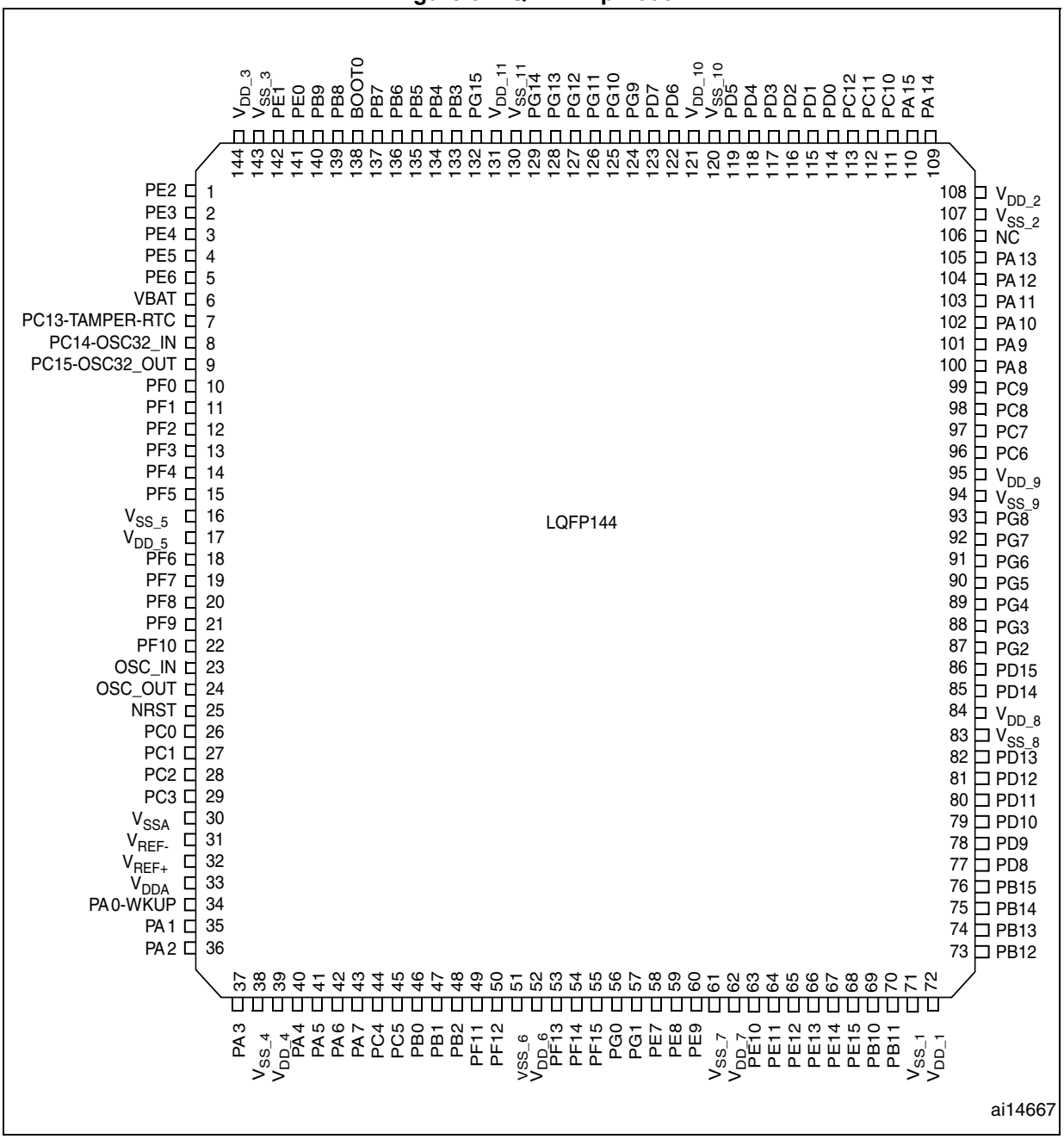
2.3.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

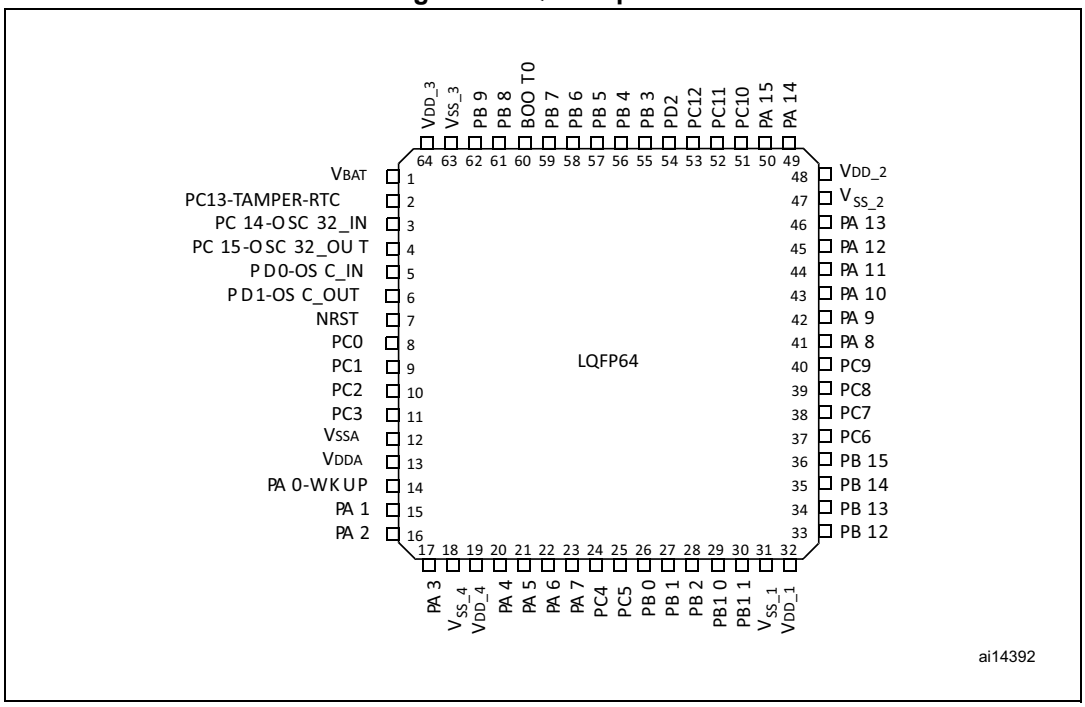
3 Pinouts and pin descriptions

Figure 3. LQFP144 pinout



1. The above figure shows the package top view.

Figure 5. LQFP64 pinout



1. The above figure shows the package top view.

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
1	-	1	PE2	I/O	FT	PE2	TRACECLK/ FSMC_A23	-
2	-	2	PE3	I/O	FT	PE3	TRACED0/FSMC_A19	-
3	-	3	PE4	I/O	FT	PE4	TRACED1/FSMC_A20	-
4	-	4	PE5	I/O	FT	PE5	TRACED2/FSMC_A21	-
5	-	5	PE6	I/O	FT	PE6	TRACED3/FSMC_A22	-
6	1	6	V_{BAT}	S	-	V_{BAT}	-	-
7	2	7	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
8	3	8	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
9	4	9	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
10	-	-	PF0	I/O	FT	PF0	FSMC_A0	-
11	-	-	PF1	I/O	FT	PF1	FSMC_A1	-

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
88	-	-	PG3	I/O	FT	PG3	FSMC_A13	-
89	-	-	PG4	I/O	FT	PG4	FSMC_A14	-
90	-	-	PG5	I/O	FT	PG5	FSMC_A15	-
91	-	-	PG6	I/O	FT	PG6	FSMC_INT2	-
92	-	-	PG7	I/O	FT	PG7	FSMC_INT3	-
93	-	-	PG8	I/O	FT	PG8	-	-
94	-	-	V_{SS_9}	S	-	V_{SS_9}	-	-
95	-	-	V_{DD_9}	S	-	V_{DD_9}	-	-
96	37	63	PC6	I/O	FT	PC6	-	TIM3_CH1
97	38	64	PC7	I/O	FT	PC7	-	TIM3_CH2
98	39	65	PC8	I/O	FT	PC8	-	TIM3_CH3
99	40	66	PC9	I/O	FT	PC9	-	TIM3_CH4
100	41	67	PA8	I/O	FT	PA8	USART1_CK/ MCO	-
101	42	68	PA9	I/O	FT	PA9	USART1_TX(8)	-
102	43	69	PA10	I/O	FT	PA10	USART1_RX(8)	-
103	44	70	PA11	I/O	FT	PA11	USART1_CTS	-
104	45	71	PA12	I/O	FT	PA12	USART1_RTS	-
105	46	72	PA13	I/O	FT	JTMS-SWDIO	-	PA13
106	-	73	Not connected					
107	47	74	V_{SS_2}	S	-	V_{SS_2}	-	-
108	48	75	V_{DD_2}	S	-	V_{DD_2}	-	-
109	49	76	PA14	I/O	FT	JTCK-SWCLK	-	PA14
110	50	77	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR/ PA15 /SPI1_NSS
111	51	78	PC10	I/O	FT	PC10	UART4_TX	USART3_TX
112	52	79	PC11	I/O	FT	PC11	UART4_RX	USART3_RX
113	53	80	PC12	I/O	FT	PC12	UART5_TX	USART3_CK
114	-	81	PD0	I/O	FT	OSC_IN(8)	FSMC_D2(9)	-
115	-	82	PD1	I/O	FT	OSC_OUT(8)	FSMC_D3(9)	-

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
140	62	96	PB9	I/O	FT	PB9	TIM4_CH4 (8)	I2C1_SDA
141	-	97	PE0	I/O	FT	PE0	TIM4_ETR(8)/ FSMC_NBL0	-
142	-	98	PE1	I/O	FT	PE1	FSMC_NBL1	-
143	63	99	V_{SS_3}	S	-	V_{SS_3}	-	-
144	64	100	V_{DD_3}	S	-	V_{DD_3}	-	-

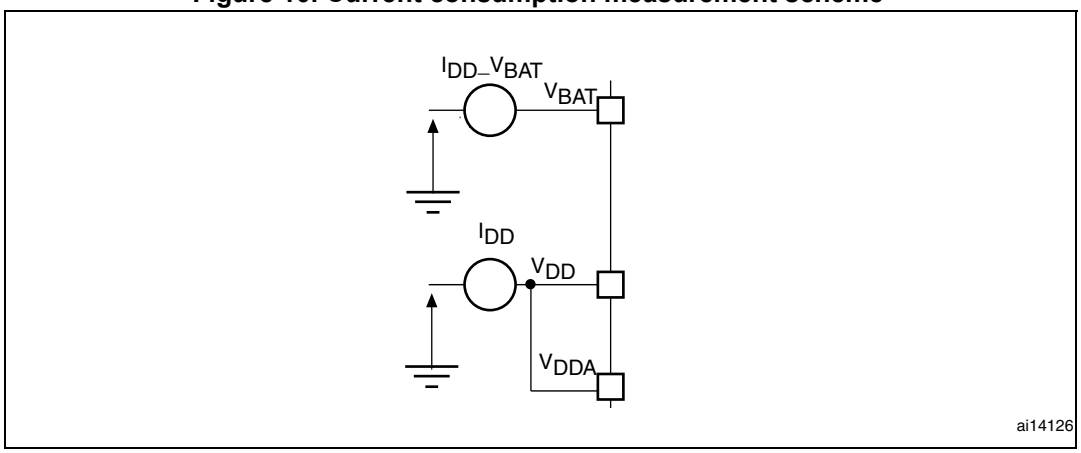
1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and LQFP144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual
8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
9. For devices delivered in LQFP64 packages, the FSMC function is not available.

Table 6. FSMC pin definition

Pins	FSMC					LQFP100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	-	A23	A23	-	Yes
PE3	-	-	A19	A19	-	Yes
PE4	-	-	A20	A20	-	Yes
PE5	-	-	A21	A21	-	Yes
PE6	-	-	A22	A22	-	Yes
PF0	A0	A0	A0	-	-	-
PF1	A1	A1	A1	-	-	-
PF2	A2	A2	A2	-	-	-
PF3	A3	-	A3	-	-	-
PF4	A4	-	A4	-	-	-
PF5	A5	-	A5	-	-	-
PF6	NIORD	NIORD	-	-	-	-
PF7	NREG	NREG	-	-	-	-
PF8	NIOWR	NIOWR	-	-	-	-
PF9	CD	CD	-	-	-	-
PF10	INTR	INTR	-	-	-	-
PF11	NIOS16	NIOS16	-	-	-	-
PF12	A6	-	A6	-	-	-
PF13	A7	-	A7	-	-	-
PF14	A8	-	A8	-	-	-
PF15	A9	-	A9	-	-	-
PG0	A10	-	A10	-	-	-
PG1	-	-	A11	-	-	-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

5.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 7: Voltage characteristics*, *Table 8: Current characteristics*, and *Table 9: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.12: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 8: Current characteristics* for the maximum allowed injected current values.

Figure 15. Typical current consumption in Stop mode with regulator in low-power mode versus temperature at different V_{DD} values

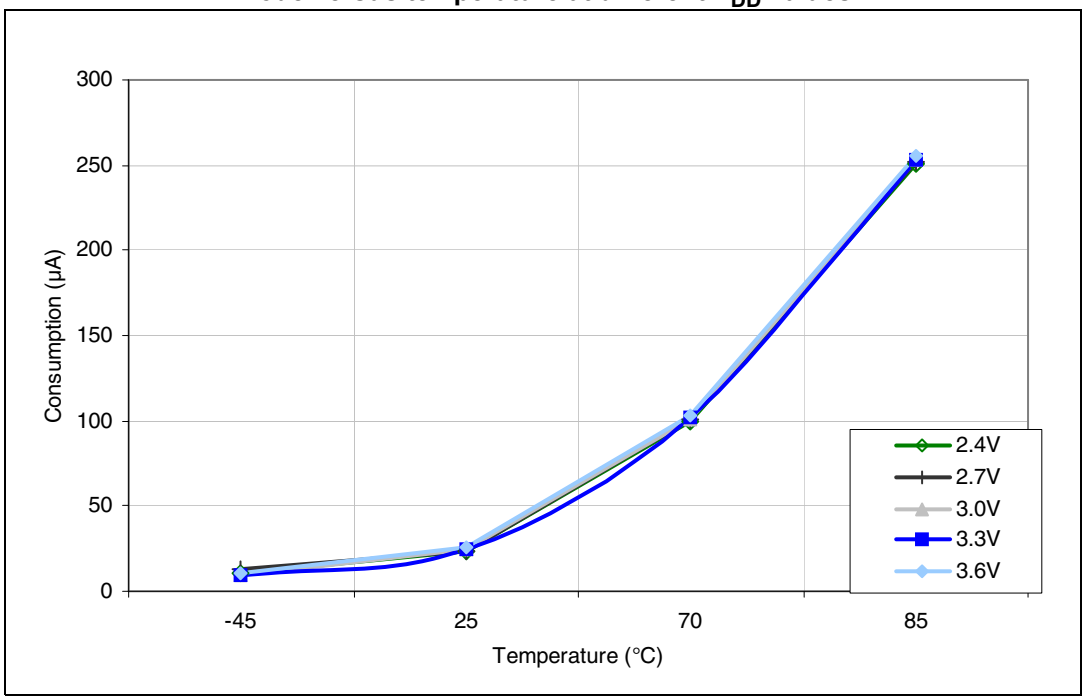


Figure 16. Typical current consumption in Standby mode versus temperature at different V_{DD} values

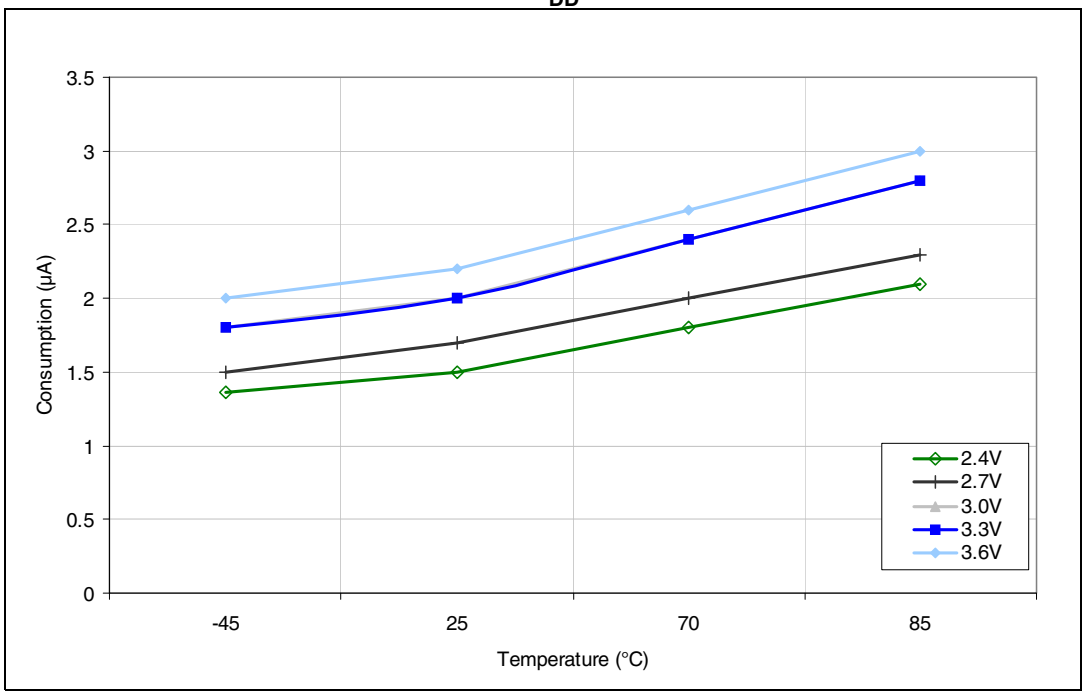


Table 20. Peripheral current consumption(1) (continued)

Peripherals		µA/MHz
APB2 (up to 36 MHz)	APB2-Bridge	4.17
	GPIOA	8.47
	GPIOB	8.47
	GPIOC	6.53
	GPIOD	8.47
	GPIOE	6.53
	GPIOF	6.53
	GPIOG	6.11
	SPI1	4.72
	USART1	12.50
	TIM1	22.92
	TIM8	22.92
	ADC1(5)(6)	17.32

1. f_{HCLK} = 36 MHz, $f_{APB1} = f_{HCLK/2}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master peripheral is ON.
3. When the I2S is enabled, a current consumption of 0.02 mA must be added.
4. When DAC_OUT1 or DAC_OUT2 is enabled, a current consumption of 0.36 mA must be added.
5. Specific conditions for ADC: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK/2}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$. When ADON bit in the ADC_CR2 register is set to 1, the current consumption is equal to 0.54 mA.
6. When the ADC is enabled, a current consumption of 0.08 mA must be added.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

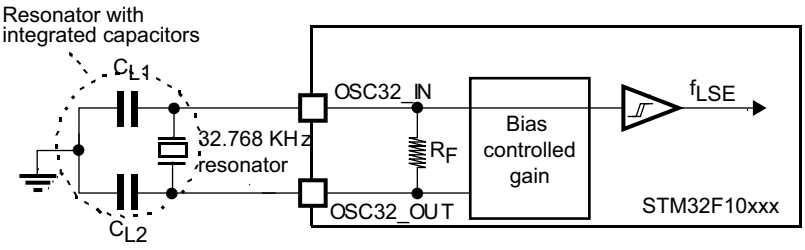
Table 21. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Figure 20. Typical application with a 32.768 kHz crystal



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5.3.7 Internal clock source characteristics

The parameters given in *Table 25* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

High-speed internal (HSI) RC oscillator

Table 25. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1(3)	%
		Factory-calibrated(4)	T_A = –40 to 105 °C	–2	-	2.5	%
			T_A = –10 to 85 °C	–1.5	-	2.2	%
			T_A = 0 to 70 °C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(4)	HSI oscillator power consumption	-		-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 85 °C unless otherwise specified.

Figure 26. Synchronous multiplexed PSRAM write timings

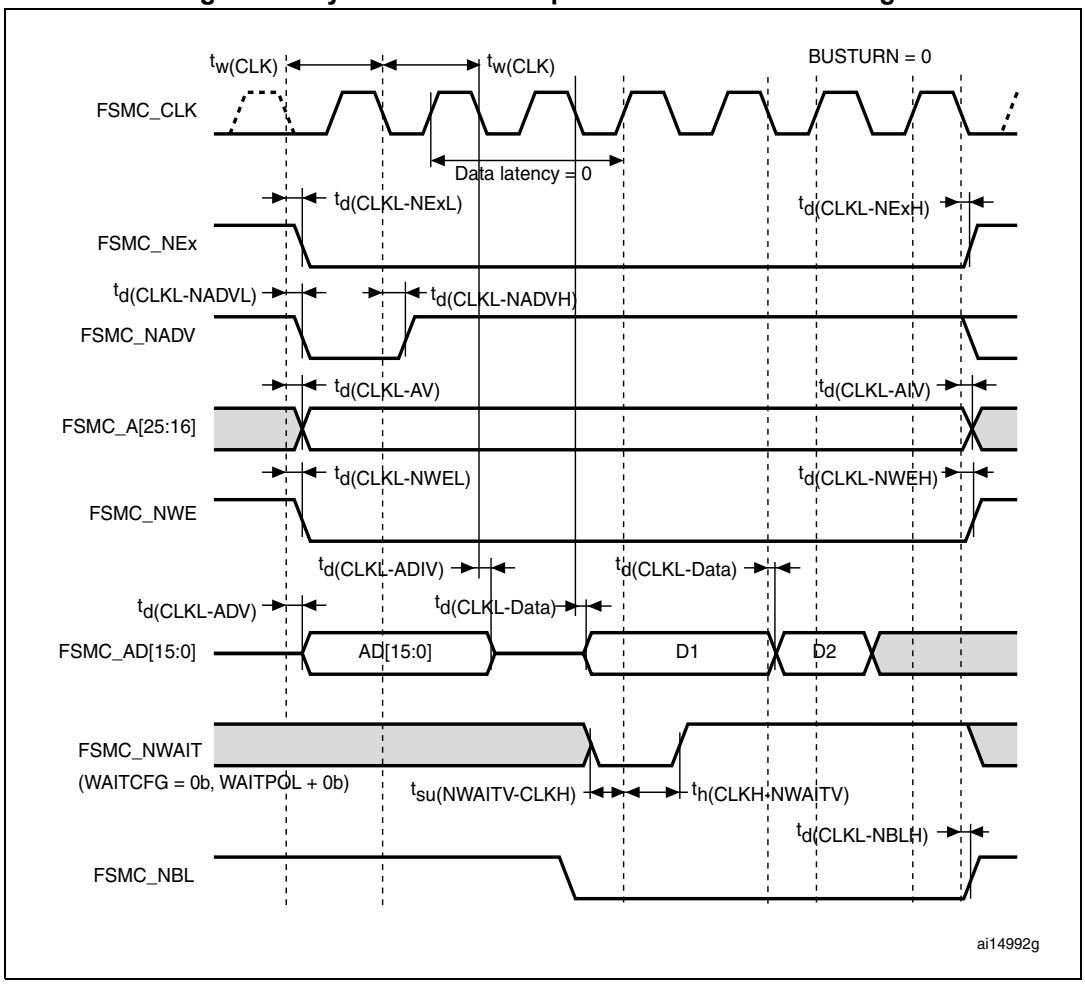


Table 38. Synchronous non-multiplexed PSRAM write timings(1)(2) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.

PC Card/CompactFlash controller waveforms and timings

Figure 29 through *Figure 34* represent synchronous waveforms and *Table 39* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 41*. They are based on the EMS levels and classes defined in application note AN1709.

Table 41. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK}= 36 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 36 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under the conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 46. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage	-	–0.3		0.28*(V_{DD}-2 V)+0.8 V	V
	IO FT(1) input low level voltage		–0.3		0.32*(V_{DD}-2V)+0.75 V	V
V_{IH}	Standard IO input high level voltage		0.41*(V_{DD}-2 V)+1.3 V		V_{DD}+0.3	V
	IO FT(1) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}-2 V)+1 V		5.5	V
		V_{DD} ≤ 2 V			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(2)	-	200		-	mV
	IO FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)		-	mV
I_{lkg}	Input leakage current (4)	V_{SS} ≤ V_{IN} ≤ V_{DD} Standard I/Os	-		±1	µA
		V_{IN} = 5 V I/O FT	-		3	
R_{PU}	Weak pull-up equivalent resistor(5)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	V_{IN} = V_{DD}	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than maximum value if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

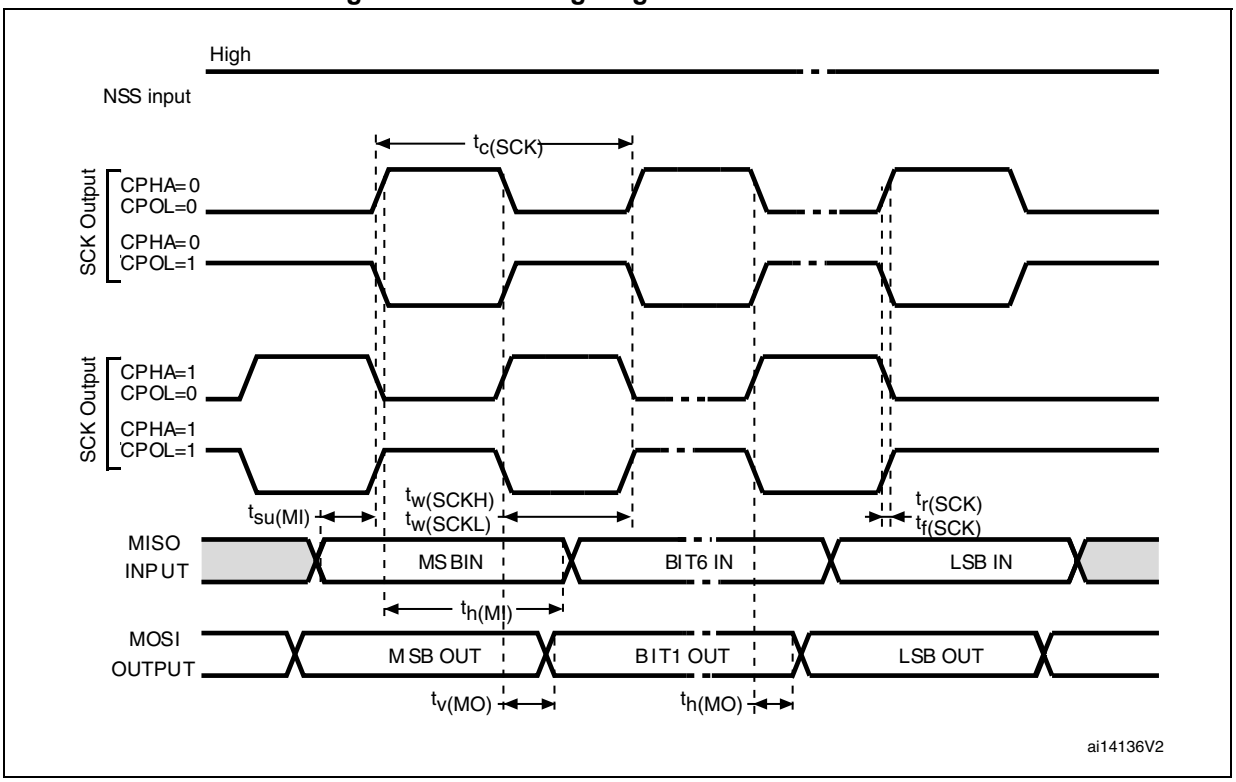
All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 39* and *Figure 40* for standard I/Os, and in *Figure 41* and *Figure 42* for 5 V tolerant I/Os.

Table 54. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$ (1)		Slave mode	4	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$ (1)(1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)(1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2	-	

1. Guaranteed by characterization results not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 48. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.18 12-bit ADC characteristics

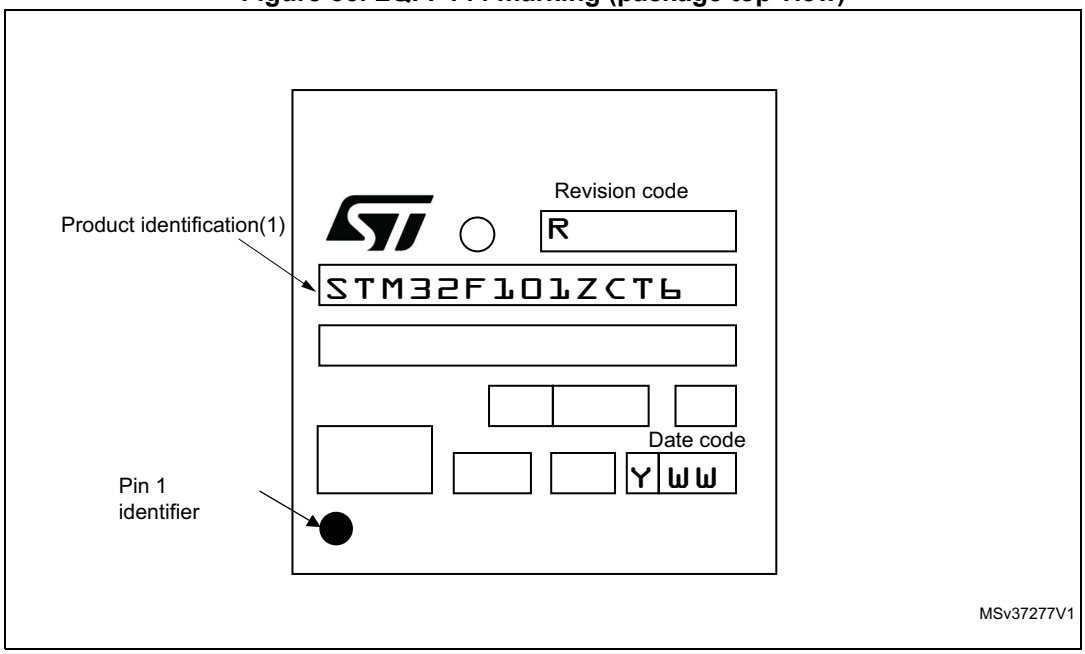
Unless otherwise specified, the parameters given in *Table 55* are valuesderived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 10*.

Note: It is recommended to perform a calibration after each power-up.

Device marking for LQFP144

The following figure gives an example of topside marking and pin 1 position identifier location.

Figure 56. LQFP144 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.