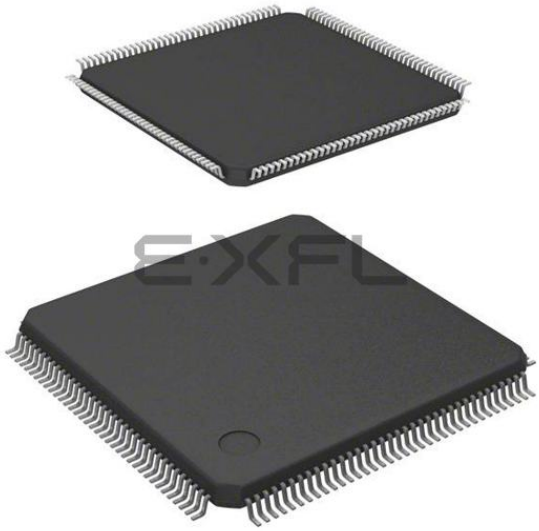

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101zdt6

Contents

List of tables

2 Description

The STM32F101xC, STM32F101xD and STM32F101xE access line family incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory up to 512 Kbytes and SRAM up to 48 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer one 12-bit ADC, four general-purpose 16-bit timers, as well as standard and advanced communication interfaces: up to two I^2Cs, three SPIs and five USARTs.

The STM32F101xx high-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F101xx high-density access line microcontroller family suitable for a wide range of applications such as medical and handheld equipment, PC peripherals and gaming, GPS platforms, industrial applications, PLC, printers, scanners alarm systems and video intercom.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.18 I²C bus

Up to two I²C bus interfaces can operate in multi-master and slave modes. They support standard and fast modes.
They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.19 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F101xC, STM32F101xD and STM32F101xE access line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The five interfaces are able to communicate at speeds of up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.20 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.3.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
62	-	-	V_{DD_7}	S	-	V_{DD_7}	-	-
63	-	41	PE10	I/O	FT	PE10	FSMC_D7	-
64	-	42	PE11	I/O	FT	PE11	FSMC_D8	-
65	-	43	PE12	I/O	FT	PE12	FSMC_D9	-
66	-	44	PE13	I/O	FT	PE13	FSMC_D10	-
67	-	45	PE14	I/O	FT	PE14	FSMC_D11	-
68	-	46	PE15	I/O	FT	PE15	FSMC_D12	-
69	29	47	PB10	I/O	FT	PB10	I2C2_SCL/ USART3_TX(8)	TIM2_CH3
70	30	48	PB11	I/O	FT	PB11	I2C2_SDA/ USART3_RX(8)	TIM2_CH4
71	31	49	V_{SS_1}	S	-	V_{SS_1}	-	-
72	32	50	V_{DD_1}	S	-	V_{DD_1}	-	-
73	33	51	PB12	I/O	FT	PB12	SPI2_NSS(8)/ I2C2_SMBA USART3_CK(8)	-
74	34	52	PB13	I/O	FT	PB13	SPI2_SCK(8)/ USART3_CTS(8)	-
75	35	53	PB14	I/O	FT	PB14	SPI2_MISO(8)/ USART3_RTS(8)	-
76	36	54	PB15	I/O	FT	PB15	SPI2_MOSI(8)	-
77	-	55	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
78	-	56	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
79	-	57	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
80	-	58	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
81	-	59	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
82	-	60	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
83	-	-	V_{SS_8}	S	-	V_{SS_8}	-	-
84	-	-	V_{DD_8}	S	-	V_{DD_8}	-	-
85	-	61	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
86	-	62	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
87	-	-	PG2	I/O	FT	PG2	FSMC_A12	-

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP144	LQFP64	LQFP100					Default	Remap
116	54	83	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX	-
117	-	84	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
118	-	85	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
119	-	86	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
120	-	-	V_{SS_10}	S	-	V_{SS_10}	-	-
121	-	-	V_{DD_10}	S	-	V_{DD_10}	-	-
122	-	87	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
123	-	88	PD7	I/O	FT	PD7	FSMC_NE1/ FSMC_NCE2	USART2_CK
124	-	-	PG9	I/O	FT	PG9	FSMC_NE2/ FSMC_NCE3	-
125	-	-	PG10	I/O	FT	PG10	FSMC_NE3/ FSMC_NCE4_1	-
126	-	-	PG11	I/O	FT	PG11	FSMC_NCE4_2	-
127	-	-	PG12	I/O	FT	PG12	FSMC_NE4	-
128	-	-	PG13	I/O	FT	PG13	FSMC_A24	-
129	-	-	PG14	I/O	FT	PG14	FSMC_A25	-
130	-	-	V_{SS_11}	S	-	V_{SS_11}	-	-
131	-	-	V_{DD_11}	S	-	V_{DD_11}	-	-
132	-	-	PG15	I/O	FT	PG15	-	-
133	55	89	PB3	I/O	FT	JTDO	SPI3_SCK	TIM2_CH2 /PB3 TRACESWO SPI1_SCK
134	56	90	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 / TIM3_CH1 SPI1_MISO
135	57	91	PB5	I/O		PB5	I2C1_SMBA/ SPI3_MOSI	TIM3_CH2 / SPI1_MOSI
136	58	92	PB6	I/O	FT	PB6	I2C1_SCL/ TIM4_CH1(8)	USART1_TX
137	59	93	PB7	I/O	FT	PB7	I2C1_SDA/FSMC_NADV TIM4_CH2(8)	USART1_RX
138	60	94	BOOT0	I	-	BOOT0	-	-
139	61	95	PB8	I/O	FT	PB8	TIM4_CH3 (8)	I2C1_SCL

Figure 11. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

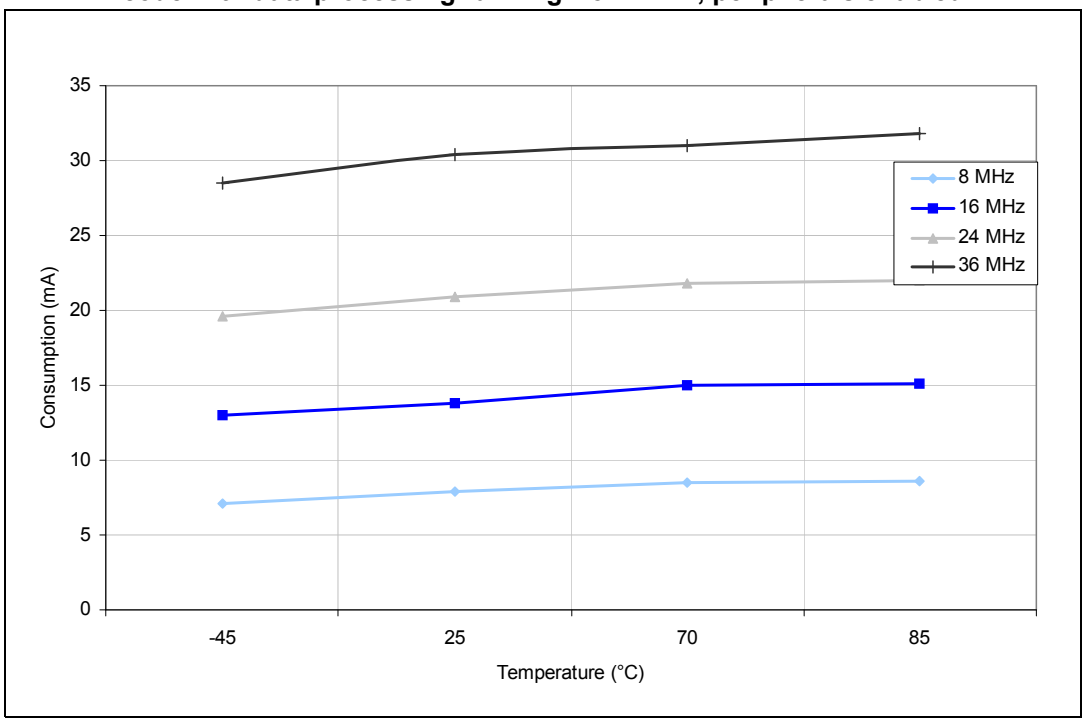
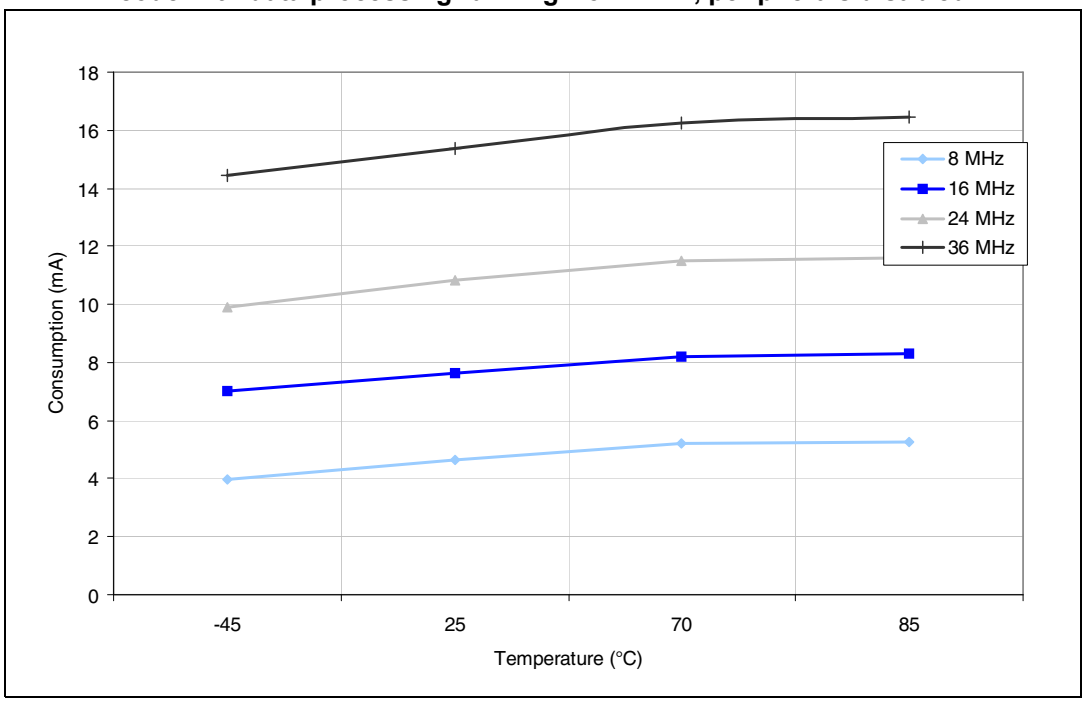


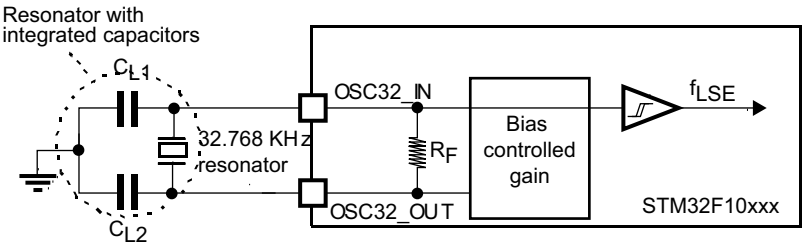
Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled



Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Figure 20. Typical application with a 32.768 kHz crystal



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5.3.7 Internal clock source characteristics

The parameters given in *Table 25* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

High-speed internal (HSI) RC oscillator

Table 25. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1(3)	%
		Factory-calibrated(4)	T_A = –40 to 105 °C	–2	-	2.5	%
			T_A = –10 to 85 °C	–1.5	-	2.2	%
			T_A = 0 to 70 °C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(4)	HSI oscillator power consumption	-		-	80	100	µA

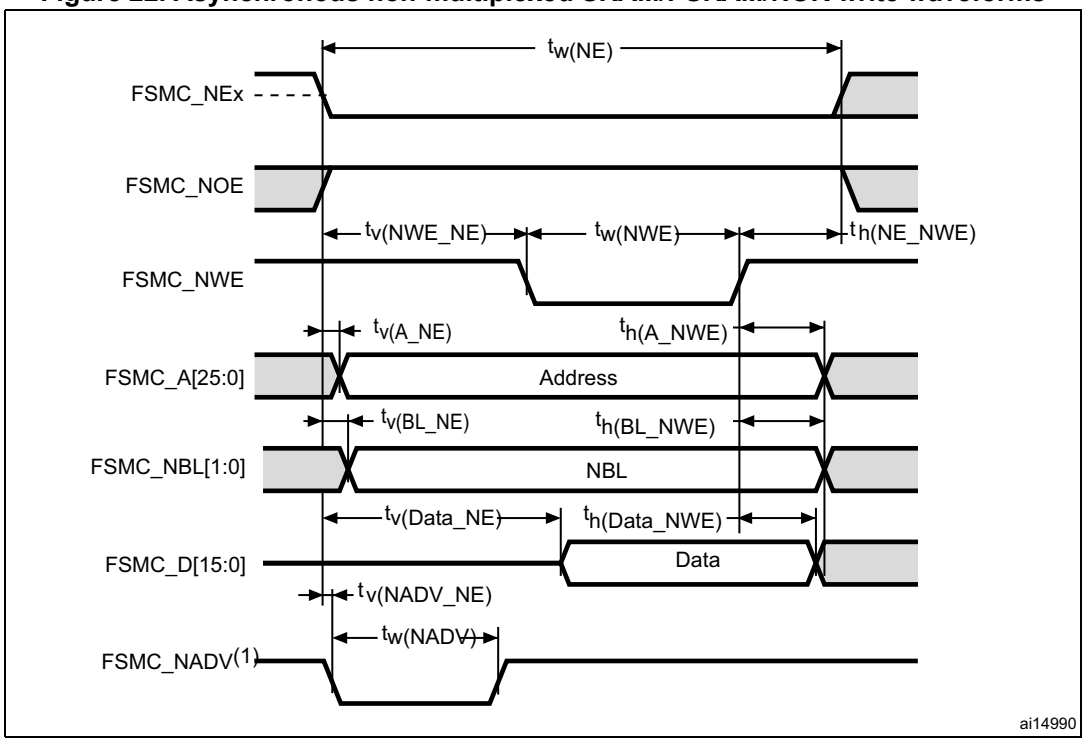
1. V_{DD} = 3.3 V, T_A = –40 to 85 °C unless otherwise specified.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	5	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	t_{HCLK} + 1.5	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 32. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3t_{HCLK} - 1$	$3t_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	$t_{HCLK} - 0.5$	$t_{HCLK} + 1.5$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$t_{HCLK} - 0.5$	$t_{HCLK} + 1.5$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	t_{HCLK}	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	7.5	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	t_{HCLK}	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$t_{HCLK} - 0.5$	-	ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid	-	$t_{HCLK} + 7$	ns

Table 36. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	55.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_Nex low (x = 0...2)	-	2	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	2	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	12	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	3	-	ns
$t_{d(CLKL-Data)}$	FSMC_A/D[15:0] valid after FSMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns

1. C_L = 15 pF.
2. Guaranteed by characterization results, not tested in production.

Figure 35. NAND controller waveforms for read access

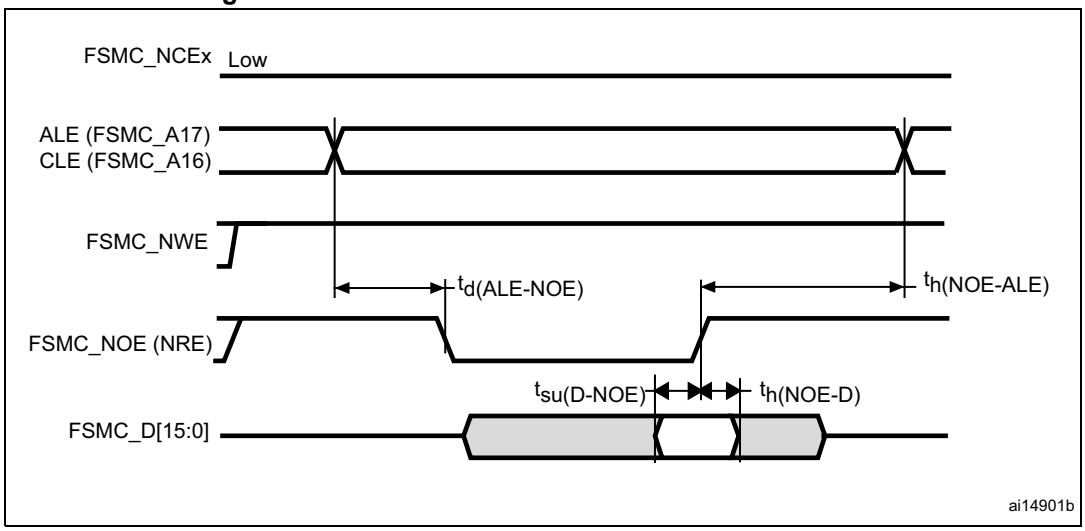


Figure 36. NAND controller waveforms for write access

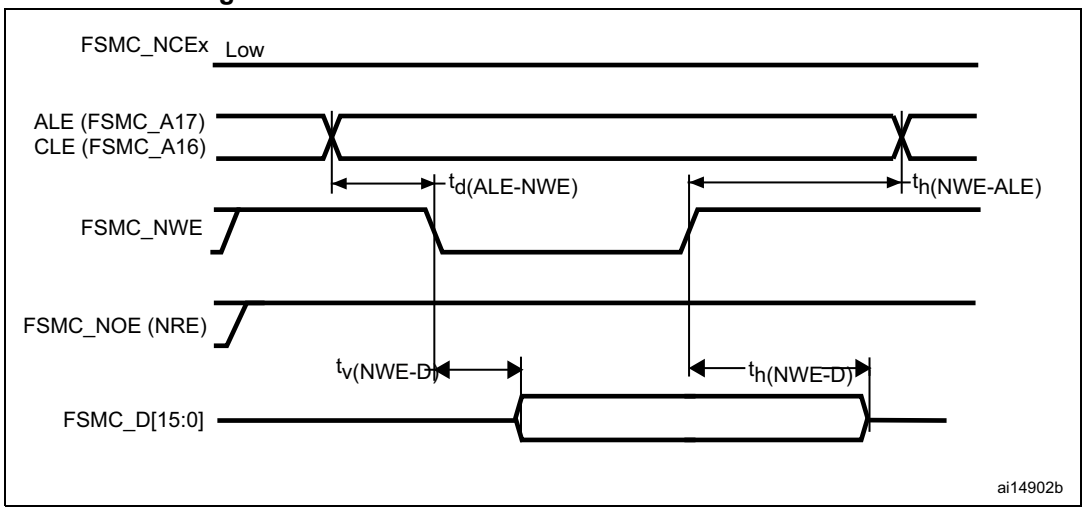
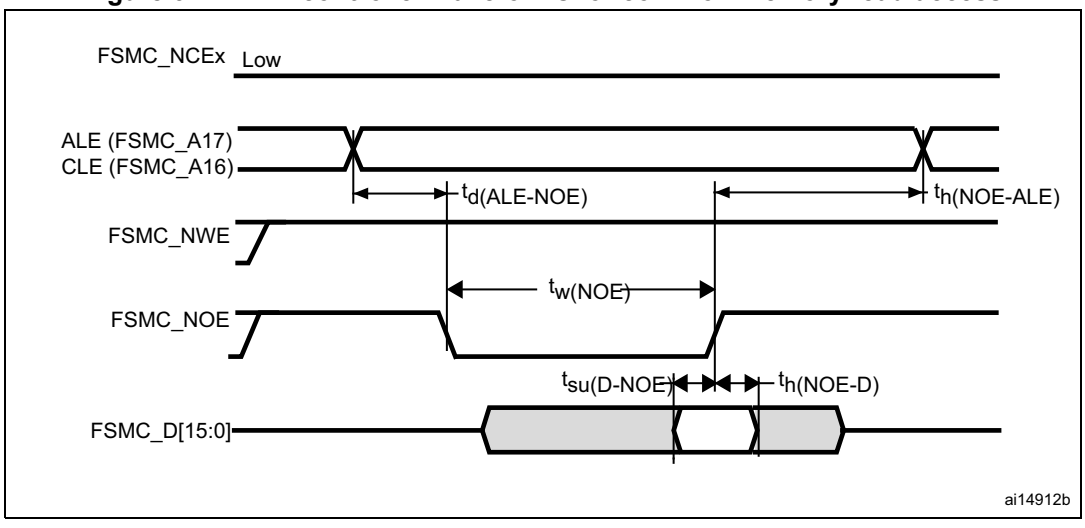


Figure 37. NAND controller waveforms for common memory read access



Output voltage levels

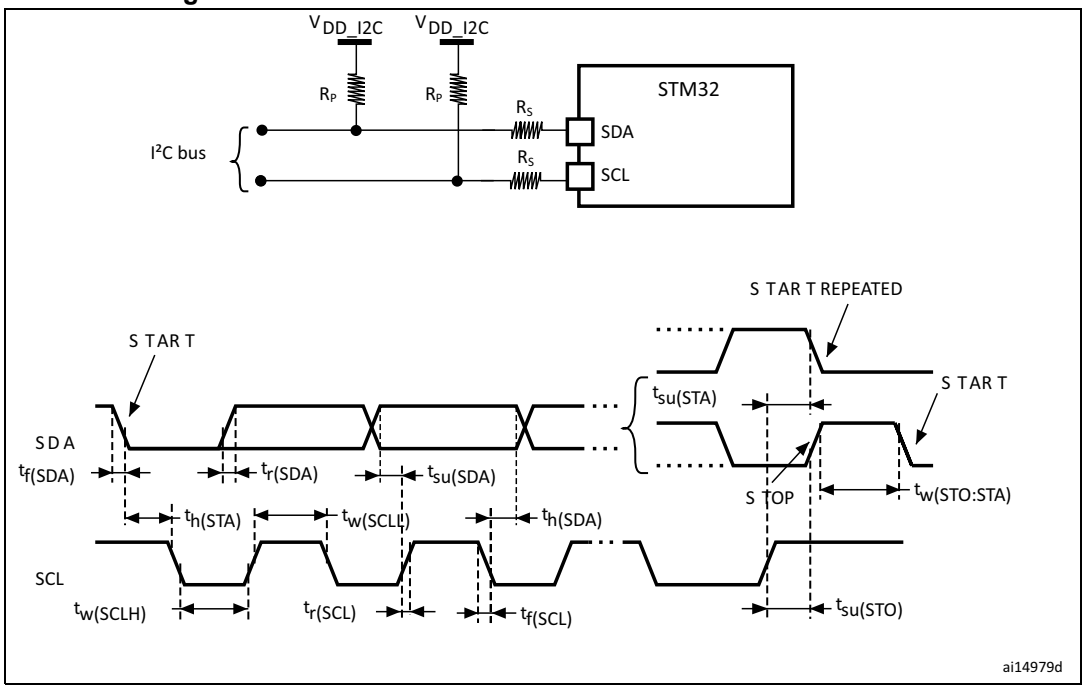
Unless otherwise specified, the parameters given in *Table 47* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 47. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port(2), I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(4) 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(4) 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results, not tested in production.

Figure 45. I²C bus AC waveforms and measurement circuit(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.

Table 52. SCL frequency (f_{PCLK1}= 36 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Table 58. ADC accuracy(1) (2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 28 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. ADC accuracy vs. negative injection current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.
4. Guaranteed by characterization results, not tested in production.

Figure 49. ADC accuracy characteristics

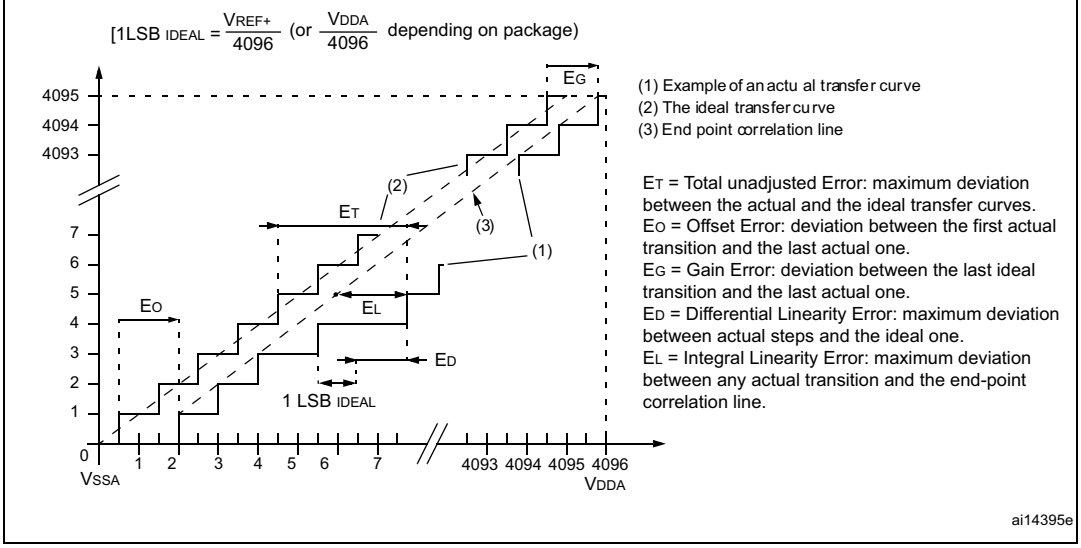
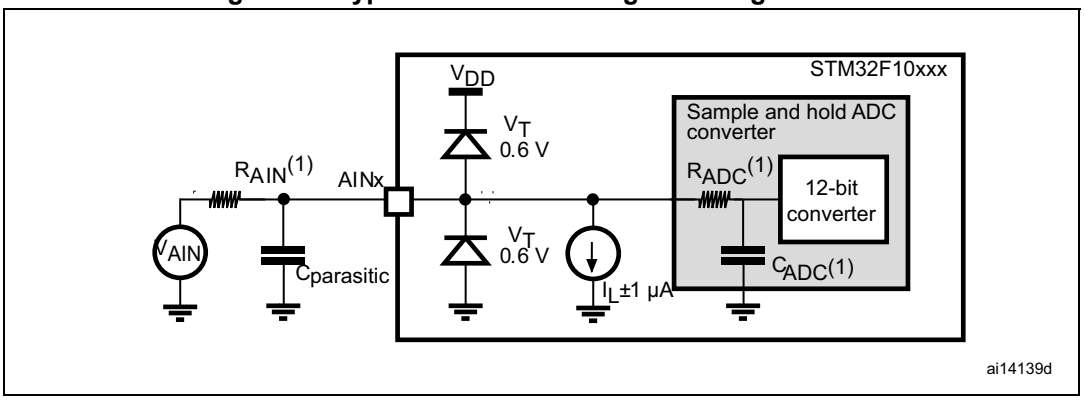


Figure 50. Typical connection diagram using the ADC

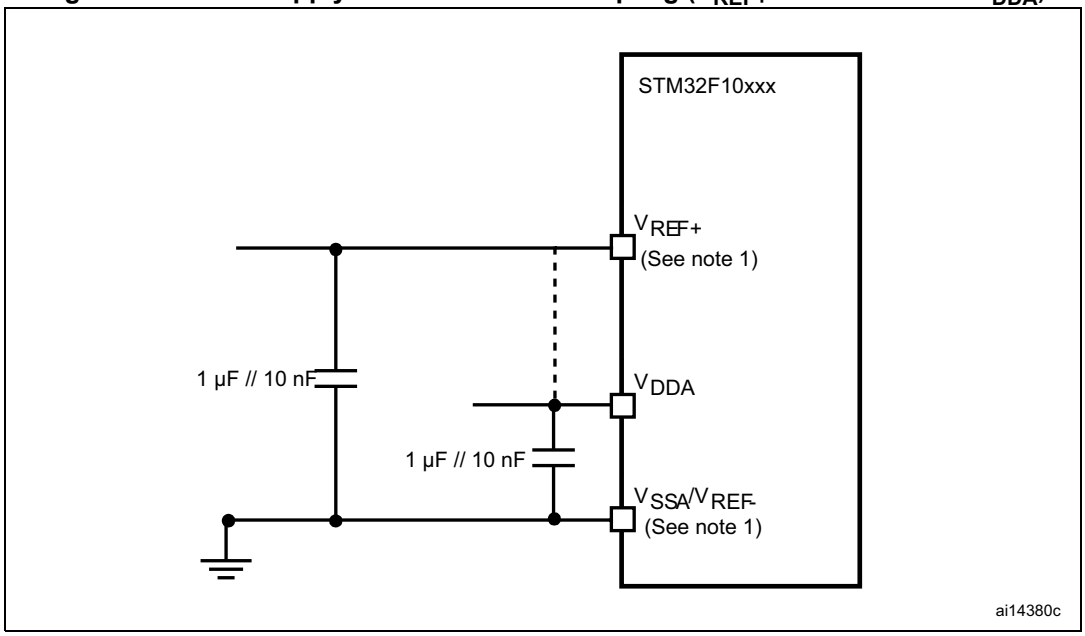


1. Refer to *Table 55* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 51* or *Figure 52*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 51. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



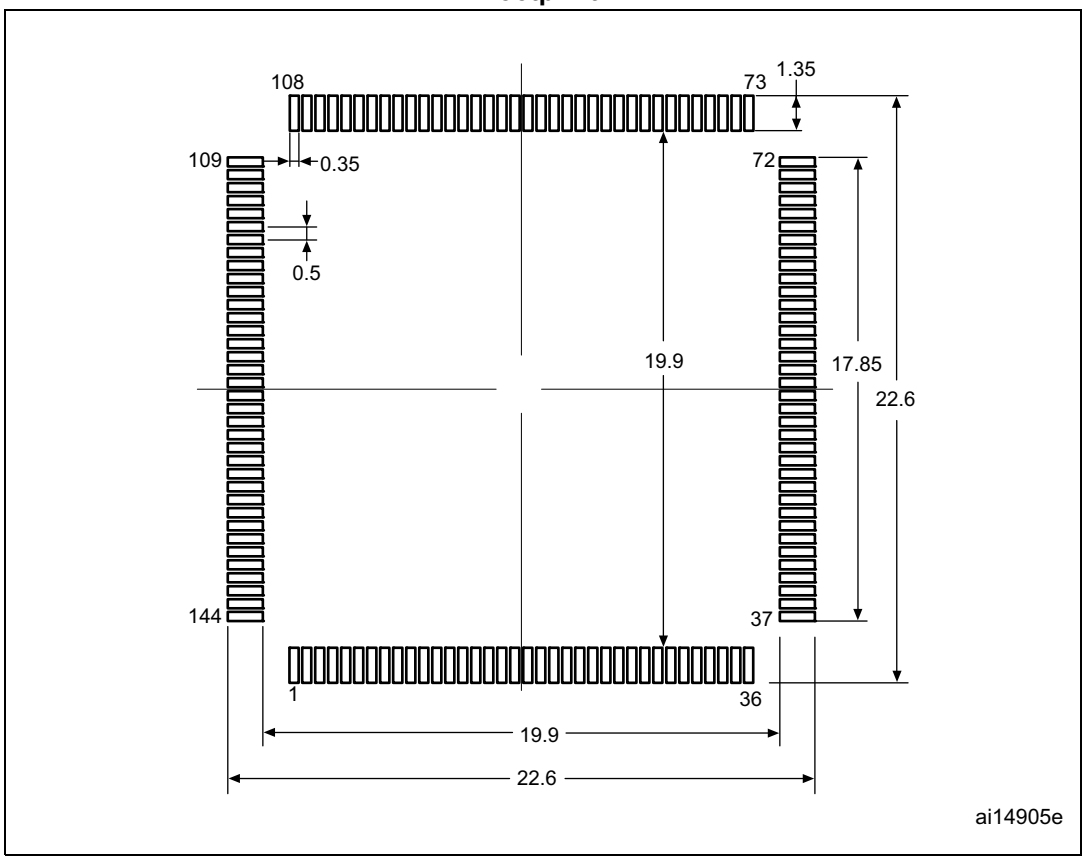
1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Table 61. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.874
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-		0.689	
e	-	0.500	-		0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-		0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

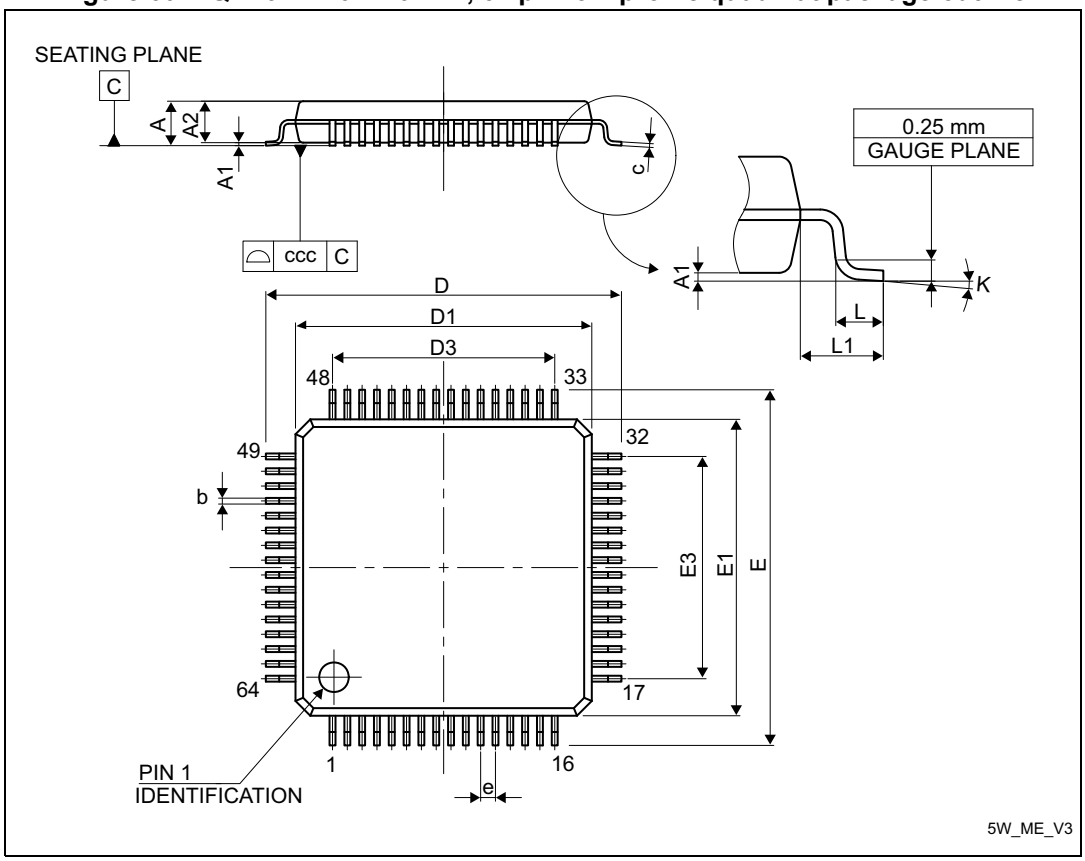
Figure 55. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package footprint



1. Dimensions are expressed in millimeters.

6.3 LQFP64 information

Figure 60. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 63. LQFP64 – 10 x 10 mm, 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-

8 Revision history

Table 66. Document revision history

Date	Revision	Changes
07-Apr-2008	1	Initial release.
22-May-2008	2	Document status promoted from Target Specification to Preliminary Data. *Section 1: Introduction* and *Section 2.2: Full compatibility throughout the family* modified. Small text changes. *Note 1* added in *Table 2: STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts on page 11*. LQPF100/BGA100 column added to *Table 6: FSMC pin definition on page 32*. Values added to *Maximum current consumption on page 42* (see *Table 14*, *Table 15*, *Table 16* and *Table 17*). Values added to *Typical current consumption on page 48* (see *Table 18*, *Table 19* and *Table 20* and see *Figure 11*, *Figure 12*, *Figure 14*, *Figure 15* and *Figure 16*), *Table 19: Typical current consumption in Standby mode* removed. *Figure 55: LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package footprint on page 105* corrected. *Equation 1* corrected. *Section 6.4.2: Evaluating the maximum junction temperature for an application on page 114* added.