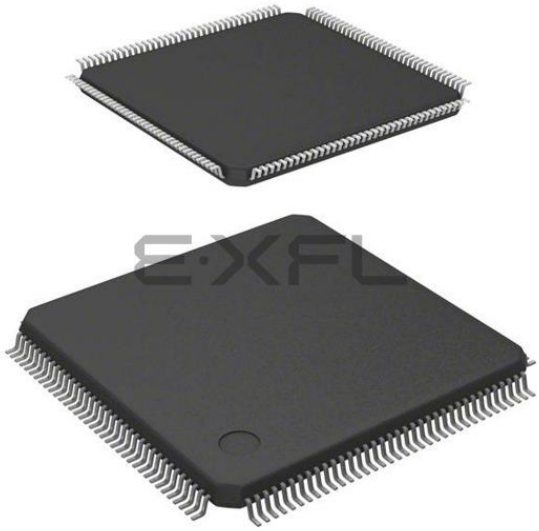


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 36MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT |
| Number of I/O | 112 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101zet6 |

## 2.1 Device overview

The STM32F101xx high-density access line family offers devices in 3 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

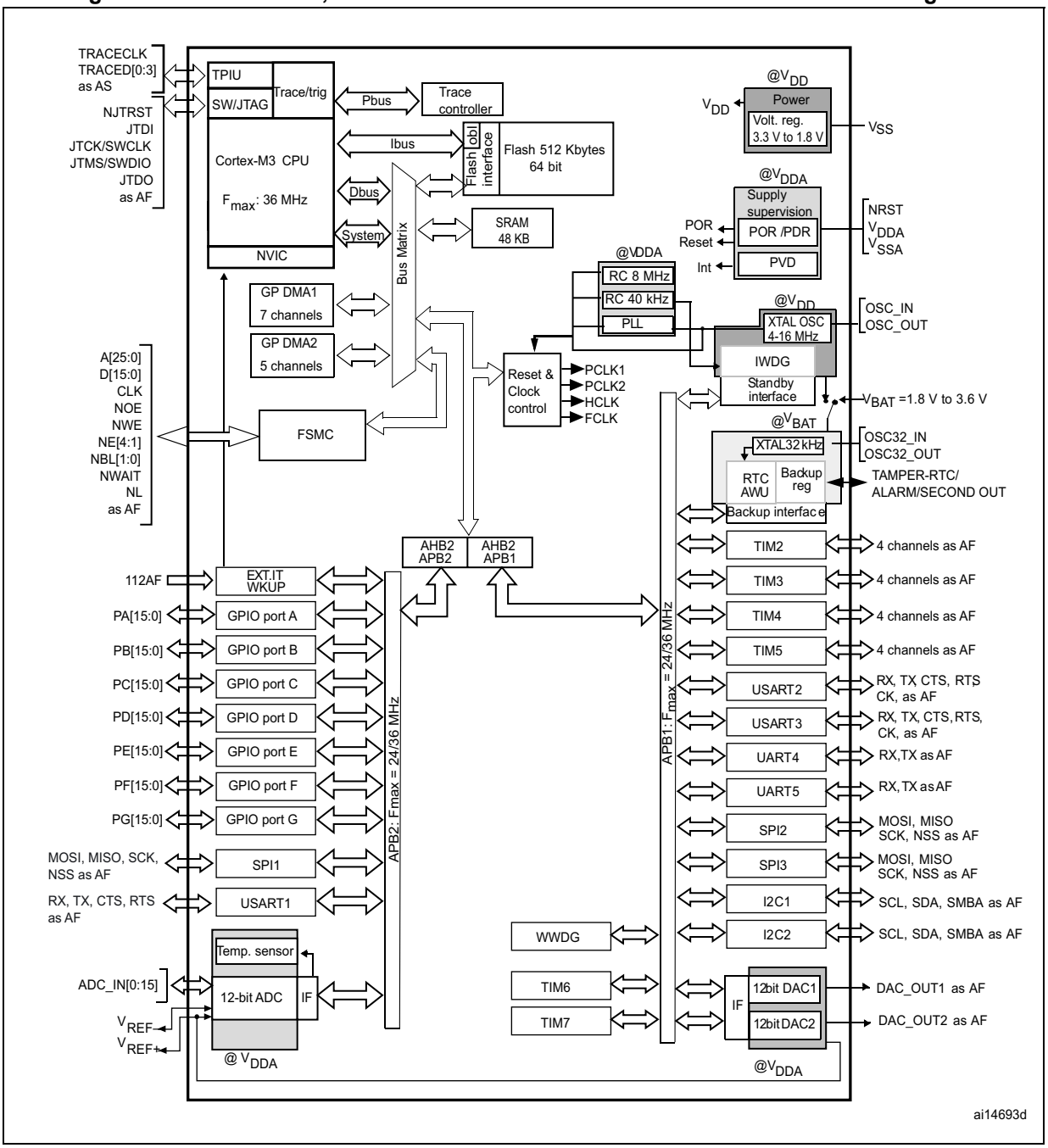
*Figure 1* shows the general block diagram of the device family.

**Table 2. STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts**

| Peripherals | | STM32F101Rx | | | STM32F101Vx | | | STM32F101Zx | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Flash memory in Kbytes | | 256 | 384 | 512 | 256 | 384 | 512 | 256 | 384 | 512 |
| SRAM in Kbytes | | 32 | 48 | | 32 | 48 | | 32 | 48 | |
| FSMC | | No | | | Yes(1) | | | Yes | | |
| Timers | General-purpose | 4 | | | | | | | | |
| | Basic | 2 | | | | | | | | |
| Comm | SPI | 3 | | | | | | | | |
| | $I^2C$ | 2 | | | | | | | | |
| | USART | 5 | | | | | | | | |
| GPIOs | | 51 | | | 80 | | | 112 | | |
| 12-bit ADC<br>Number of channels | | Yes<br>16 | | | Yes<br>16 | | | Yes<br>16 | | |
| 12-bit DAC<br>Number of channels | | 1<br>2 | | | | | | | | |
| CPU frequency | | 36 MHz | | | | | | | | |
| Operating voltage | | 2.0 to 3.6 V | | | | | | | | |
| Operating temperatures | | Ambient temperature: –40 to +85 °C (see *Table 10*)<br>Junction temperature: –40 to +105 °C (see *Table 10*) | | | | | | | | |
| Package | | LQFP64 | | | LQFP100 | | | LQFP144 | | |

1. For the LQFP100 package, only FSMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.

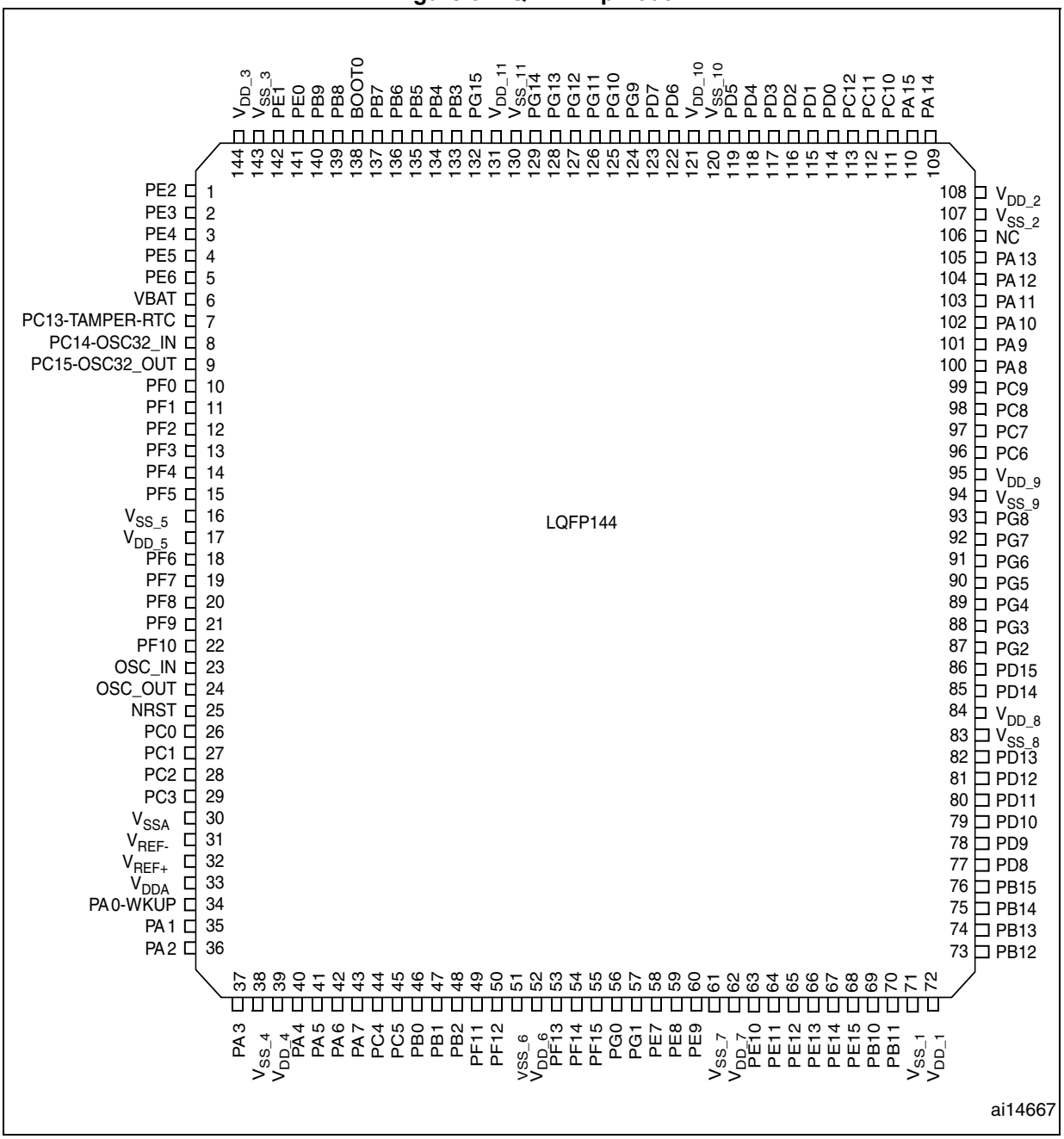
**Figure 1. STM32F101xC, STM32F101xD and STM32F101xE access line block diagram**




1. $T_A$ = –40 °C to +85 °C (junction temperature up to 105 °C).
2. AF = alternate function on I/O port pin.

# 3 Pinouts and pin descriptions

**Figure 3. LQFP144 pinout**




1. The above figure shows the package top view.

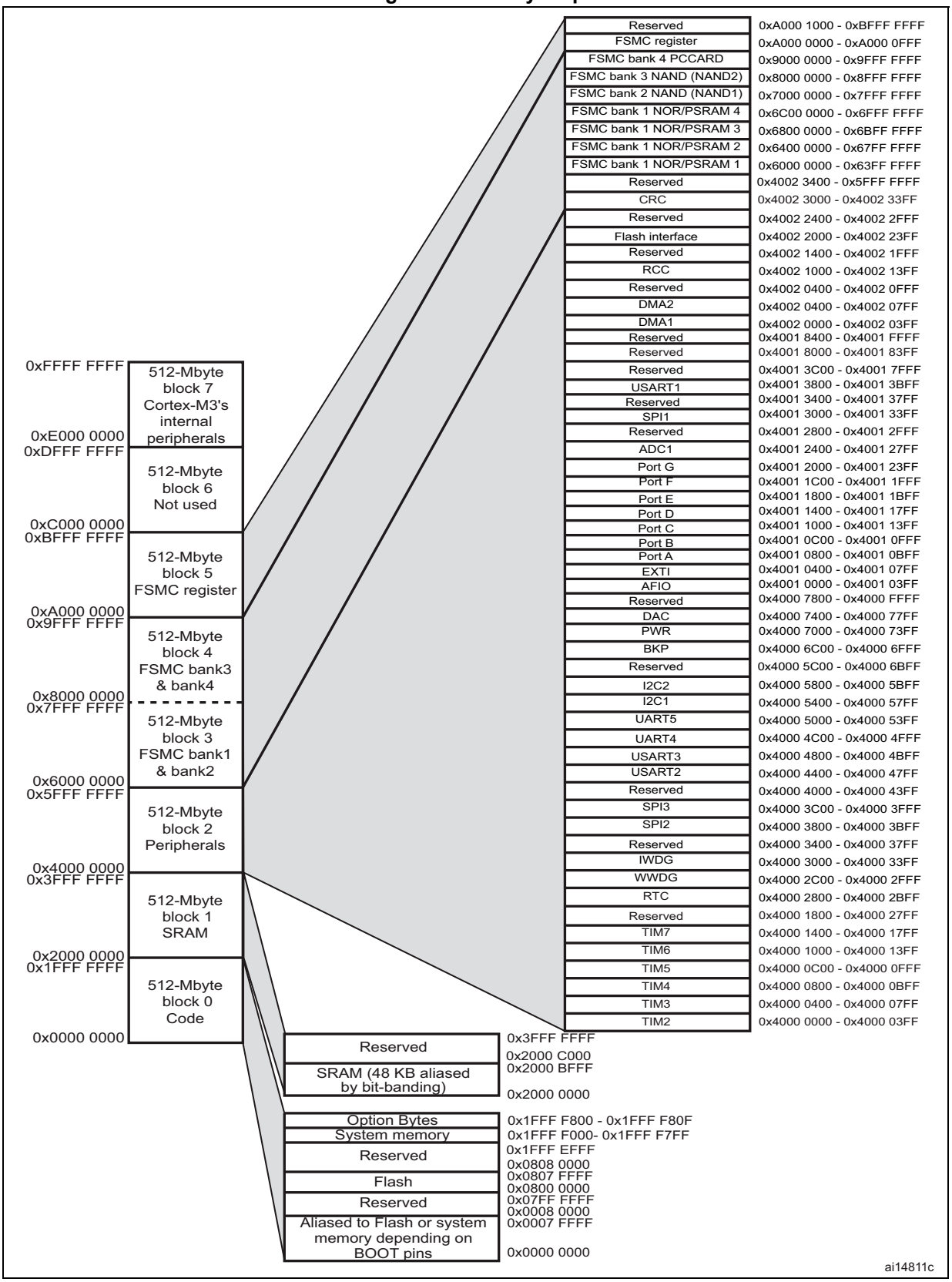
Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

| Pins | | | Pin name | Type(1) | I / O Level(2) | Main function(3) (after reset) | Alternate functions(4) | |
|---|---|---|---|---|---|---|---|---|
| LQFP144 | LQFP64 | LQFP100 | | | | | Default | Remap |
| 37 | 17 | 26 | PA3 | I/O | - | PA3 | USART2_RX(8)/ TIM5_CH4 / ADC_IN3/ TIM2_CH4(8) | - |
| 38 | 18 | 27 | $V_{SS\_4}$ | S | - | $V_{SS\_4}$ | - | - |
| 39 | 19 | 28 | $V_{DD\_4}$ | S | - | $V_{DD\_4}$ | - | - |
| 40 | 20 | 29 | PA4 | I/O | - | PA4 | SPI1_NSS/ DAC_OUT1 ADC_IN4 / USART2_CK(8) | - |
| 41 | 21 | 30 | PA5 | I/O | - | PA5 | SPI1_SCK/ DAC_OUT2/ADC_IN5 | - |
| 42 | 22 | 31 | PA6 | I/O | - | PA6 | SPI1_MISO / ADC_IN6 / TIM3_CH1(8) | - |
| 43 | 23 | 32 | PA7 | I/O | - | PA7 | SPI1_MOSI / ADC_IN7/ TIM3_CH2(8) | - |
| 44 | 24 | 33 | PC4 | I/O | - | PC4 | ADC_IN14 | - |
| 45 | 25 | 34 | PC5 | I/O | - | PC5 | ADC_IN15 | - |
| 46 | 26 | 35 | PB0 | I/O | - | PB0 | ADC_IN8 / TIM3_CH3(8) | - |
| 47 | 27 | 36 | PB1 | I/O | - | PB1 | ADC_IN9/TIM3_CH4(8) | - |
| 48 | 28 | 37 | PB2 | I/O | FT | PB2/BOOT1 | - | - |
| 49 | - | - | PF11 | I/O | FT | PF11 | FSMC_NIOS16 | - |
| 50 | - | - | PF12 | I/O | FT | PF12 | FSMC_A6 | - |
| 51 | - | - | $V_{SS\_6}$ | S | - | $V_{SS\_6}$ | - | - |
| 52 | - | - | $V_{DD\_6}$ | S | - | $V_{DD\_6}$ | - | - |
| 53 | - | - | PF13 | I/O | FT | PF13 | FSMC_A7 | - |
| 54 | - | - | PF14 | I/O | FT | PF14 | FSMC_A8 | - |
| 55 | - | - | PF15 | I/O | FT | PF15 | FSMC_A9 | - |
| 56 | - | - | PG0 | I/O | FT | PG0 | FSMC_A10 | - |
| 57 | - | - | PG1 | I/O | FT | PG1 | FSMC_A11 | - |
| 58 | - | 38 | PE7 | I/O | FT | PE7 | FSMC_D4 | - |
| 59 | - | 39 | PE8 | I/O | FT | PE8 | FSMC_D5 | - |
| 60 | - | 40 | PE9 | I/O | FT | PE9 | FSMC_D6 | - |
| 61 | - | - | $V_{SS\_7}$ | S | - | $V_{SS\_7}$ | - | - |

Table 5. STM32F101xC/STM32F101xD/STM32F101xE pin definitions (continued)

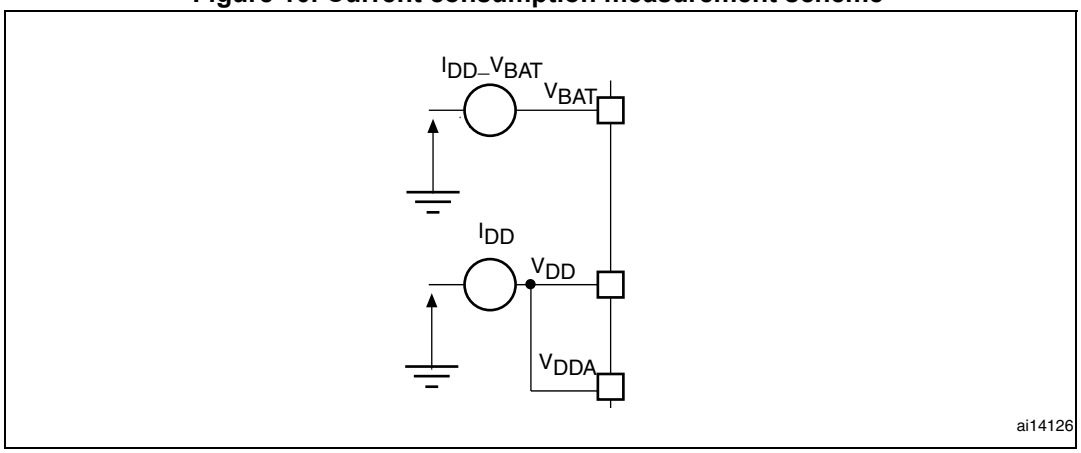
| Pins | | | Pin name | Type(1) | I / O Level(2) | Main function(3) (after reset) | Alternate functions(4) | |
|---|---|---|---|---|---|---|---|---|
| LQFP144 | LQFP64 | LQFP100 | | | | | Default | Remap |
| 88 | - | - | PG3 | I/O | FT | PG3 | FSMC_A13 | - |
| 89 | - | - | PG4 | I/O | FT | PG4 | FSMC_A14 | - |
| 90 | - | - | PG5 | I/O | FT | PG5 | FSMC_A15 | - |
| 91 | - | - | PG6 | I/O | FT | PG6 | FSMC_INT2 | - |
| 92 | - | - | PG7 | I/O | FT | PG7 | FSMC_INT3 | - |
| 93 | - | - | PG8 | I/O | FT | PG8 | - | - |
| 94 | - | - | $V_{SS\_9}$ | S | - | $V_{SS\_9}$ | - | - |
| 95 | - | - | $V_{DD\_9}$ | S | - | $V_{DD\_9}$ | - | - |
| 96 | 37 | 63 | PC6 | I/O | FT | PC6 | - | TIM3_CH1 |
| 97 | 38 | 64 | PC7 | I/O | FT | PC7 | - | TIM3_CH2 |
| 98 | 39 | 65 | PC8 | I/O | FT | PC8 | - | TIM3_CH3 |
| 99 | 40 | 66 | PC9 | I/O | FT | PC9 | - | TIM3_CH4 |
| 100 | 41 | 67 | PA8 | I/O | FT | PA8 | USART1_CK/ MCO | - |
| 101 | 42 | 68 | PA9 | I/O | FT | PA9 | USART1_TX(8) | - |
| 102 | 43 | 69 | PA10 | I/O | FT | PA10 | USART1_RX(8) | - |
| 103 | 44 | 70 | PA11 | I/O | FT | PA11 | USART1_CTS | - |
| 104 | 45 | 71 | PA12 | I/O | FT | PA12 | USART1_RTS | - |
| 105 | 46 | 72 | PA13 | I/O | FT | JTMS-SWDIO | - | PA13 |
| 106 | - | 73 | Not connected | | | | | |
| 107 | 47 | 74 | $V_{SS\_2}$ | S | - | $V_{SS\_2}$ | - | - |
| 108 | 48 | 75 | $V_{DD\_2}$ | S | - | $V_{DD\_2}$ | - | - |
| 109 | 49 | 76 | PA14 | I/O | FT | JTCK-SWCLK | - | PA14 |
| 110 | 50 | 77 | PA15 | I/O | FT | JTDI | SPI3_NSS | TIM2_CH1_ETR/ PA15 /SPI1_NSS |
| 111 | 51 | 78 | PC10 | I/O | FT | PC10 | UART4_TX | USART3_TX |
| 112 | 52 | 79 | PC11 | I/O | FT | PC11 | UART4_RX | USART3_RX |
| 113 | 53 | 80 | PC12 | I/O | FT | PC12 | UART5_TX | USART3_CK |
| 114 | - | 81 | PD0 | I/O | FT | OSC_IN(8) | FSMC_D2(9) | - |
| 115 | - | 82 | PD1 | I/O | FT | OSC_OUT(8) | FSMC_D3(9) | - |

**Figure 6. Memory map**



### 5.1.7 Current consumption measurement

**Figure 10. Current consumption measurement scheme**




## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 7: Voltage characteristics*, *Table 8: Current characteristics*, and *Table 9: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 7. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD} - V_{SS}$ | External main supply voltage (including $V_{DDA}$ and $V_{DD}$)(1) | –0.3 | 4.0 | V |
| $V_{IN}$(2) | Input voltage on five volt tolerant pin | $V_{SS} - 0.3$ | $V_{DD} + 4.0$ | |
| | Input voltage on any other pin | $V_{SS} - 0.3$ | 4.0 | |
| $\lvert\Delta V_{DDx}\rvert$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{SSX} - V_{SS}\rvert$ | Variations between all the different ground pins | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 5.3.12: Absolute maximum ratings (electrical sensitivity)* | | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum must always be respected. Refer to *Table 8: Current characteristics* for the maximum allowed injected current values.

**Table 8. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $\Sigma I_{VDD}$ | Total current into $V_{DD}/V_{DDA}$ power lines (source)(1) | 150 | mA |
| $\Sigma I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink)(1) | 150 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | – 25 | |
| $I_{INJ(PIN)}$(2) | Injected current on five volt tolerant pins(3) | -5/+0 | |
| | Injected current on any other pin(4) | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(5) | ± 25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See note 3 below *Table 58 on page 98*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 7: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 7: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 9. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

**Figure 11. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled**

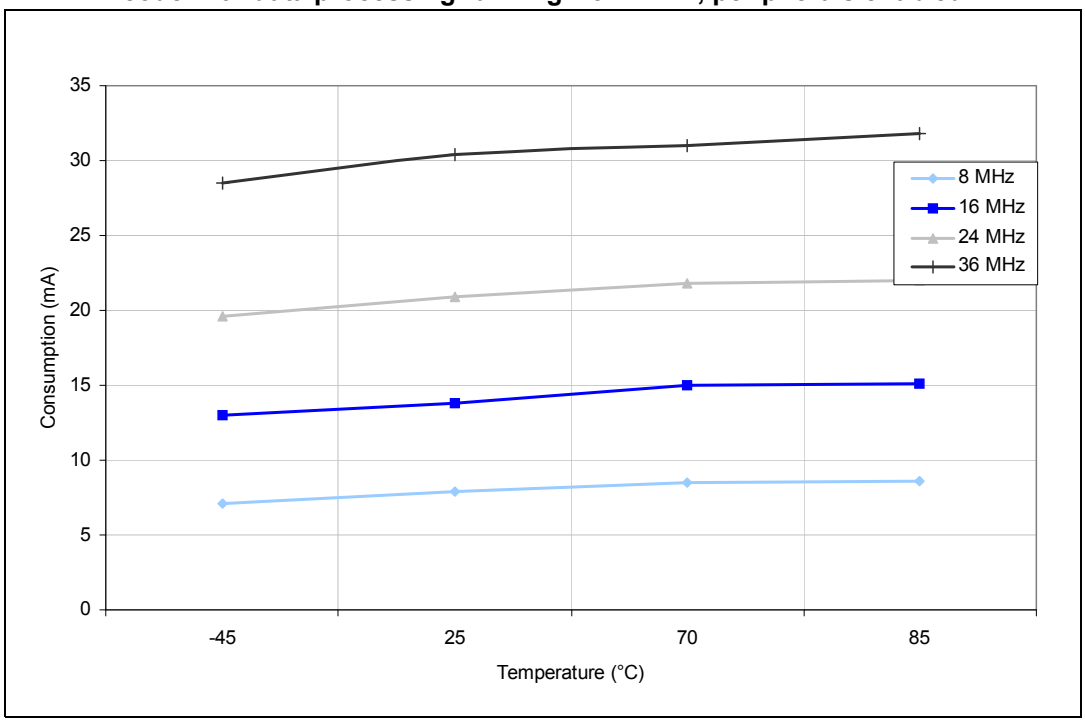



**Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled**

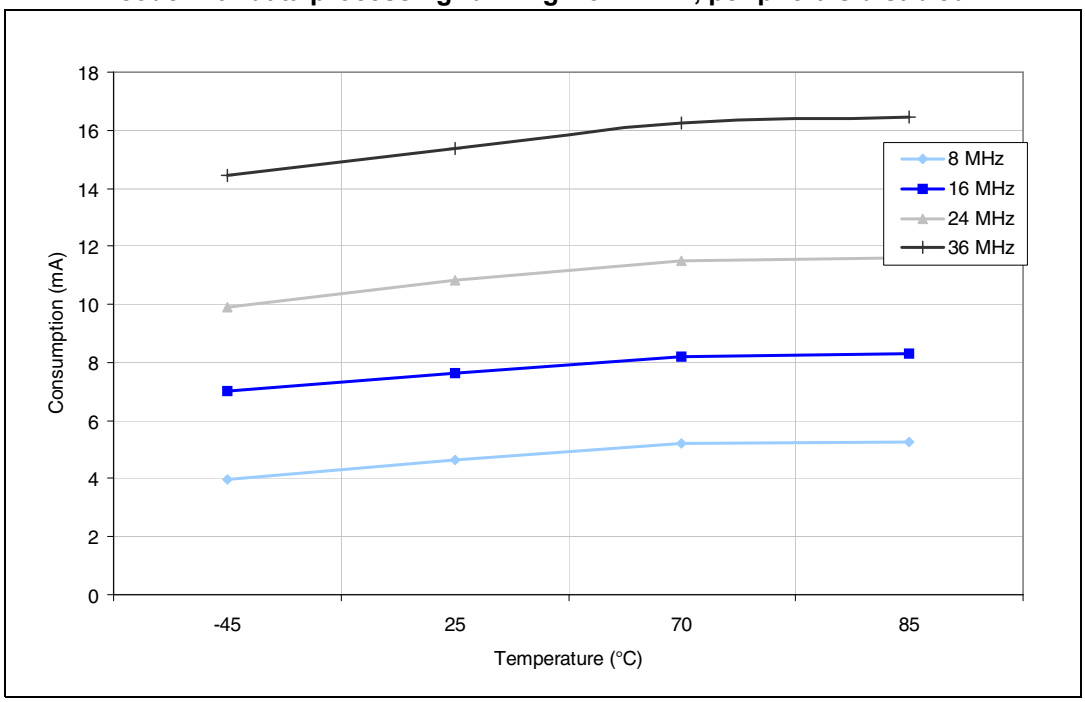


**Figure 13. Typical current consumption on $V_{BAT}$ with RTC on vs. temperature at different $V_{BAT}$ values**

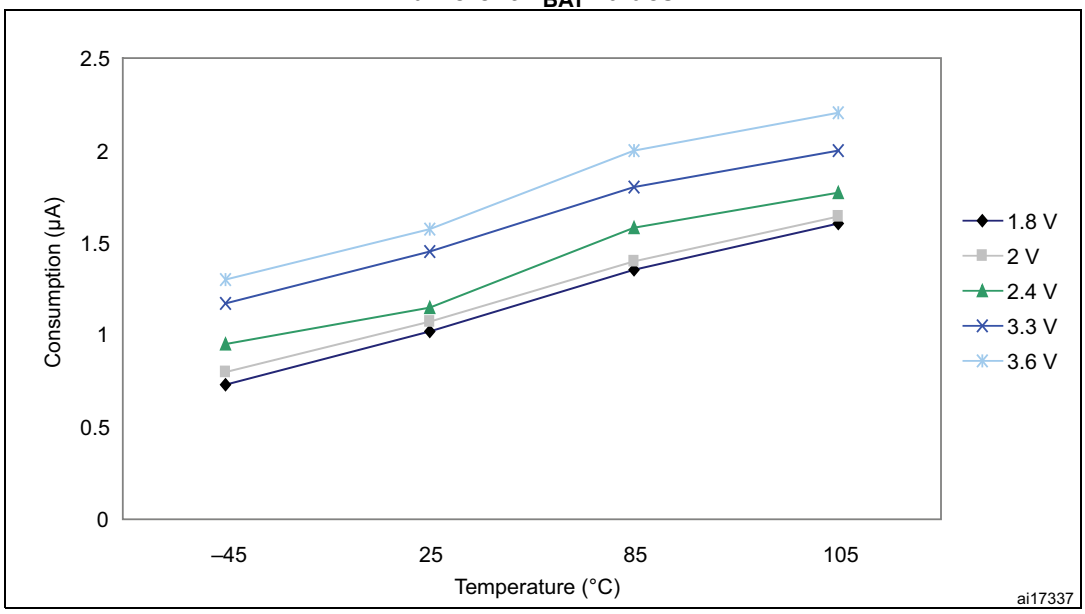



**Figure 14. Typical current consumption in Stop mode with regulator in run mode versus temperature at different $V_{DD}$ values**

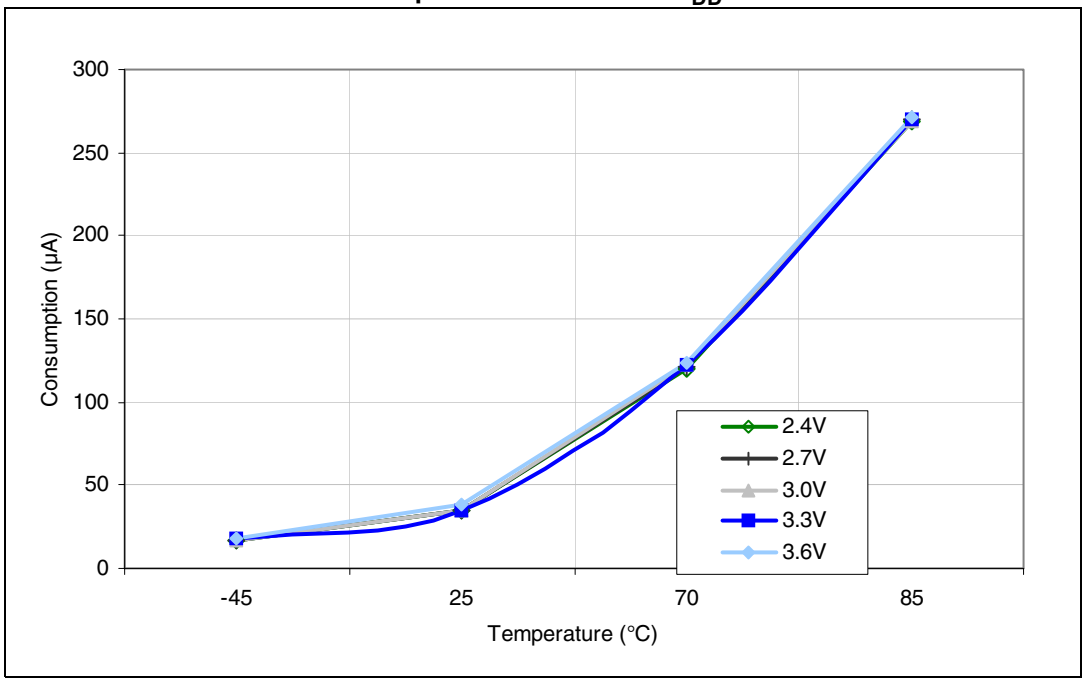


**Table 19. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ(1) | Typ(1) | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled(2) | All peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(3) | 36 MHz | 15.1 | 3.6 | mA |
| | | | 24 MHz | 10.4 | 2.6 | |
| | | | 16 MHz | 7.2 | 2 | |
| | | | 8 MHz | 3.9 | 1.3 | |
| | | | 4 MHz | 2.6 | 1.2 | |
| | | | 2 MHz | 1.85 | 1.15 | |
| | | | 1 MHz | 1.5 | 1.1 | |
| | | | 500 kHz | 1.3 | 1.05 | |
| | | | 125 kHz | 1.2 | 1.05 | |
| | | Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency | 36 MHz | 14.5 | 3 | |
| | | | 24 MHz | 9.8 | 2 | |
| | | | 16 MHz | 6.6 | 1.4 | |
| | | | 8 MHz | 3.3 | 0.7 | |
| | | | 4 MHz | 2 | 0.6 | |
| | | | 2 MHz | 1.25 | 0.55 | |
| | | | 1 MHz | 0.9 | 0.5 | |
| | | | 500 kHz | 0.7 | 0.45 | |
| | | | 125 kHz | 0.6 | 0.45 | |

1. Typical values are measures at $T_A$ = 25 °C, $V_{DD}$ = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

## On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 20*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and $V_{DD}$ supply voltage conditions summarized in *Table 7*.

**Table 21. High-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{in(HSE)}$ | OSC_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(HSE)}$ | Duty cycle | - | 45 | - | 55 | % |
| $I_L$ | OSC_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design, not tested in production

### Low-speed external user clock generated from an external source

The characteristics given in *Table 22* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

**Table 22. Low-speed user external clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User external clock source frequency(1) | - | - | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | - | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | - | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{w(LSE)}$ | OSC32_IN high or low time(1) | - | 450 | - | - | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | - | - | - | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | - | - | 5 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle | - | 30 | - | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design, not tested in production.

**Figure 17. High-speed external clock source AC timing diagram**

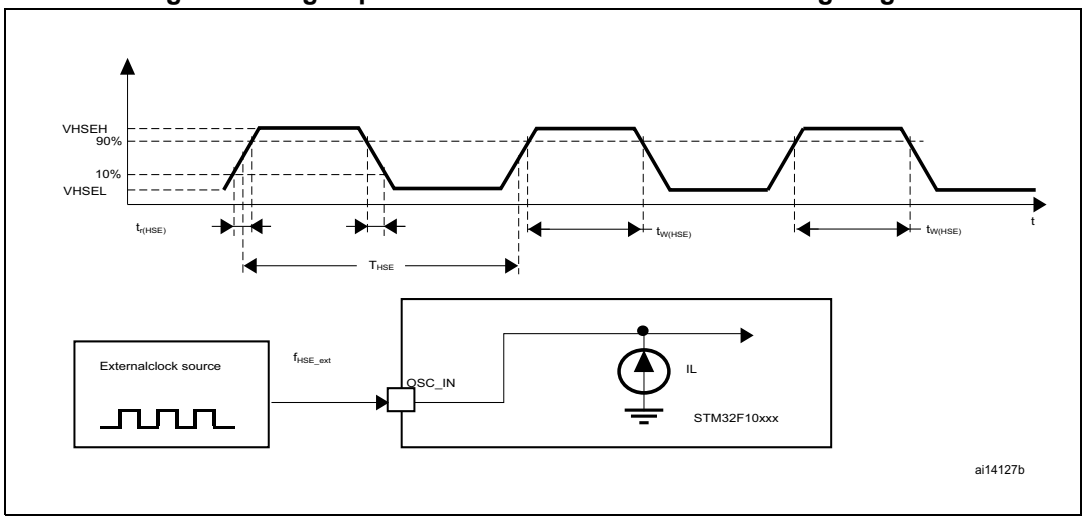
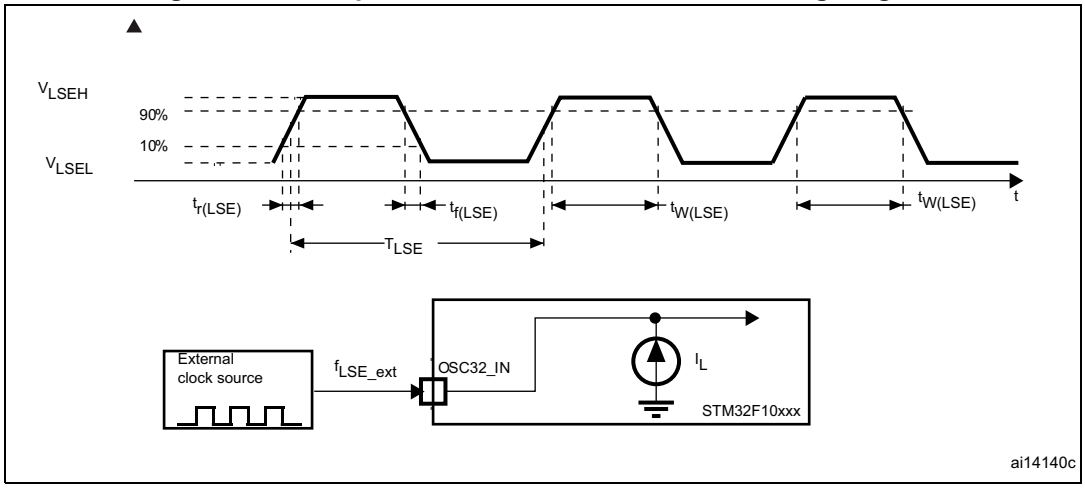



**Figure 18. Low-speed external clock source AC timing diagram**



### 5.3.8 PLL characteristics

The parameters given in *Table 28* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 10*.

**Table 28. PLL characteristics**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min(1) | Typ | Max(1) | |
| $f_{PLL\_IN}$ | PLL input clock(2) | 1 | 8.0 | 25 | MHz |
| | PLL input clock duty cycle | 40 | - | 60 | % |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | 16 | - | 36 | MHz |
| $t_{LOCK}$ | PLL lock time | - | - | 200 | µs |
| Jitter | Cycle-to-cycle jitter | - | - | 300 | ps |

1. Guaranteed by characterization results, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by $f_{PLL\_OUT}$.

### 5.3.9 Memory characteristics

#### Flash memory

The characteristics are given at $T_A$ = –40 to 85 °C unless otherwise specified.

**Table 29. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | 16-bit programming time | $T_A$ = –40 to +85 °C | 40 | 52.5 | 70 | µs |
| $t_{ERASE}$ | Page (2 KB) erase time | $T_A$ = –40 to +85 °C | 20 | - | 40 | ms |
| $t_{ME}$ | Mass erase time | $T_A$ = –40 to +85 °C | 20 | - | 40 | ms |
| $I_{DD}$ | Supply current | Read mode $f_{HCLK}$ = 36 MHz with 1 wait state, $V_{DD}$ = 3.3 V | - | - | 28 | mA |
| | | Write mode $f_{HCLK}$ = 36 MHz, $V_{DD}$ = 3.3 V | - | - | 7 | mA |
| | | Erase mode $f_{HCLK}$ = 36 MHz, $V_{DD}$ = 3.3 V | - | - | 5 | mA |
| | | Power-down mode / Halt, $V_{DD}$ = 3.0 to 3.6 V | - | - | 50 | µA |
| $V_{prog}$ | Programming voltage | | 2 | - | 3.6 | V |

1. Guaranteed by design, not tested in production.

**Table 38. Synchronous non-multiplexed PSRAM write timings(1)(2) (continued)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{h(CLKH-NWAITV)}$ | FSMC_NWAIT valid after FSMC_CLK high | 2 | - | ns |
| $t_{d(CLKL-NBLH)}$ | FSMC_CLK low to FSMC_NBL high | 1 | - | ns |

1. $C_L$ = 15 pF.
2. Guaranteed by characterization results, not tested in production.

### PC Card/CompactFlash controller waveforms and timings

*Figure 29* through *Figure 34* represent synchronous waveforms and *Table 39* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

**Figure 35. NAND controller waveforms for read access**

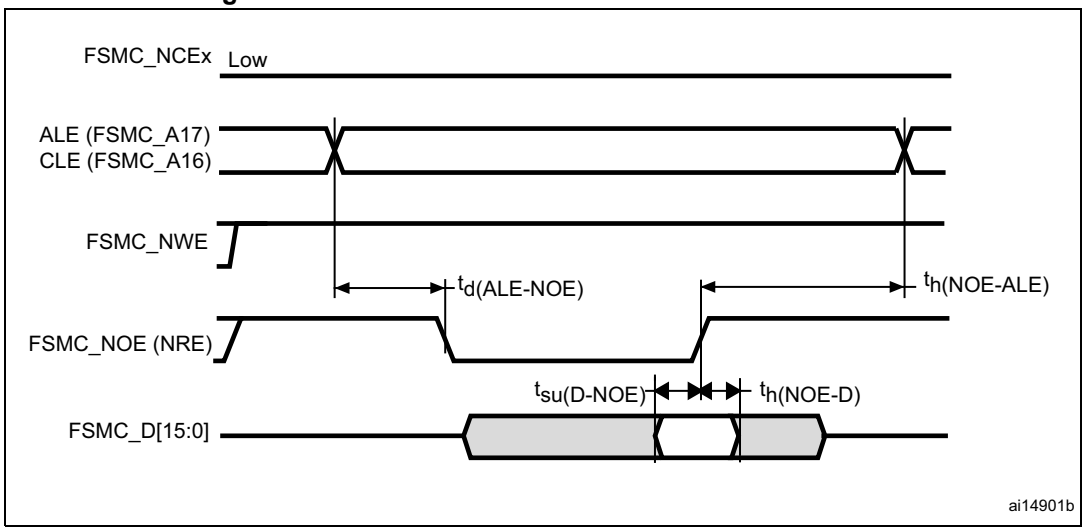



**Figure 36. NAND controller waveforms for write access**

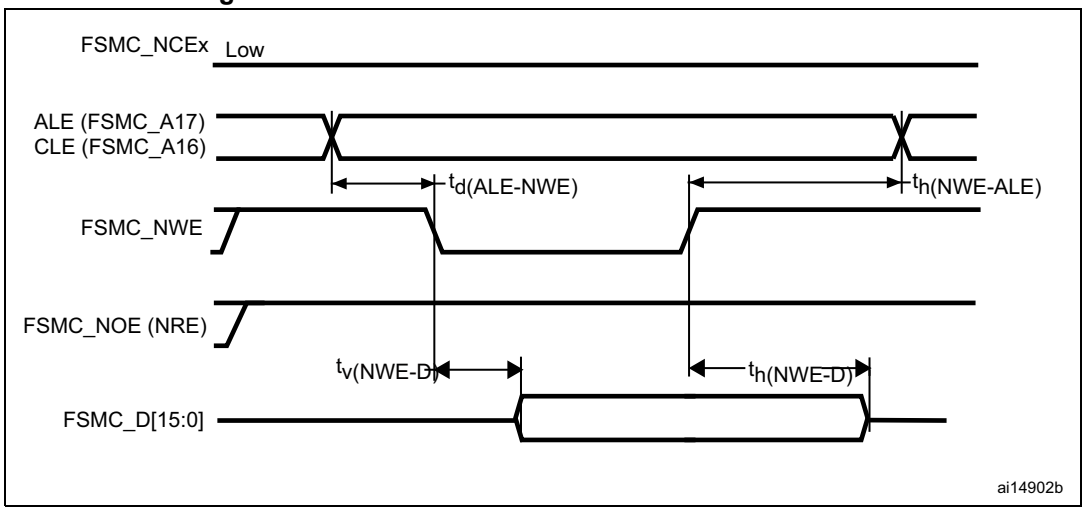



**Figure 37. NAND controller waveforms for common memory read access**

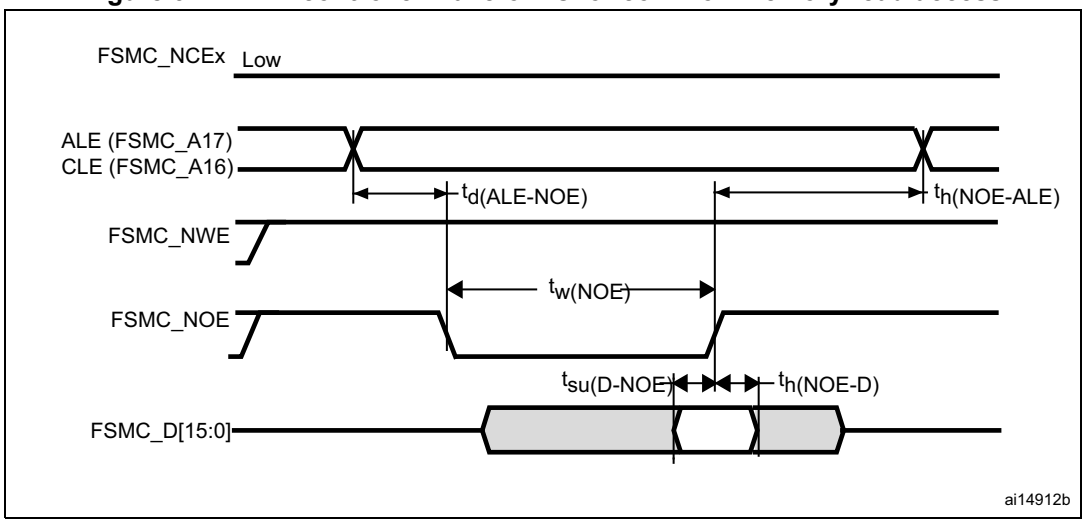


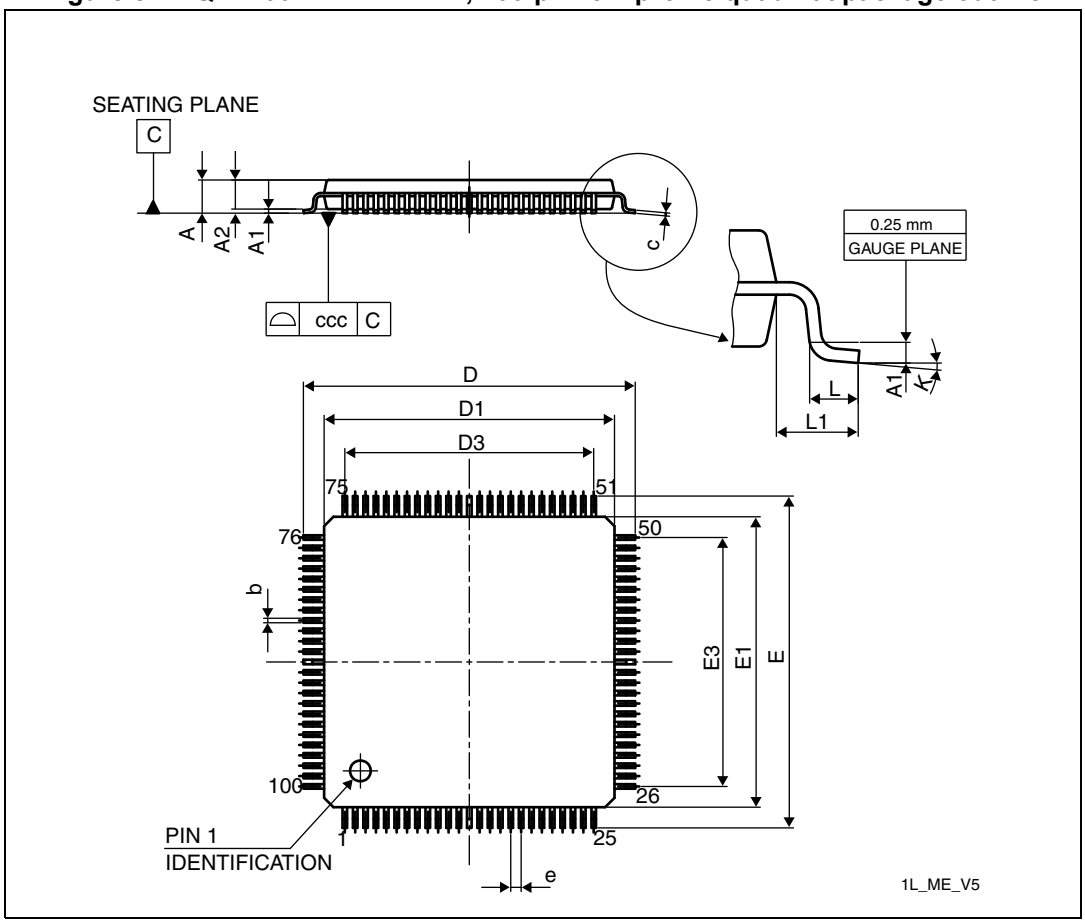
**Table 54. SPI characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 18 | MHz |
| | | Slave mode | - | 18 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 8 | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$ (1) | NSS setup time | Slave mode | $4t_{PCLK}$ | - | ns |
| $t_{h(NSS)}$ (1) | NSS hold time | Slave mode | $2t_{PCLK}$ | - | |
| $t_{w(SCKH)}$ (1)<br>$t_{w(SCKL)}$ (1) | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 50 | 60 | |
| $t_{su(MI)}$ (1)<br>$t_{su(SI)}$ (1) | Data input setup time | Master mode | 5 | - | |
| | | Slave mode | 5 | - | |
| $t_{h(MI)}$ (1) | Data input hold time | Master mode | 5 | - | |
| $t_{h(SI)}$ (1) | | Slave mode | 4 | - | |
| $t_{a(SO)}$ (1)(2) | Data output access time | Slave mode, $f_{PCLK}$ = 20 MHz | 0 | $3t_{PCLK}$ | |
| $t_{dis(SO)}$ (1)(3) | Data output disable time | Slave mode | 2 | 10 | |
| $t_{v(SO)}$ (1)(1) | Data output valid time | Slave mode (after enable edge) | - | 25 | |
| $t_{v(MO)}$ (1)(1) | Data output valid time | Master mode (after enable edge) | - | 5 | |
| $t_{h(SO)}$ (1) | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| $t_{h(MO)}$ (1) | | Master mode (after enable edge) | 2 | - | |

1. Guaranteed by characterization results not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

## 6.2 LQFP100 package information

**Figure 57. LQFP100 – 14 x 14 mm, 100-pin low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 62. LQPF100 – 14 x 14 mm, 100-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.622 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | - | 12.000 | - | - | 0.4724 | - |
| E | 15.800 | 16.000 | 16.200 | 0.622 | 0.6299 | 0.6378 |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |

## 6.4 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 10: General operating conditions on page 40*.

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 64. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LQFP144 - 20 x 20 mm / 0.5 mm pitch | 30 | °C/W |
| | **Thermal resistance junction-ambient** LQFP100 - 14 x 14 mm / 0.5 mm pitch | 46 | |
| | **Thermal resistance junction-ambient** LQFP64 - 10 x 10 mm / 0.5 mm pitch | 45 | |

### 6.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air), available from www.jedec.org.