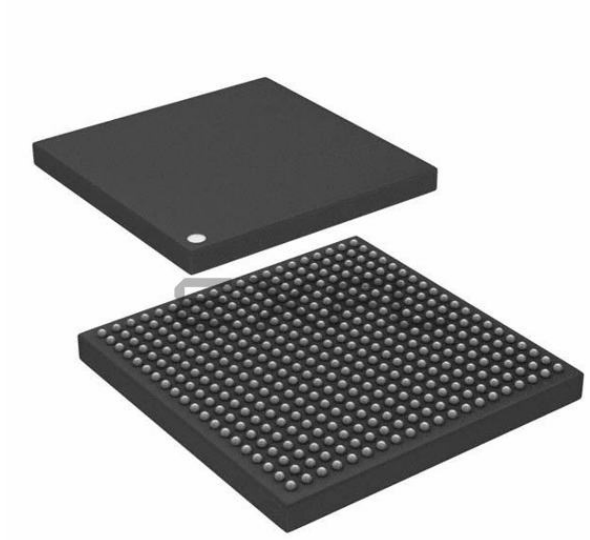

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, I²C, UART
Clock Rate	300MHz
Non-Volatile Memory	ROM (8kB)
On-Chip RAM	464kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmsc7118vm1200

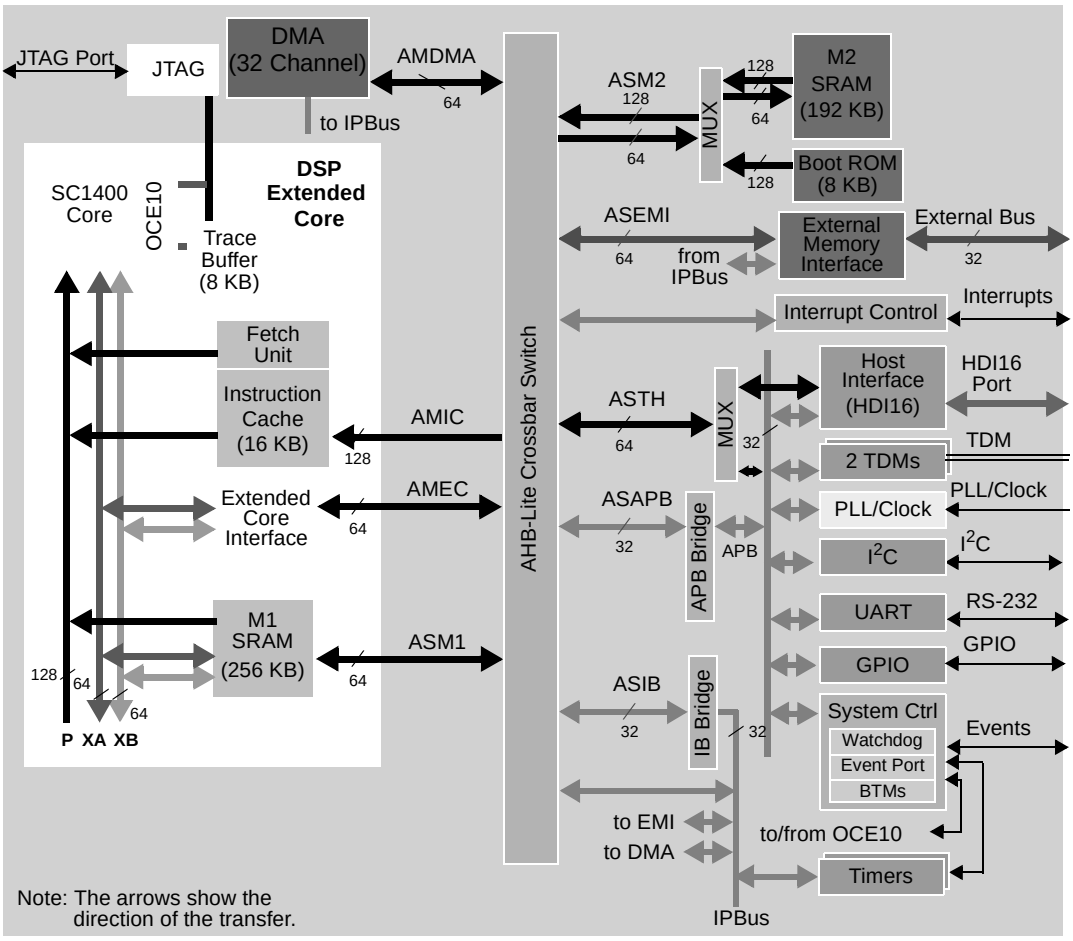


Figure 1. MSC7118 Block Diagram

1 Pin Assignments

This section includes diagrams of the MSC7118 package ball grid array layouts and pinout allocation tables.

1.1 MAP-BGA Ball Layout Diagrams

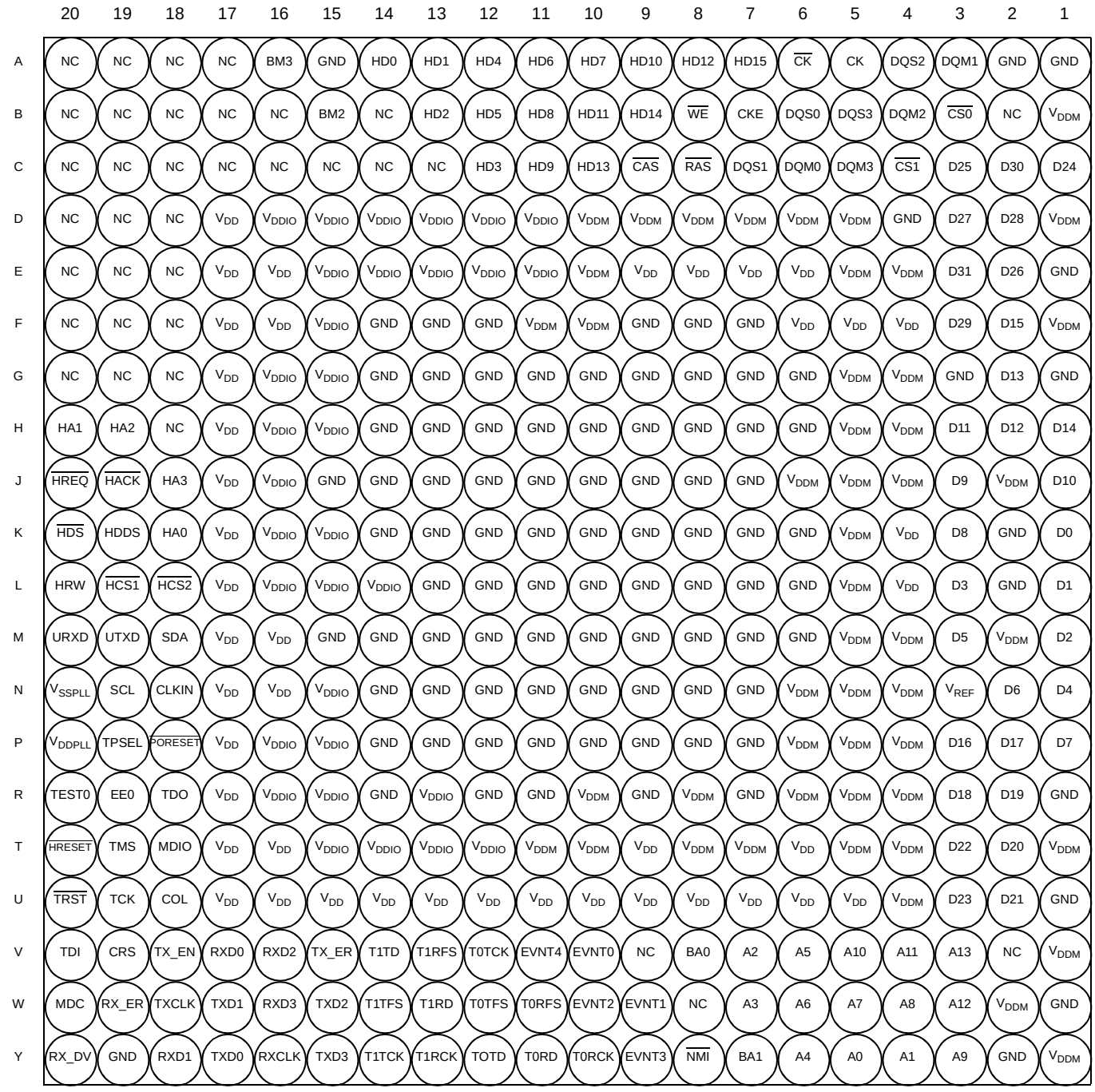
Top and bottom views of the MAP-BGA package are shown in **Figure 2** and **Figure 3** with their ball location index numbers.

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	DQM1	DQS2	CK	$\overline{CK}$	HD15	HD12	HD10	HD7	HD6	HD4	HD1	HD0	GND	BM3	NC	NC	NC	NC
B	V_{DDM}	NC	$\overline{CS0}$	DQM2	DQS3	DQS0	CKE	$\overline{WE}$	HD14	HD11	HD8	HD5	HD2	NC	BM2	NC	NC	NC	NC	NC
C	D24	D30	D25	$\overline{CS1}$	DQM3	DQM0	DQS1	$\overline{RAS}$	$\overline{CAS}$	HD13	HD9	HD3	NC	NC	NC	NC	NC	NC	NC	NC
D	V_{DDM}	D28	D27	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	NC	NC
E	GND	D26	D31	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	V_{DDC}	NC	NC	NC
F	V_{DDM}	D15	D29	V_{DDC}	V_{DDC}	V_{DDC}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DDIO}	V_{DDC}	V_{DDC}	NC	NC	NC
G	GND	D13	GND	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	NC	NC
H	D14	D12	D11	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	HA2	HA1
J	D10	V_{DDM}	D9	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDC}	HA3	$\overline{HACK}$	$\overline{HREQ}$
K	D0	GND	D8	V_{DDC}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	HA0	HDDS	$\overline{HDS}$
L	D1	GND	D3	V_{DDC}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	$\overline{HCS2}$	$\overline{HCS1}$	HRW
M	D2	V_{DDM}	D5	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDC}	V_{DDC}	SDA	UTXD	URXD
N	D4	D6	V_{REF}	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDC}	V_{DDC}	CLKIN	SCL	V_{SSPLL}
P	D7	D17	D16	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	$\overline{PORESET}$	TPSEL	V_{DDPLL}
R	GND	D19	D18	V_{DDM}	V_{DDM}	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	GND	GND	V_{DDIO}	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	TDO	EE0	TEST0
T	V_{DDM}	D20	D22	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDM}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	V_{DDC}	MDIO	TMS	$\overline{HRESET}$
U	GND	D21	D23	V_{DDM}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	COL	TCK	$\overline{TRST}$
V	V_{DDM}	NC	A13	A11	A10	A5	A2	BA0	NC	EVNT0	EVNT4	T0TCK	T1RFS	T1TD	TX_ER	RXD2	RXD0	TX_EN	CRS	TDI
W	GND	V_{DDM}	A12	A8	A7	A6	A3	NC	EVNT1	EVNT2	T0RFS	T0TFS	T1RD	T1TFS	TXD2	RXD3	TXD1	TXCLK	RX_ER	MDC
Y	V_{DDM}	GND	A9	A1	A0	A4	BA1	$\overline{NMI}$	EVNT3	T0RCK	T0RD	TOTD	T1RCK	T1TCK	TXD3	RXCLK	TXD0	RXD1	GND	RX_DV

Figure 2. MSC7118 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

Bottom View



	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	NC	NC	NC	BM3	GND	HD0	HD1	HD4	HD6	HD7	HD10	HD12	HD15	$\overline{CK}$	CK	DQS2	DQM1	GND	GND
B	NC	NC	NC	NC	NC	BM2	NC	HD2	HD5	HD8	HD11	HD14	$\overline{WE}$	CKE	DQS0	DQS3	DQM2	$\overline{CS0}$	NC	V_{DDM}
C	NC	NC	NC	NC	NC	NC	NC	NC	HD3	HD9	HD13	$\overline{CAS}$	$\overline{RAS}$	DQS1	DQM0	DQM3	$\overline{CS1}$	D25	D30	D24
D	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	GND	D27	D28	V_{DDM}
E	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	V_{DDM}	D31	D26	GND
F	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DD}	V_{DD}	V_{DD}	D29	D15	V_{DDM}
G	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	GND	D13	GND
H	HA1	HA2	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D11	D12	D14
J	$\overline{HREQ}$	$\overline{HACK}$	HA3	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D9	V_{DDM}	D10
K	$\overline{HDS}$	HDDS	HA0	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D8	GND	D0
L	HRW	$\overline{HCS1}$	$\overline{HCS2}$	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D3	GND	D1
M	URXD	UTXD	SDA	V_{DD}	V_{DD}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D5	V_{DDM}	D2
N	V_{SSPLL}	SCL	CLKIN	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{REF}	D6	D4
P	V_{DDPLL}	TPSEL	$\overline{PORESET}$	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D16	D17	D7
R	TEST0	EE0	TDO	V_{DD}	V_{DDIO}	V_{DDIO}	GND	V_{DDIO}	GND	GND	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	V_{DDM}	V_{DDM}	D18	D19	GND
T	$\overline{HRESET}$	TMS	MDIO	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	D22	D20	V_{DDM}
U	$\overline{TRST}$	TCK	COL	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	D23	D21	GND
V	TDI	CRS	TX_EN	RXD0	RXD2	TX_ER	T1TD	T1RFS	T0TCK	EVNT4	EVNT0	NC	BA0	A2	A5	A10	A11	A13	NC	V_{DDM}
W	MDC	RX_ER	TXCLK	TXD1	RXD3	TXD2	T1TFS	T1RD	T0TFS	T0RFS	EVNT2	EVNT1	NC	A3	A6	A7	A8	A12	V_{DDM}	GND
Y	RX_DV	GND	RXD1	TXD0	RXCLK	TXD3	T1TCK	T1RCK	TOTD	T0RD	T0RCK	EVNT3	$\overline{NMI}$	BA1	A4	A0	A1	A9	GND	V_{DDM}

Figure 3. MSC7118 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
B14	NC					
B15	BM2	GPID7		GPOD7	reserved	
B16	NC					
B17	NC					
B18	NC					
B19	NC					
B20	NC					
C1	D24					
C2	D30					
C3	D25					
C4	$\overline{CS1}$					
C5	DQM3					
C6	DQM0					
C7	DQS1					
C8	$\overline{RAS}$					
C9	$\overline{CAS}$					
C10	GPIC5			GPOC5	HD13	
C11	GPIC1			GPOC1	HD9	
C12	reserved				HD3	
C13	NC					
C14	NC					
C15	NC					
C16	NC					
C17	NC					
C18	NC					
C19	NC					
C20	NC					
D1	V_{DDM}					
D2	D28					
D3	D27					
D4	GND					
D5	V_{DDM}					
D6	V_{DDM}					
D7	V_{DDM}					
D8	V_{DDM}					
D9	V_{DDM}					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
F6	V_{DDC}					
F7	GND					
F8	GND					
F9	GND					
F10	V_{DDM}					
F11	V_{DDM}					
F12	GND					
F13	GND					
F14	GND					
F15	V_{DDIO}					
F16	V_{DDC}					
F17	V_{DDC}					
F18	NC					
F19	NC					
F20	NC					
G1	GND					
G2	D13					
G3	GND					
G4	V_{DDM}					
G5	V_{DDM}					
G6	GND					
G7	GND					
G8	GND					
G9	GND					
G10	GND					
G11	GND					
G12	GND					
G13	GND					
G14	GND					
G15	V_{DDIO}					
G16	V_{DDIO}					
G17	V_{DDC}					
G18	NC					
G19	NC					
G20	NC					
H1	D14					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
N10	GND					
N11	GND					
N12	GND					
N13	GND					
N14	GND					
N15	V_{DDIO}					
N16	V_{DDC}					
N17	V_{DDC}					
N18	CLKIN					
N19	GPIA15		$\overline{IRQ14}$	GPOA15	SCL	
N20	V_{SSPLL}					
P1	D7					
P2	D17					
P3	D16					
P4	V_{DDM}					
P5	V_{DDM}					
P6	V_{DDM}					
P7	GND					
P8	GND					
P9	GND					
P10	GND					
P11	GND					
P12	GND					
P13	GND					
P14	GND					
P15	V_{DDIO}					
P16	V_{DDIO}					
P17	V_{DDC}					
P18	$\overline{PORESET}$					
P19	TPSEL					
P20	V_{DDPLL}					
R1	GND					
R2	D19					
R3	D18					
R4	V_{DDM}					
R5	V_{DDM}					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
V18	GPIA24		$\overline{\text{IRQ24}}$	GPOA24	TX_EN	
V19	reserved				CRS	
V20	TDI					
W1	GND					
W2	V_{DDM}					
W3	A12					
W4	A8					
W5	A7					
W6	A6					
W7	A3					
W8	NC					
W9	GPIA17		$\overline{\text{IRQ13}}$	GPOA17	EVNT1	CLKO
W10	BM0	GPIC14		GPOC14	EVNT2	
W11	GPIA10		$\overline{\text{IRQ5}}$	GPOA10	T0RFS	
W12	GPIA7		$\overline{\text{IRQ7}}$	GPOA7	T0TFS	
W13	GPIA3		$\overline{\text{IRQ8}}$	GPOA3	T1RD	
W14	GPIA1		$\overline{\text{IRQ10}}$	GPOA1	T1TFS	
W15	GPID4			GPOD4	TXD2	reserved
W16	GPIA27		$\overline{\text{IRQ18}}$	GPOA27	RXD3	reserved
W17	GPIA19		$\overline{\text{IRQ19}}$	GPOA19	TXD1	
W18	GPIA23		$\overline{\text{IRQ23}}$	GPOA23	TXCLK or REFCLK	
W19	GPIA26		$\overline{\text{IRQ26}}$	GPOA26	RX_ER	
W20	H8BIT	reserved			MDC	
Y1	V_{DDM}					
Y2	GND					
Y3	A9					
Y4	A1					
Y5	A0					
Y6	A4					
Y7	BA1					
Y8	reserved		$\overline{\text{NMI}}$	reserved		
Y9	BM1	GPIC15		GPOC15	EVNT3	
Y10	GPIA11		$\overline{\text{IRQ4}}$	GPOA11	T0RCK	
Y11	GPIA9			GPOA9	T0RD	
Y12	GPIA6			GPOA6	T0TD	
Y13	GPIA5		$\overline{\text{IRQ0}}$	GPOA5	T1RCK	

Table 2 describes the maximum electrical ratings for the MSC7118.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.5	V
Memory supply voltage	V_{DDM}	4.0	V
PLL supply voltage	V_{DDPLL}	1.5	V
I/O supply voltage	V_{DDIO}	–0.2 to 4.0	V
Input voltage	V_{IN}	(GND – 0.2) to 4.0	V
Reference voltage	V_{REF}	4.0	V
Maximum operating temperature	T_J	105	°C
Minimum operating temperature	T_A	–40	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 3.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 3.1**, *Thermal Design Considerations* includes a formula for computing the chip junction temperature (T_J).

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.14 to 1.26	V
Memory supply voltage	V_{DDM}	2.38 to 2.63	V
PLL supply voltage	V_{DDPLL}	1.14 to 1.26	V
I/O supply voltage	V_{DDIO}	3.14 to 3.47	V
Reference voltage	V_{REF}	1.19 to 1.31	V
Operating temperature range	T_J T_A	maximum: 105 minimum: –40	°C °C

2.5 AC Timings

This section presents timing diagrams and specifications for individual signals and parallel I/O outputs and inputs. All AC timings are based on a 30 pF load, except where noted otherwise, and a 50 Ω transmission line. For any additional pF, use the following equations to compute the delay:

— Standard interface: 2.45 + (0.054 × C_{load}) ns
— DDR interface: 1.6 + (0.002 × C_{load}) ns

2.5.1 Clock and Timing Signals

The following tables describe clock signal characteristics. **Table 6** shows the maximum frequency values for internal (core, reference, and peripherals) and external (CLKO) clocks. You must ensure that maximum frequency values are not exceeded (see **Section 2.5.2** for the allowable ranges when using the PLL).

Table 6. Maximum Frequencies

Characteristic	Maximum in MHz
Core clock frequency (CLOCK)	300
External output clock frequency (CLKO)	75
Memory clock frequency (CK, $\overline{CK}$)	150
TDM clock frequency (TxRCK, TxTCK)	50

Table 7. Clock Frequencies in MHz

Characteristic	Symbol	Min	Max
CLKIN frequency	F_{CLKIN}	10	100
CLOCK frequency	F_{CORE}	—	300
CK, $\overline{CK}$ frequency	F_{CK}	—	150
TDMxRCK, TDMxTCK frequency	F_{TDMCK}	—	50
CLKO frequency	F_{CKO}	—	75
AHB/IPBus/APB clock frequency	F_{BCK}	—	150
Note: The rise and fall time of external clocks should be 5 ns maximum			

Table 8. System Clock Parameters

Characteristic	Min	Max	Unit
CLKIN frequency	10	100	MHz
CLKIN slope	—	5	ns
CLKIN frequency jitter (peak-to-peak)	—	1000	ps
CLKO frequency jitter (peak-to-peak)	—	150	ps

2.5.2 Configuring Clock Frequencies

This section describes important requirements for configuring clock frequencies in the MSC7118 device when using the PLL block. To configure the device clocking, you must program four fields in the Clock Control Register (CLKCTL):

- *PLLDVF field*. Specifies the PLL division factor (PLLDVF + 1) to divide the input clock frequency F_{CLKIN}. The output of the divider block is the input to the multiplier block.
- *PLLMLTF field*. Specifies the PLL multiplication factor (PLLMLTF + 1). The output from the multiplier block is the loop frequency F_{LOOP}.
- *RNG field*. Selects the available PLL frequency range for F_{VCO}, either F_{LOOP} when the RNG bit is set (1) or $F_{LOOP}/2$ when the RNG bit is cleared (0).
- *CKSEL field*. Selects F_{CLKIN}, F_{VCO}, or $F_{VCO}/2$ as the source for the core clock.

There are restrictions on the frequency range permitted at the beginning of the multiplication portion of the PLL that affect the allowable values for the PLLDVF and PLLMLTF fields. The following sections define these restrictions and provide guidelines to configure the device clocking when using the PLL. Refer to the Clock and Power Management chapter in the *MSC711x Reference Manual* for details on the clock programming model.

2.5.2.1 PLL Multiplier Restrictions

There are two restrictions for correct usage of the PLL block:

- The input frequency to the PLL multiplier block (that is, the output of the divider) must be in the range 10–25 MHz.
- The output frequency of the PLL multiplier must be in the range 266–532 MHz.

When programming the PLL for a desired output frequency using the PLLDVF, PLLMLTF, and RNG fields, you must meet these constraints.

2.5.2.2 Input Division Factors and Corresponding CLKIN Frequency Range

The value of the PLLDVF field determines the allowable CLKIN frequency range, as shown in **Table 9**.

Table 9. CLKIN Frequency Ranges by Divide Factor Value

PLLDVF Field Value	Input Divide Factor	CLKIN Frequency Range	Comments
0x00	1	10 to 25 MHz	Input Division by 1
0x01	2	20 to 50 MHz	Input Division by 2
0x02	3	30 to 75 MHz	Input Division by 3
0x03	4	40 to 100 MHz	Input Division by 4
0x04	5	50 to 100 MHz	Input Division by 5
0x05	6	60 to 100 MHz	Input Division by 6
0x06	7	70 to 100 MHz	Input Division by 7
0x07	8	80 to 100 MHz	Input Division by 8
0x08	9	90 to 100 MHz	Input Division by 9
0x09	10	100 MHz	Input Division by 10
Note: The maximum CLKIN frequency is 100 MHz. Therefore, the PLLDVF value must be in the range from 1–10.			

2.5.2.3 Multiplication Factor Range

The multiplier block output frequency ranges depend on the divided input clock frequency as shown in **Table 10**.

Table 10. PLLMLTF Ranges

Multiplier Block (Loop) Output Range	Minimum PLLMLTF Value	Maximum PLLMLTF Value
266 ≤ [Divided Input Clock × (PLLMLTF + 1)] ≤ 532 MHz	266/Divided Input Clock	532/Divided Input Clock
Note: This table results from the allowed range for F_{Loop}. The minimum and maximum multiplication factors are dependent on the frequency of the Divided Input Clock.		

2.5.2.4 Allowed Core Clock Frequency Range

The frequency delivered to the core, extended core, and peripherals depends on the value of the CLKCTRL[RNG] bit as shown in **Table 11**.

Table 11. F_{vco} Frequency Ranges

CLKCTRL[RNG] Value	Allowed Range of F_{vco}
1	266 ≤ F_{vco} ≤ 532 MHz
0	133 ≤ F_{vco} ≤ 266 MHz
Note: This table results from the allowed range for F_{vco}, which is F_{Loop} modified by CLKCTRL[RNG].	

This bit along with the CKSEL determines the frequency range of the core clock.

Table 12. Resulting Ranges Permitted for the Core Clock

CLKCTRL[CKSEL]	CLKCTRL[RNG]	Resulting Division Factor	Allowed Range of Core Clock	Comments
11	1	1	266 ≤ core clock ≤ 300 MHz	Limited by maximum core frequency
11	0	2	133 ≤ core clock ≤ 266 MHz	Limited by range of PLL
01	1	2	133 ≤ core clock ≤ 266 MHz	Limited by range of PLL
01	0	4	66.5 ≤ core clock ≤ 133 MHz	Limited by range of PLL
Note: This table results from the allowed range for F_{OUT}, which depends on clock selected via CLKCTRL[CKSEL].				

2.5.2.5 Core Clock Frequency Range When Using DDR Memory

The core clock can also be limited by the frequency range of the DDR devices in the system. **Table 13** summarizes this restriction.

Table 13. Core Clock Ranges When Using DDR

DDR Type	Allowed Frequency Range for DDR CK	Corresponding Range for the Core Clock	Comments
DDR 200 (PC-1600)	83–100 MHz	166 ≤ core clock ≤ 200 MHz	Core limited to 2 × maximum DDR frequency
DDR 266 (PC-2100)	83–133 MHz	166 ≤ core clock ≤ 266 MHz	Core limited to 2 × maximum DDR frequency
DDR 333 (PC-2600)	83–150 MHz	166 ≤ core clock ≤ 300 MHz	Core limited to 2 × maximum DDR frequency

2.5.3 Reset Timing

The MSC7118 device has several inputs to the reset logic. All MSC7118 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 14** describes the reset sources.

Table 14. Reset Sources

Name	Direction	Description
Power-on reset (PORESET)	Input	Initiates the power-on reset flow that resets the MSC7118 and configures various attributes of the MSC7118. On PORESET, the entire MSC7118 device is reset. SPLL and DLL states are reset, HRESET is driven, the SC1400 extended core is reset, and system configuration is sampled. The system is configured only when PORESET is asserted.
External Hard reset (HRESET)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC7118. While HRESET is asserted, HRESET is an open-drain output. Upon hard reset, HRESET is driven and the SC1400 extended core is reset.
Software watchdog reset	Internal	When the MSC7118 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC7118 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
JTAG EXTEST, CLAMP, or HIGHZ command	Internal	When a Test Access Port (TAP) executes an EXTEST, CLAMP, or HIGHZ command, the TAP logic asserts an internal reset signal that generates an internal soft reset sequence.

Table 15 summarizes the reset actions that occur as a result of the different reset sources.

Table 15. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)
	External only	External or Internal (Software Watchdog or Bus Monitor)	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (refer to **Section 2.5.3.1** for details).	Yes	No	No
PLL and clock synthesis states Reset	Yes	No	No
HRESET Driven	Yes	Yes	No
Software watchdog and bus time-out monitor registers	Yes	Yes	Yes
Clock synthesis modules (STOPCTRL, HLTREQ, and HLTACK) reset	Yes	Yes	Yes
Extended core reset	Yes	Yes	Yes
Peripheral modules reset	Yes	Yes	Yes

2.5.3.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 16 CLKIN cycles after external power to the MSC7118 reaches at least 2/3 V_{DD}.

2.5.4 DDR DRAM Controller Timing

This section provides the AC electrical characteristics for the DDR DRAM interface.

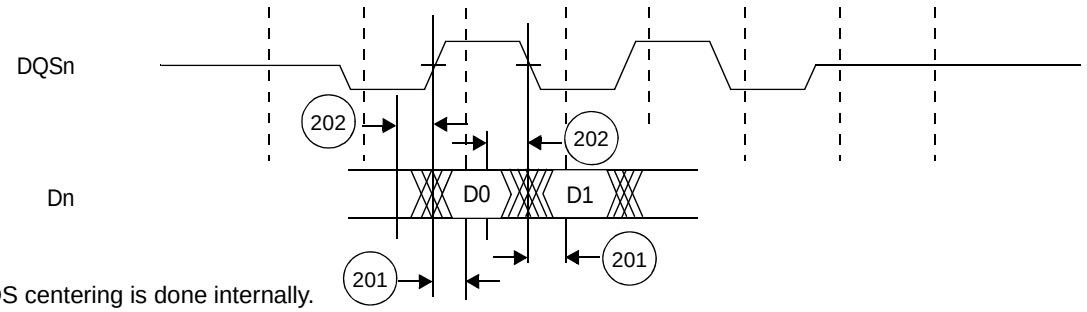
2.5.4.1 DDR DRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR DRAM interface.

Table 17. DDR DRAM Input AC Timing

No.	Parameter	Symbol	Min	Max	Unit
—	AC input low voltage	V_{IL}	—	V_{REF} – 0.31	V
—	AC input high voltage	V_{IH}	V_{REF} + 0.31	V_{DDM} + 0.3	V
201	Maximum Dn input setup skew relative to DQSn input	—	—	900	ps
202	Maximum Dn input hold skew relative to DQSn input	—	—	900	ps

Notes:
1. Maximum possible skew between a data strobe (DQSn) and any corresponding bit of data (D[8n + {0...7}] if 0 ≤ n ≤ 7).
2. See **Table 18** for t_{CK} value.
3. Dn should be driven at the same time as DQSn. This is necessary because the DQSn centering on the DQn data tenure is done internally.



Note: DQS centering is done internally.

Figure 5. DDR DRAM Input Timing Diagram

2.5.4.2 DDR DRAM Output AC Timing Specifications

Table 18 and **Table 19** list the output AC timing specifications and measurement conditions for the DDR DRAM interface.

Table 18. DDR DRAM Output AC Timing

No.	Parameter	Symbol	Min	Max	Unit
200	CK cycle time, (CK/$\overline{CK}$ crossing)[1] • 100 MHz (DDR200) • 150 MHz (DDR300)	t_{CK}	 10 6.67	 — —	 ns ns
204	An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE output setup with respect to CK	t_{DDKHAS}	0.5 × t_{CK} – 1000	—	ps
205	An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE output hold with respect to CK	t_{DDKHAX}	0.5 × t_{CK} – 1000	—	ps
206	$\overline{CSn}$ output setup with respect to CK	t_{DDKHCS}	0.5 × t_{CK} – 1000	—	ps
207	$\overline{CSn}$ output hold with respect to CK	t_{DDKHCX}	0.5 × t_{CK} – 1000	—	ps
208	CK to DQSn[2]	t_{DDKHMH}	–600	600	ps

Figure 10 and **Figure 11** show HDI16 read signal timing. **Figure 12** and **Figure 13** show HDI16 write signal timing.

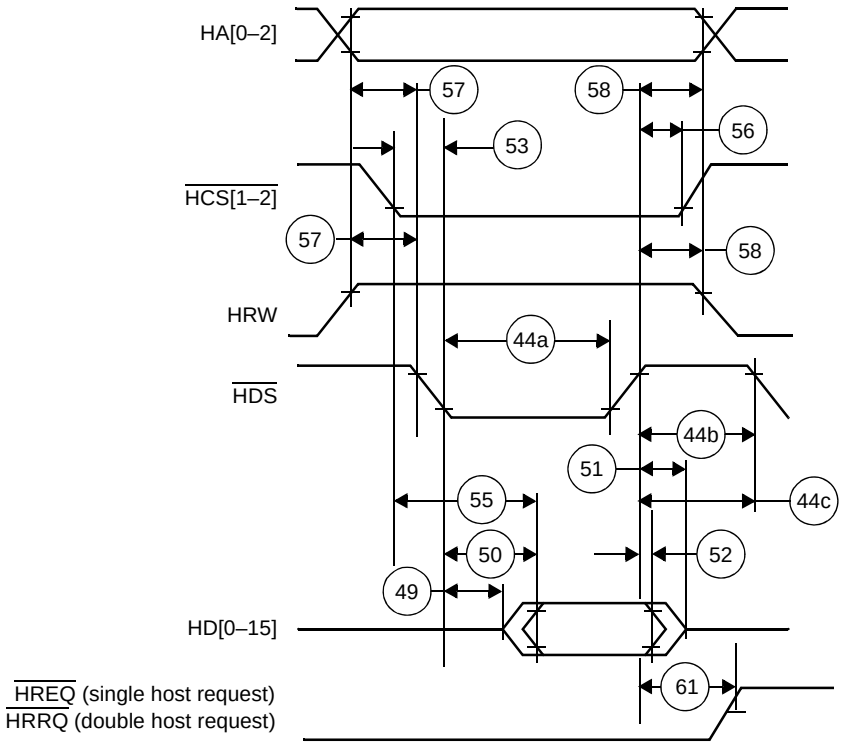


Figure 10. Read Timing Diagram, Single Data Strobe

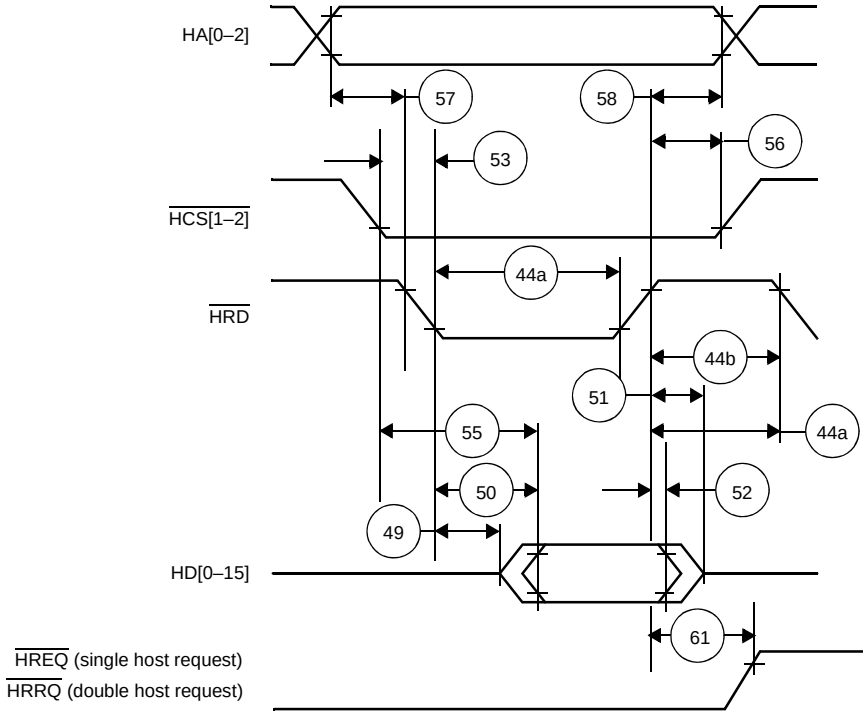


Figure 11. Read Timing Diagram, Double Data Strobe

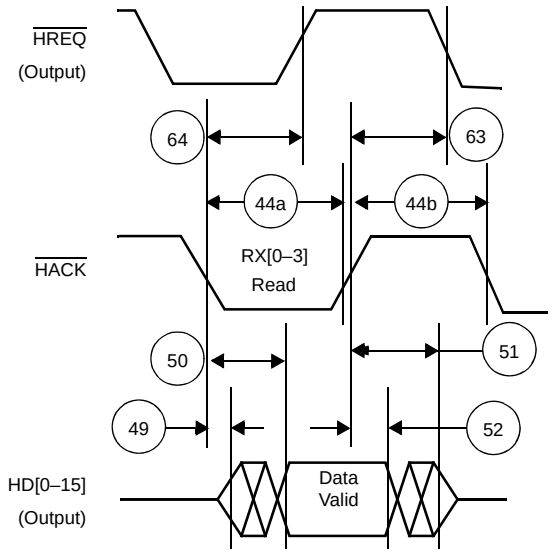


Figure 14. Host DMA Read Timing Diagram, HPCR[OAD] = 0

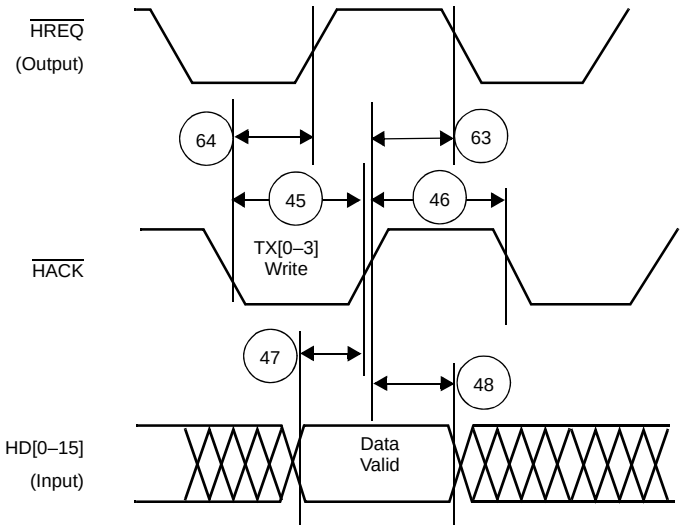


Figure 15. Host DMA Write Timing Diagram, HPCR[OAD] = 0

2.5.8 UART Timing

Table 23. UART Timing

No.	Characteristics	Expression	Min	Max	Unit
—	Internal bus clock (APBCLK)	$F_{CORE}/2$	—	150	MHz
—	Internal bus clock period (1/APBCLK)	T_{APBCLK}	6.67	—	ns
400	URXD and UTXD inputs high/low duration	$16 \times T_{APBCLK}$	106.67	—	ns
401	URXD and UTXD inputs rise/fall time		—	5	ns
402	UTXD output rise/fall time		—	5	ns

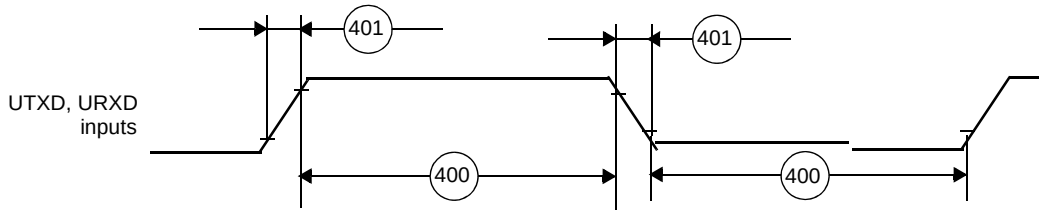


Figure 17. UART Input Timing

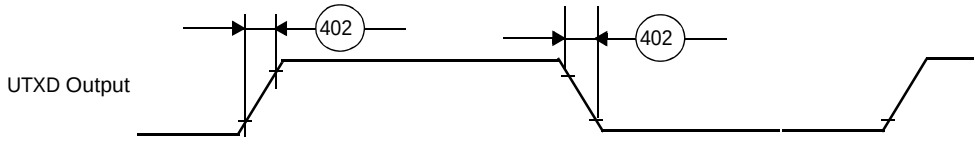


Figure 18. UART Output Timing

2.5.9 EE Timing

Table 24. EE0 Timing

Number	Characteristics	Type	Min
65	EE0 input to the core	Asynchronous	4 core clock periods
66	EE0 output from the core	Synchronous to core clock	1 core clock period

Notes:
1. The core clock is the SC1400 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Configure the direction of the EE pin in the EE_CTRL register (see the *SC140/SC1400 Core Reference Manual* for details.
3. Refer to **Table 1-11** on page 1-16 for details on EE pin functionality.

Figure 20 shows the signal behavior of the EE pin.

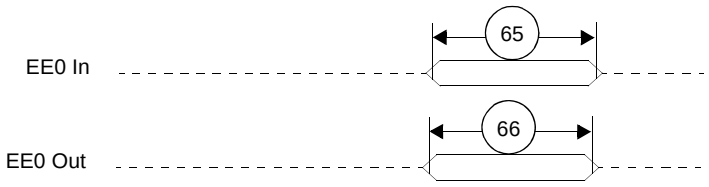


Figure 19. EE Pin Timing

2.5.10 Event Timing

Table 25. EVNT Signal Timing

Number	Characteristics	Type	Min
67	EVNT as input	Asynchronous	1.5 × APBCLK periods
68	EVNT as output	Synchronous to core clock	1 APBCLK period

Notes:
1. Refer to **Table 23** for a definition of the APBCLK period.
2. Direction of the EVNT signal is configured through the GPIO and Event port registers.
3. Refer to the signal chapter in the *MSC711x Reference Manual* for details on EVNT pin functionality.

Figure 20 shows the signal behavior of the EVNT pins.

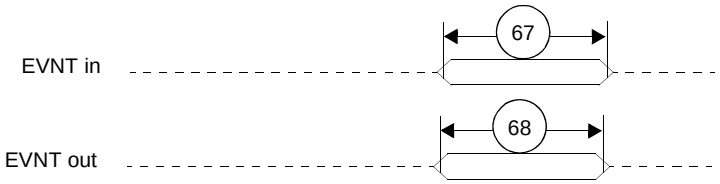


Figure 20. EVNT Pin Timing

2.5.11 GPIO Timing

Table 26. GPIO Signal Timing[1,2,3]

Number	Characteristics	Type	Min
601	GPI[4,5]	Asynchronous	1.5 × APBCLK periods
602	GPO[5]	Synchronous to core clock	1 APBCLK period
603	Port A edge-sensitive interrupt	Asynchronous	1.5 × APBCLK periods
604	Port A level-sensitive interrupt	Asynchronous	3 × APBCLK periods[6]

Notes:
1. Refer to **Table 23** for a definition of the APBCLK period.
2. Direction of the GPIO signal is configured through the GPIO port registers.
3. Refer to **Section 1.5** for details on GPIO pin functionality.
4. GPI data is synchronized to the APBCLK internally and the minimum listed is the capability of the hardware to capture data into a register when the GPADR is read. The specification is not tested due to the asynchronous nature of the input and dependence on the state of the DSP core. It is guaranteed by design.
5. The output signals cannot toggle faster than 75 MHz.
6. Level-sensitive interrupts should be held low until the system determines (via the service routine) that the interrupt is acknowledged.

Figure 21 shows the signal behavior of the GPI/GPO pins.

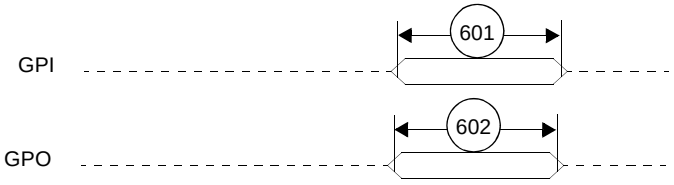


Figure 21. GPI/GPO Pin Timing

3.2 Power Supply Design Considerations

This section outlines the MSC7118 power considerations: power supply, power sequencing, power planes, decoupling, power supply filtering, and power consumption. It also presents a recommended power supply design and options for low-power consumption. For information on AC/DC electrical specifications and thermal characteristics, refer to **Section 2**.

3.2.1 Power Supply

The MSC7118 requires four input voltages, as shown in **Table 28**.

Table 28. MSC7118 Voltages

Voltage	Symbol	Value
Core	V_{DDC}	1.2 V
Memory	V_{DDM}	2.5 V
Reference	V_{REF}	1.25 V
I/O	V_{DDIO}	3.3 V

You should supply the MSC7118 core voltage via a variable switching supply or regulator to allow for compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied with 1.2 V (+5% and –10%) across V_{DDC} and GND and the I/O section is supplied with 3.3 V (± 10%) across V_{DDIO} and GND. The memory and reference voltages supply the DDR memory controller block. The memory voltage is supplied with 2.5 V across V_{DDM} and GND. The reference voltage is supplied across V_{REF} and GND and must be between $0.49 \times V_{DDM}$ and $0.51 \times V_{DDM}$. Refer to the JEDEC standard JESD8 (*Stub Series Terminated Logic for 2.5 Volts* (STTL_2)) for memory voltage supply requirements.

3.2.2 Power Sequencing

One consequence of multiple power supplies is that the voltage rails ramp up at different rates when power is initially applied. The rates depend on the power supply, the type of load on each power supply, and the way different voltages are derived. It is extremely important to observe the power up and power down sequences at the board level to avoid latch-up, forward biasing of ESD devices, and excessive currents, which all lead to severe device damage.

Note: There are five possible power-up/power-down sequence cases. The first four cases listed in the following sections are recommended for new designs. The fifth case is not recommended for new designs and must be carefully evaluated for current spike risks based on actual information for the specific application.

3.2.2.1 Case 1

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDM} (2.5 V) supply second.
3. Turn off the V_{DDC} (1.2 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 26** for relative timing for power sequencing case 1.

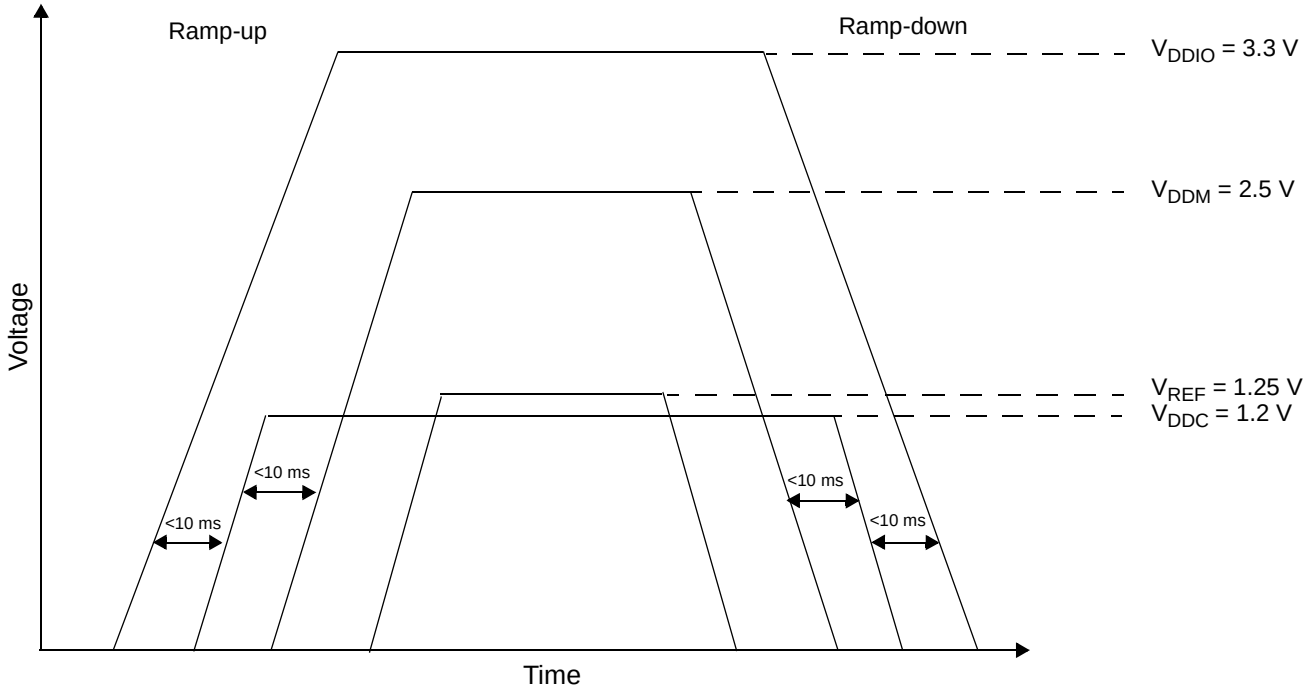


Figure 26. Voltage Sequencing Case 1

3.3.2 Peripheral Power

Peripherals include the DDR memory controller, DMA controller, HDI16, TDM, UART, timers, GPIOs, and the I^2C module. Basic power consumption by each module is assumed to be the same and is computed by using the following equation which assumes an effective load of 20 pF, core voltage swing of 1.2 V, and a switching frequency of 100 MHz. This yields:

$$P_{PERIPHERAL} = 20\ pF \times (1.2\ V)^2 \times 150\ MHz \times 10^{-3} = 4.32\ mW\ per\ peripheral \quad \text{Eqn. 6}$$

Multiply this value by the number of peripherals used in the application to compute the total peripheral power consumption.

3.3.3 External Memory Power

Estimation of power consumption by the DDR memory system is complex. It varies based on overall system signal line usage, termination and load levels, and switching rates. Because the DDR memory includes terminations external to the MSC7118 device, the 2.5 V power source provides the power for the termination, which is a static value of 16 mA per signal driven high. The dynamic power is computed, however, using a differential voltage swing of ±0.200 V, yielding a peak-to-peak swing of 0.4 V. The equations for computing the DDR power are:

$$P_{DDRIO} = P_{STATIC} + P_{DYNAMIC} \quad \text{Eqn. 7}$$

$$P_{STATIC} = (unused\ pins \times \%\ driven\ high) \times 16\ mA \times 2.5\ V \quad \text{Eqn. 8}$$

$$P_{DYNAMIC} = (pin\ activity\ value) \times 20\ pF \times (0.4\ V)^2 \times 300\ MHz \times 10^{-3}\ mW \quad \text{Eqn. 9}$$

$$pin\ activity\ value = (active\ data\ lines \times \%\ activity \times \%\ data\ switching) + (active\ address\ lines \times \%\ activity) \quad \text{Eqn. 10}$$

As an example, assume the following:

unused pins = 16 (DDR uses 16-pin mode)
% driven high = 50%
active data lines = 16
% activity = 60%
% data switching = 50%
active address lines = 3

In this example, the DDR memory power consumption is:

$$P_{DDRIO} = ((16 \times 0.5) \times 16 \times 2.5) + (((16 \times 0.6 \times 0.5) + (3 \times 0.6)) \times 20 \times (0.4)^2 \times 300 \times 10^{-3}) = 326.3\ mW \quad \text{Eqn. 11}$$

3.3.4 External I/O Power

The estimation of the I/O power is similar to the computation of the peripheral power estimates. The power consumption per signal line is computed assuming a maximum load of 20 pF, a voltage swing of 3.3 V, and a switching frequency of 25 MHz, which yields:

$$P_{IO} = 20\ pF \times (3.3\ V)^2 \times 25\ MHz \times 10^{-3} = 5.44\ mW\ per\ I/O\ line \quad \text{Eqn. 12}$$

Multiply this number by the number of I/O signal lines used in the application design to compute the total I/O power.

Note: The signal loading depends on the board routing. For systems using a single DDR device, the load could be as low as 7 pF.

3.3.5 Leakage Power

The leakage power is for all power supplies combined at a specific temperature. The value is temperature dependent. The observed leakage value at room temperature is 64 mW.