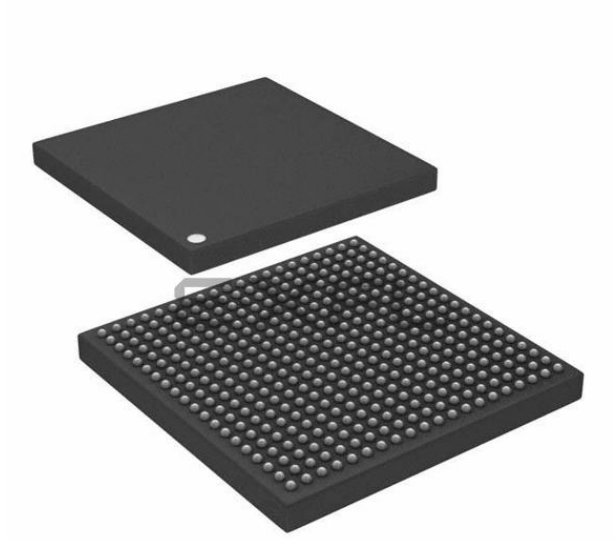


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, I²C, UART
Clock Rate	300MHz
Non-Volatile Memory	ROM (8kB)
On-Chip RAM	464kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc7118vm1200

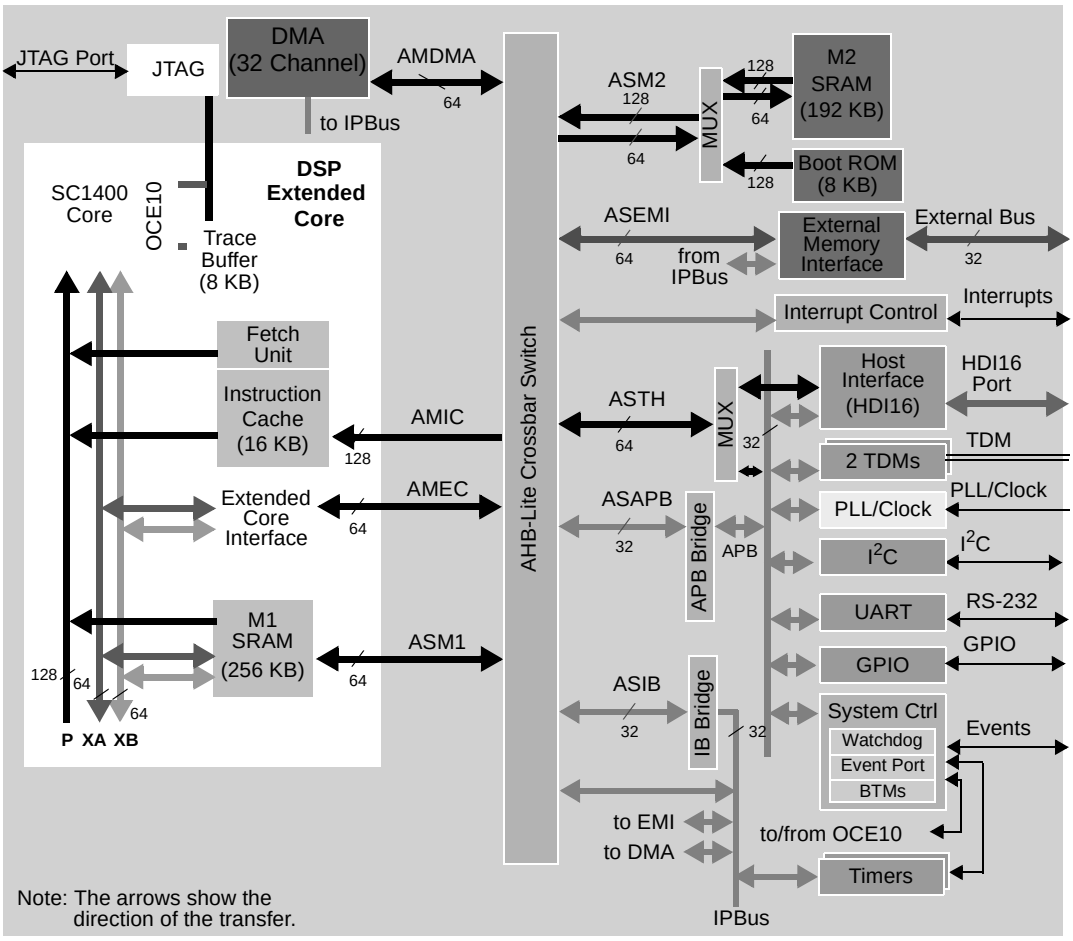


Figure 1. MSC7118 Block Diagram

1 Pin Assignments

This section includes diagrams of the MSC7118 package ball grid array layouts and pinout allocation tables.

1.1 MAP-BGA Ball Layout Diagrams

Top and bottom views of the MAP-BGA package are shown in **Figure 2** and **Figure 3** with their ball location index numbers.

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	DQM1	DQS2	CK	$\overline{CK}$	HD15	HD12	HD10	HD7	HD6	HD4	HD1	HD0	GND	BM3	NC	NC	NC	NC
B	V_{DDM}	NC	$\overline{CS0}$	DQM2	DQS3	DQS0	CKE	$\overline{WE}$	HD14	HD11	HD8	HD5	HD2	NC	BM2	NC	NC	NC	NC	NC
C	D24	D30	D25	$\overline{CS1}$	DQM3	DQM0	DQS1	$\overline{RAS}$	$\overline{CAS}$	HD13	HD9	HD3	NC	NC	NC	NC	NC	NC	NC	NC
D	V_{DDM}	D28	D27	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	NC	NC
E	GND	D26	D31	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	V_{DDC}	NC	NC	NC
F	V_{DDM}	D15	D29	V_{DDC}	V_{DDC}	V_{DDC}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DDIO}	V_{DDC}	V_{DDC}	NC	NC	NC
G	GND	D13	GND	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	NC	NC
H	D14	D12	D11	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	HA2	HA1
J	D10	V_{DDM}	D9	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDC}	HA3	$\overline{HACK}$	$\overline{HREQ}$
K	D0	GND	D8	V_{DDC}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	HA0	HDDS	$\overline{HDS}$
L	D1	GND	D3	V_{DDC}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	$\overline{HCS2}$	$\overline{HCS1}$	HRW
M	D2	V_{DDM}	D5	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDC}	V_{DDC}	SDA	UTXD	URXD
N	D4	D6	V_{REF}	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDC}	V_{DDC}	CLKIN	SCL	V_{SSPLL}
P	D7	D17	D16	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	$\overline{PORESET}$	TPSEL	V_{DDPLL}
R	GND	D19	D18	V_{DDM}	V_{DDM}	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	GND	GND	V_{DDIO}	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	TDO	EE0	TEST0
T	V_{DDM}	D20	D22	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDM}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	V_{DDC}	MDIO	TMS	$\overline{HRESET}$
U	GND	D21	D23	V_{DDM}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	COL	TCK	$\overline{TRST}$
V	V_{DDM}	NC	A13	A11	A10	A5	A2	BA0	NC	EVNT0	EVNT4	T0TCK	T1RFS	T1TD	TX_ER	RXD2	RXD0	TX_EN	CRS	TDI
W	GND	V_{DDM}	A12	A8	A7	A6	A3	NC	EVNT1	EVNT2	T0RFS	T0TFS	T1RD	T1TFS	TXD2	RXD3	TXD1	TXCLK	RX_ER	MDC
Y	V_{DDM}	GND	A9	A1	A0	A4	BA1	$\overline{NMI}$	EVNT3	T0RCK	T0RD	TOTD	T1RCK	T1TCK	TXD3	RXCLK	TXD0	RXD1	GND	RX_DV

Figure 2. MSC7118 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

1.2 Signal List By Ball Location

Table 1 lists the signals sorted by ball number and configuration.

Table 1. MSC7118 Signals by Ball Designator

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
A1	GND					
A2	GND					
A3	DQM1					
A4	DQS2					
A5	CK					
A6	$\overline{CK}$					
A7	GPIC7			GPOC7	HD15	
A8	GPIC4			GPOC4	HD12	
A9	GPIC2			GPOC2	HD10	
A10	reserved				HD7	
A11	reserved				HD6	
A12	reserved				HD4	
A13	reserved				HD1	
A14	reserved				HD0	
A15	GND					
A16	BM3	GPID8		GPOD8	reserved	
A17	NC					
A18	NC					
A19	NC					
A20	NC					
B1	V_{DDM}					
B2	NC					
B3	$\overline{CS0}$					
B4	DQM2					
B5	DQS3					
B6	DQS0					
B7	CKE					
B8	$\overline{WE}$					
B9	GPIC6			GPOC6	HD14	
B10	GPIC3			GPOC3	HD11	
B11	GPIC0			GPOC0	HD8	
B12	reserved				HD5	
B13	reserved				HD2	

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
B14	NC					
B15	BM2	GPID7		GPOD7	reserved	
B16	NC					
B17	NC					
B18	NC					
B19	NC					
B20	NC					
C1	D24					
C2	D30					
C3	D25					
C4	$\overline{CS1}$					
C5	DQM3					
C6	DQM0					
C7	DQS1					
C8	$\overline{RAS}$					
C9	$\overline{CAS}$					
C10	GPIC5			GPOC5	HD13	
C11	GPIC1			GPOC1	HD9	
C12	reserved				HD3	
C13	NC					
C14	NC					
C15	NC					
C16	NC					
C17	NC					
C18	NC					
C19	NC					
C20	NC					
D1	V_{DDM}					
D2	D28					
D3	D27					
D4	GND					
D5	V_{DDM}					
D6	V_{DDM}					
D7	V_{DDM}					
D8	V_{DDM}					
D9	V_{DDM}					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
D10	V_{DDM}					
D11	V_{DDIO}					
D12	V_{DDIO}					
D13	V_{DDIO}					
D14	V_{DDIO}					
D15	V_{DDIO}					
D16	V_{DDIO}					
D17	V_{DDC}					
D18	NC					
D19	NC					
D20	NC					
E1	GND					
E2	D26					
E3	D31					
E4	V_{DDM}					
E5	V_{DDM}					
E6	V_{DDC}					
E7	V_{DDC}					
E8	V_{DDC}					
E9	V_{DDC}					
E10	V_{DDM}					
E11	V_{DDIO}					
E12	V_{DDIO}					
E13	V_{DDIO}					
E14	V_{DDIO}					
E15	V_{DDIO}					
E16	V_{DDC}					
E17	V_{DDC}					
E18	NC					
E19	NC					
E20	NC					
F1	V_{DDM}					
F2	D15					
F3	D29					
F4	V_{DDC}					
F5	V_{DDC}					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
H2	D12					
H3	D11					
H4	V_{DDM}					
H5	V_{DDM}					
H6	GND					
H7	GND					
H8	GND					
H9	GND					
H10	GND					
H11	GND					
H12	GND					
H13	GND					
H14	GND					
H15	V_{DDIO}					
H16	V_{DDIO}					
H17	V_{DDC}					
H18	NC					
H19	reserved				HA2	
H20	reserved				HA1	
J1	D10					
J2	V_{DDM}					
J3	D9					
J4	V_{DDM}					
J5	V_{DDM}					
J6	V_{DDM}					
J7	GND					
J8	GND					
J9	GND					
J10	GND					
J11	GND					
J12	GND					
J13	GND					
J14	GND					
J15	GND					
J16	V_{DDIO}					
J17	V_{DDC}					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
L14	V_{DDIO}					
L15	V_{DDIO}					
L16	V_{DDIO}					
L17	V_{DDC}					
L18	GPIB11			GPOB11	$\overline{\text{HCS2}}$/HCS2	
L19	reserved				$\overline{\text{HCS1}}$/HCS1	
L20	reserved				HRW or $\overline{\text{HRD}}$/HRD	
M1	D2					
M2	V_{DDM}					
M3	D5					
M4	V_{DDM}					
M5	V_{DDM}					
M6	GND					
M7	GND					
M8	GND					
M9	GND					
M10	GND					
M11	GND					
M12	GND					
M13	GND					
M14	GND					
M15	GND					
M16	V_{DDC}					
M17	V_{DDC}					
M18	GPIA14		$\overline{\text{IRQ15}}$	GPOA14	SDA	
M19	GPIA12		$\overline{\text{IRQ3}}$	GPOA12	UTXD	
M20	GPIA13		$\overline{\text{IRQ2}}$	GPOA13	URXD	
N1	D4					
N2	D6					
N3	V_{REF}					
N4	V_{DDM}					
N5	V_{DDM}					
N6	V_{DDM}					
N7	GND					
N8	GND					
N9	GND					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
N10	GND					
N11	GND					
N12	GND					
N13	GND					
N14	GND					
N15	V_{DDIO}					
N16	V_{DDC}					
N17	V_{DDC}					
N18	CLKIN					
N19	GPIA15		$\overline{IRQ14}$	GPOA15	SCL	
N20	V_{SSPLL}					
P1	D7					
P2	D17					
P3	D16					
P4	V_{DDM}					
P5	V_{DDM}					
P6	V_{DDM}					
P7	GND					
P8	GND					
P9	GND					
P10	GND					
P11	GND					
P12	GND					
P13	GND					
P14	GND					
P15	V_{DDIO}					
P16	V_{DDIO}					
P17	V_{DDC}					
P18	$\overline{PORESET}$					
P19	TPSEL					
P20	V_{DDPLL}					
R1	GND					
R2	D19					
R3	D18					
R4	V_{DDM}					
R5	V_{DDM}					

Table 1. MSC7118 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
R6	V_{DDM}					
R7	GND					
R8	V_{DDM}					
R9	GND					
R10	V_{DDM}					
R11	GND					
R12	GND					
R13	V_{DDIO}					
R14	GND					
R15	V_{DDIO}					
R16	V_{DDIO}					
R17	V_{DDC}					
R18	TDO					
R19	reserved				EE0/DBREQ	
R20	TEST0					
T1	V_{DDM}					
T2	D20					
T3	D22					
T4	V_{DDM}					
T5	V_{DDM}					
T6	V_{DDC}					
T7	V_{DDM}					
T8	V_{DDM}					
T9	V_{DDC}					
T10	V_{DDM}					
T11	V_{DDM}					
T12	V_{DDIO}					
T13	V_{DDIO}					
T14	V_{DDIO}					
T15	V_{DDIO}					
T16	V_{DDC}					
T17	V_{DDC}					
T18	reserved				MDIO	
T19	TMS					
T20	$\overline{\text{HRESET}}$					
U1	GND					

2.5.4 DDR DRAM Controller Timing

This section provides the AC electrical characteristics for the DDR DRAM interface.

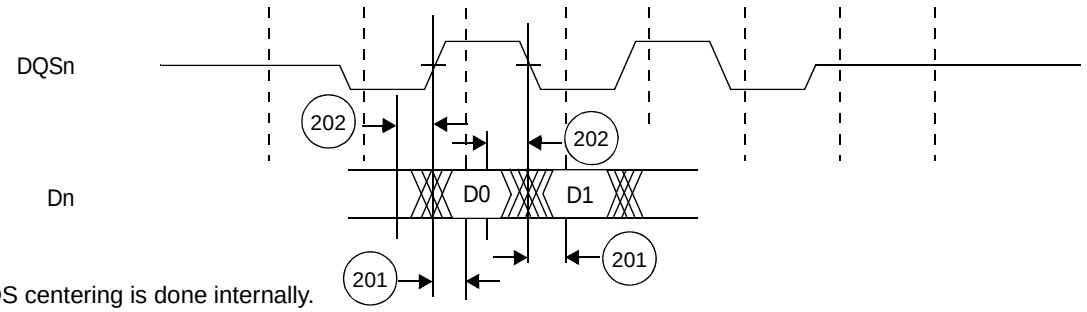
2.5.4.1 DDR DRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR DRAM interface.

Table 17. DDR DRAM Input AC Timing

No.	Parameter	Symbol	Min	Max	Unit
—	AC input low voltage	V_{IL}	—	V_{REF} – 0.31	V
—	AC input high voltage	V_{IH}	V_{REF} + 0.31	V_{DDM} + 0.3	V
201	Maximum Dn input setup skew relative to DQSn input	—	—	900	ps
202	Maximum Dn input hold skew relative to DQSn input	—	—	900	ps

Notes:
1. Maximum possible skew between a data strobe (DQSn) and any corresponding bit of data (D[8n + {0...7}] if 0 ≤ n ≤ 7).
2. See **Table 18** for t_{CK} value.
3. Dn should be driven at the same time as DQSn. This is necessary because the DQSn centering on the DQn data tenure is done internally.



Note: DQS centering is done internally.

Figure 5. DDR DRAM Input Timing Diagram

2.5.4.2 DDR DRAM Output AC Timing Specifications

Table 18 and **Table 19** list the output AC timing specifications and measurement conditions for the DDR DRAM interface.

Table 18. DDR DRAM Output AC Timing

No.	Parameter	Symbol	Min	Max	Unit
200	CK cycle time, (CK/$\overline{CK}$ crossing)[1] • 100 MHz (DDR200) • 150 MHz (DDR300)	t_{CK}	 10 6.67	 — —	 ns ns
204	An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE output setup with respect to CK	t_{DDKHAS}	0.5 × t_{CK} – 1000	—	ps
205	An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE output hold with respect to CK	t_{DDKHAX}	0.5 × t_{CK} – 1000	—	ps
206	$\overline{CSn}$ output setup with respect to CK	t_{DDKHCS}	0.5 × t_{CK} – 1000	—	ps
207	$\overline{CSn}$ output hold with respect to CK	t_{DDKHCX}	0.5 × t_{CK} – 1000	—	ps
208	CK to DQSn[2]	t_{DDKHMH}	–600	600	ps

2.5.6 HDI16 Signals

Table 21. Host Interface (HDI16) Timing[1, 2]

No.	Characteristics[3]	Expression	Value	Unit
40	Host Interface Clock period	T_{CORE}	Note 1	ns
44a	Read data strobe minimum assertion width[4] HACK read minimum assertion width	$2.0 \times T_{CORE} + 9.0$	Note 11	ns
44b	Read data strobe minimum deassertion width[4] HACK read minimum deassertion width	$1.5 \times T_{CORE}$	Note 11	ns
44c	Read data strobe minimum deassertion width[4] after “Last Data Register” reads[5,6], or between two consecutive CVR, ICR, or ISR reads[7] HACK minimum deassertion width after “Last Data Register” reads[5,6]	$2.5 \times T_{CORE}$	Note 11	ns
45	Write data strobe minimum assertion width[8] HACK write minimum assertion width	$1.5 \times T_{CORE}$	Note 11	ns
46	Write data strobe minimum deassertion width[8] HACK write minimum deassertion width after ICR, CVR and Data Register writes[5]	$2.5 \times T_{CORE}$	Note 11	ns
47	Host data input minimum setup time before write data strobe deassertion[8] Host data input minimum setup time before HACK write deassertion	—	2.5	ns
48	Host data input minimum hold time after write data strobe deassertion[8] Host data input minimum hold time after HACK write deassertion	—	2.5	ns
49	Read data strobe minimum assertion to output data active from high impedance[4] HACK read minimum assertion to output data active from high impedance	—	1.0	ns
50	Read data strobe maximum assertion to output data valid[4] HACK read maximum assertion to output data valid	$(2.0 \times T_{CORE}) + 8.0$	Note 11	ns
51	Read data strobe maximum deassertion to output data high impedance[4] HACK read maximum deassertion to output data high impedance	—	9.0	ns
52	Output data minimum hold time after read data strobe deassertion[4] Output data minimum hold time after HACK read deassertion	—	1.0	ns
53	HCS[1–2] minimum assertion to read data strobe assertion[4]	—	0.5	ns
54	HCS[1–2] minimum assertion to write data strobe assertion[8]	—	0.0	ns
55	HCS[1–2] maximum assertion to output data valid	$(2.0 \times T_{CORE}) + 6.0$	Note 11	ns
56	HCS[1–2] minimum hold time after data strobe deassertion[9]	—	0.5	ns
57	HA[0–2], HRW minimum setup time before data strobe assertion[9]	—	5.0	ns
58	HA[0–2], HRW minimum hold time after data strobe deassertion[9]	—	5.0	ns
61	Maximum delay from read data strobe deassertion to host request deassertion for “Last Data Register” read[4, 5, 10]	$(3.0 \times T_{CORE}) + 6.0$	Note 11	ns
62	Maximum delay from write data strobe deassertion to host request deassertion for “Last Data Register” write[5,8,10]	$(3.0 \times T_{CORE}) + 6.0$	Note 11	ns
63	Minimum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) deassertion to HREQ assertion.	$(2.0 \times T_{CORE}) + 1.0$	Note 11	ns
64	Maximum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) assertion to HREQ deassertion	$(5.0 \times T_{CORE}) + 6.0$	Note 11	ns

Notes:
1. T_{CORE} = core clock period. At 300 MHz, T_{CORE} = 3.333 ns.
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. V_{DD} = 3.3 V ± 0.15 V; T_J = –40°C to +105 °C, C_L = 30 pF for maximum delay timings and C_L = 0 pF for minimum delay timings.
4. The read data strobe is HRD/HRD in the dual data strobe mode and HDS/HDS in the single data strobe mode.
5. For 64-bit transfers, the “last data register” is the register at address 0x7, which is the last location to be read or written in data transfers. This is RX0/TX0 in the little endian mode (HBE = 0), or RX3/TX3 in the big endian mode (HBE = 1).
6. This timing is applicable only if a read from the “last data register” is followed by a read from the RX[0–3] registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ/HREQ signal.
7. This timing is applicable only if two consecutive reads from one of these registers are executed.
8. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
9. The data strobe is host read (HRD/HRD) or host write (HWR/HWR) in the dual data strobe mode and host data strobe (HDS/HDS) in the single data strobe mode.
10. The host request is HREQ/HREQ in the single host request mode and HRRQ/HRRQ and HTRQ/HTRQ in the double host request mode. HRRQ/HRRQ is deasserted only when HOTX fifo is empty, HTRQ/HTRQ is deasserted only if HORX fifo is full
11. Compute the value using the expression.
12. The read and write data strobe minimum deassertion width for non-”last data register” accesses in single and dual data strobe modes is based on timings 57 and 58.

2.5.10 Event Timing

Table 25. EVNT Signal Timing

Number	Characteristics	Type	Min
67	EVNT as input	Asynchronous	1.5 × APBCLK periods
68	EVNT as output	Synchronous to core clock	1 APBCLK period

Notes:
1. Refer to **Table 23** for a definition of the APBCLK period.
2. Direction of the EVNT signal is configured through the GPIO and Event port registers.
3. Refer to the signal chapter in the *MSC711x Reference Manual* for details on EVNT pin functionality.

Figure 20 shows the signal behavior of the EVNT pins.

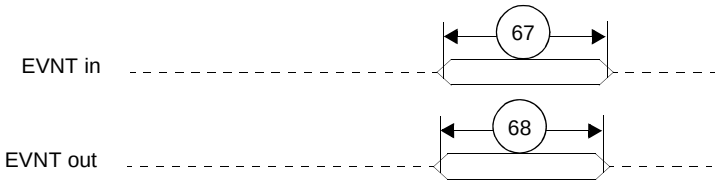


Figure 20. EVNT Pin Timing

2.5.11 GPIO Timing

Table 26. GPIO Signal Timing[1,2,3]

Number	Characteristics	Type	Min
601	GPI[4,5]	Asynchronous	1.5 × APBCLK periods
602	GPO[5]	Synchronous to core clock	1 APBCLK period
603	Port A edge-sensitive interrupt	Asynchronous	1.5 × APBCLK periods
604	Port A level-sensitive interrupt	Asynchronous	3 × APBCLK periods[6]

Notes:
1. Refer to **Table 23** for a definition of the APBCLK period.
2. Direction of the GPIO signal is configured through the GPIO port registers.
3. Refer to **Section 1.5** for details on GPIO pin functionality.
4. GPI data is synchronized to the APBCLK internally and the minimum listed is the capability of the hardware to capture data into a register when the GPADR is read. The specification is not tested due to the asynchronous nature of the input and dependence on the state of the DSP core. It is guaranteed by design.
5. The output signals cannot toggle faster than 75 MHz.
6. Level-sensitive interrupts should be held low until the system determines (via the service routine) that the interrupt is acknowledged.

Figure 21 shows the signal behavior of the GPI/GPO pins.

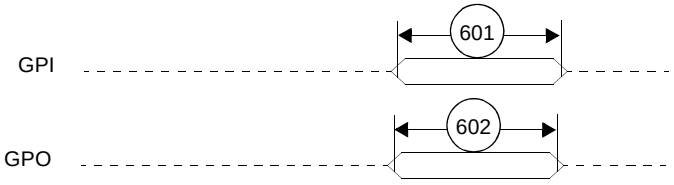


Figure 21. GPI/GPO Pin Timing

3.2 Power Supply Design Considerations

This section outlines the MSC7118 power considerations: power supply, power sequencing, power planes, decoupling, power supply filtering, and power consumption. It also presents a recommended power supply design and options for low-power consumption. For information on AC/DC electrical specifications and thermal characteristics, refer to **Section 2**.

3.2.1 Power Supply

The MSC7118 requires four input voltages, as shown in **Table 28**.

Table 28. MSC7118 Voltages

Voltage	Symbol	Value
Core	V_{DDC}	1.2 V
Memory	V_{DDM}	2.5 V
Reference	V_{REF}	1.25 V
I/O	V_{DDIO}	3.3 V

You should supply the MSC7118 core voltage via a variable switching supply or regulator to allow for compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied with 1.2 V (+5% and –10%) across V_{DDC} and GND and the I/O section is supplied with 3.3 V (± 10%) across V_{DDIO} and GND. The memory and reference voltages supply the DDR memory controller block. The memory voltage is supplied with 2.5 V across V_{DDM} and GND. The reference voltage is supplied across V_{REF} and GND and must be between $0.49 \times V_{DDM}$ and $0.51 \times V_{DDM}$. Refer to the JEDEC standard JESD8 (*Stub Series Terminated Logic for 2.5 Volts* (STTL_2)) for memory voltage supply requirements.

3.2.2 Power Sequencing

One consequence of multiple power supplies is that the voltage rails ramp up at different rates when power is initially applied. The rates depend on the power supply, the type of load on each power supply, and the way different voltages are derived. It is extremely important to observe the power up and power down sequences at the board level to avoid latch-up, forward biasing of ESD devices, and excessive currents, which all lead to severe device damage.

Note: There are five possible power-up/power-down sequence cases. The first four cases listed in the following sections are recommended for new designs. The fifth case is not recommended for new designs and must be carefully evaluated for current spike risks based on actual information for the specific application.

3.2.2.1 Case 1

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) supply second.
3. Turn on the V_{DDM} (2.5 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDM} (2.5 V) supply second.
3. Turn off the V_{DDC} (1.2 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 26** for relative timing for power sequencing case 1.

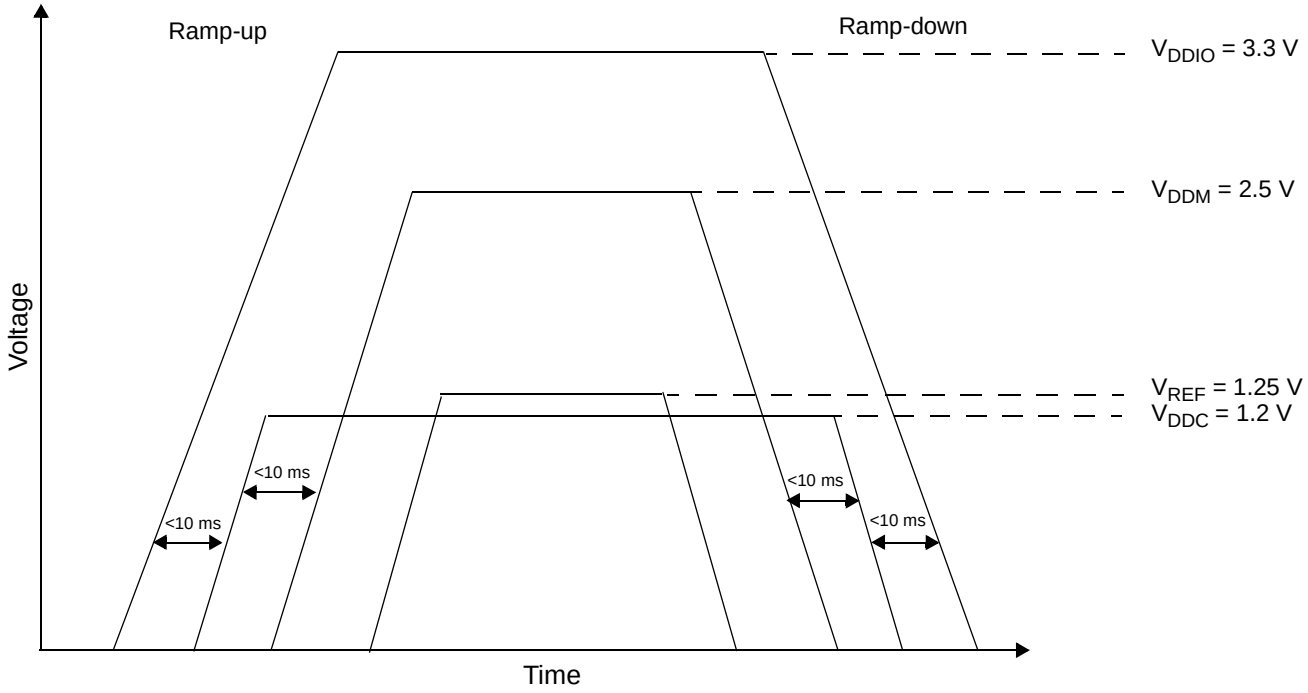


Figure 26. Voltage Sequencing Case 1

3.2.2.2 Case 2

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V) and V_{DDM} (2.5 V) supplies simultaneously (second).
3. Turn on the V_{REF} (1.25 V) supply last (third).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC}/V_{DDM} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDM} (2.5 V) supply second.
3. Turn off the V_{DDC} (1.2 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down for V_{DDIO} and V_{DDC} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 27** for relative timing for Case 2.

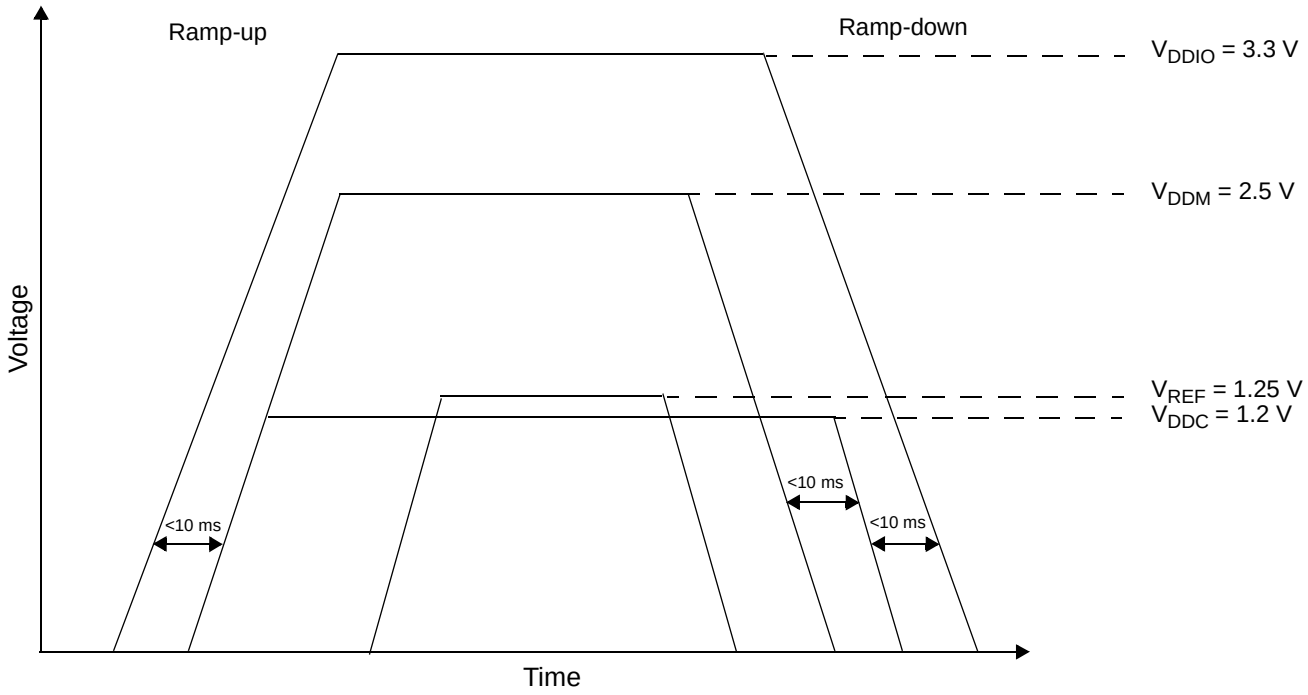


Figure 27. Voltage Sequencing Case 2

3.2.2.5 Case 5 (not recommended for new designs)

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDM} (2.5 V) supply second.
3. Turn on the V_{DDC} (1.2 V) supply third.
4. Turn on the V_{REF} (1.25 V) supply fourth (last).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDM} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{REF} (1.25 V) supply first.
2. Turn off the V_{DDC} (1.2 V) supply second.
3. Turn off the V_{DDM} (2.5 V) supply third.
4. Turn of the V_{DDIO} (3.3 V) supply fourth (last).

Use the following guidelines:

- Make sure that the time interval between the ramp-down of V_{DDIO} and V_{DDM} is less than 10 ms.
- Make sure that the time interval between the ramp-up or ramp-down for V_{DDC} and V_{DDM} is less than 2 ms for power-up and power-down.
- Refer to **Figure 30** for relative timing for power sequencing case 5.

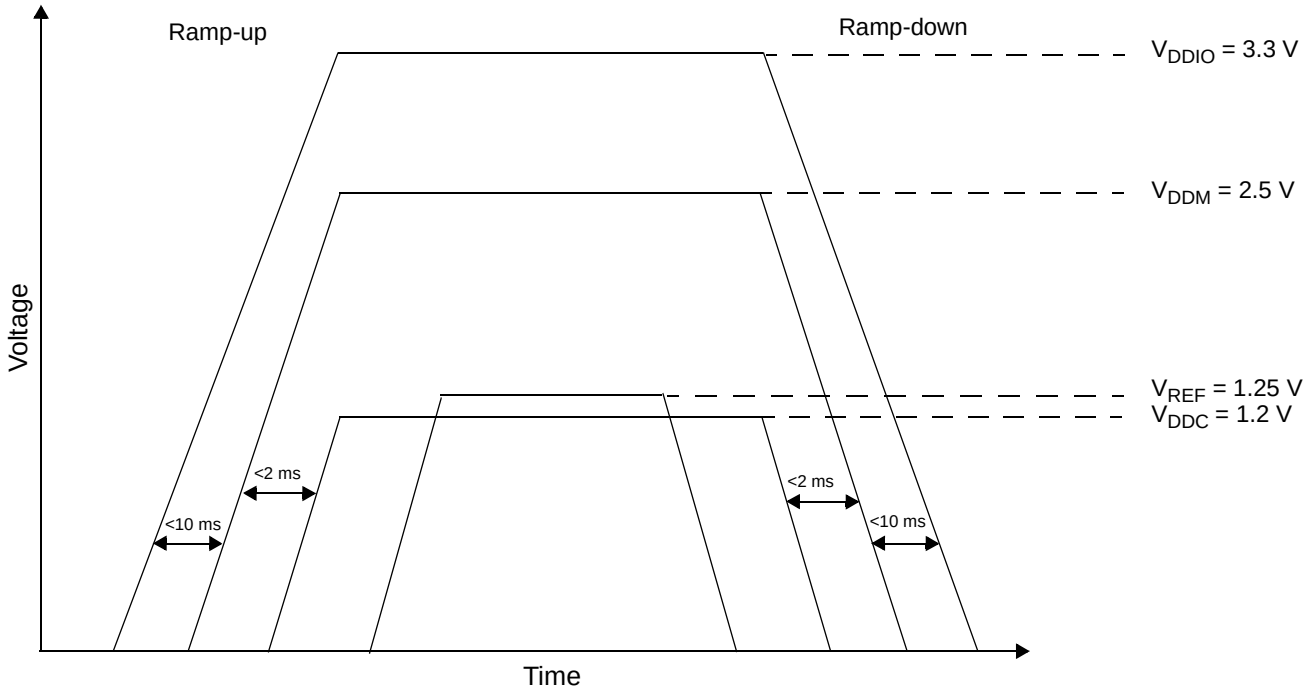


Figure 30. Voltage Sequencing Case 5

Note: Cases 1, 2, 3, and 4 are recommended for system design. Designs that use Case 5 may have large current spikes on the V_{DDM} supply at startup and is not recommended for most designs. If a design uses case 5, it must accommodate the potential current spikes. Verify risks related to current spikes using actual information for the specific application.

3.2.3 Power Planes

Each power supply pin (V_{DDC}, $V_{DDM,}$ and V_{DDIO}) should have a low-impedance path to the board power supply. Each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the device. The MSC7118 V_{DDC} power supply pins should be bypassed to ground using decoupling capacitors. The capacitor leads and associated printed circuit traces connecting to device power pins and GND should be kept to less than half an inch per capacitor lead. A minimum four-layer board that employs two inner layers as power and GND planes is recommended. See **Section 3.5** for DDR Controller power guidelines.

3.2.4 Decoupling

Both the I/O voltage and core voltage should be decoupled for switching noise. For I/O decoupling, use standard capacitor values of 0.01 µF for every two to three voltage pins. For core voltage decoupling, use two levels of decoupling. The first level should consist of a 0.01 µF high frequency capacitor with low effective series resistance (ESR) and effective series inductance (ESL) for every two to three voltage pins. The second decoupling level should consist of two bulk/tantalum decoupling capacitors, one 10 µF and one 47 µF, (with low ESR and ESL) mounted as closely as possible to the MSC7118 voltage pins. Additionally, the maximum drop between the power supply and the DSP device should be 15 mV at 1 A.

3.2.5 PLL Power Supply Filtering

The MSC7118 V_{DDPLL} power signal provides power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to this pin should be filtered with capacitors that have low and high frequency filtering characteristics. V_{DDPLL} can be connected to V_{DDC} through a 2 Ω resistor. V_{SSPLL} can be tied directly to the GND plane. A circuit similar to the one shown in **Figure 31** is recommended. The PLL loop filter should be placed as closely as possible to the V_{DDPLL} pin (which are located on the outside edge of the silicon package) to minimize noise coupled from nearby circuits.The 0.01 µF capacitor should be closest to V_{DDPLL}, followed by the 0.1 µF capacitor, the 10 µF capacitor, and finally the 2-Ω resistor to V_{DDC}. These traces should be kept short.

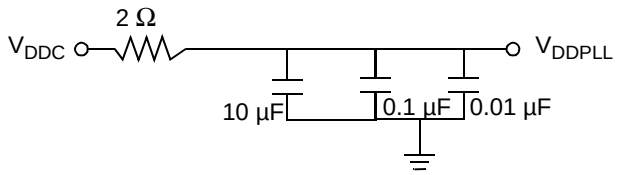


Figure 31. PLL Power Supply Filter Circuits

3.2.6 Power Consumption

You can reduce power consumption in your design by controlling the power consumption of the following regions of the device:

- *Extended core.* Use the SC1400 Stop and Wait modes by issuing a **stop** or **wait** instruction.
- *Clock synthesis module.* Disable the PLL, timer, watchdog, or DDR clocks or disable the CLKO pin.
- *AHB subsystem.* Freeze or shut down the AHB subsystem using the GPSCTL[XBR_HRQ] bit.
- *Peripheral subsystem.* Halt the individual on-device peripherals such as the DDR memory controller, HDI16, TDM, UART, I^2C, and timer modules.

For details, see the “Clocks and Power Management” chapter of the *MSC711x Reference Manual*.

3.3.6 Example Total Power Consumption

Using the examples in this section and assuming four peripherals and 10 I/O lines active, a total power consumption value is estimated as the following:

$$P_{TOTAL} = 324.0 + (4 \times 4.32) + 326.3 + (10 \times 5.44) + 64 = 784.98\ mW \qquad \text{Eqn. 13}$$

3.4 Reset and Boot

This section describes the recommendations for configuring the MSC7118 at reset and boot.

3.4.1 Reset Circuit

$\overline{\text{HRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. For an open-drain output such as $\overline{\text{HRESET}}$, take care when driving many buffers that implement input bus-hold circuitry. The bus-hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MSC7118 output current, the pull-up value should not be too small (a 1 KΩ pull-up resistor is used in the MSC711xADS reference design).

3.4.2 Reset Configuration Pins

Table 30 shows the MSC7118 reset configuration signals. These signals are sampled at the deassertion (rising edge) of $\overline{\text{PORESET}}$. For details, refer to the Reset chapter of the *MSC711x Reference Manual*.

Table 30. Reset Configuration Signals

Signal	Description	Settings
BM[3–0]	Determines boot mode.	See **Table 31** for details.
SWTE	Determines watchdog functionality.	0 Watchdog timer disabled. 1 Watchdog timer enabled.
HDSP	Configures HDI16 strobe polarity.	0 Host Data strobes active low. 1 Host Data strobes active high.
H8BIT	Configures HDI16 operation mode.	0 HDI16 port configured for 16-bit operation. 1 HDI16 port configured for 8-bit operation.

3.6 Connectivity Guidelines

This section summarizes the connections and special conditions, such as pull-up or pull-down resistors, for the MSC7118 device. Following are guidelines for signal groups and configuration settings:

- *Clock and reset signals*.
  - SWTE is used to configure the MSC7118 device and is sampled on the deassertion of $\overline{\text{PORESET}}$, so it should be tied to V_{DDC} or GND either directly or through pull-up or pull-down resistors until $\overline{\text{PORESET}}$ is deasserted. After $\overline{\text{PORESET}}$, this signal can be left floating.
  - BM[0–1] configure the MSC7118 device and are sampled until $\overline{\text{PORESET}}$ is deasserted, so they should be tied to V_{DDIO} or GND either directly or through pull-up or pull-down resistors.
  - $\overline{\text{HRESET}}$ should be pulled up.
- *Interrupt signals*. When used, $\overline{\text{IRQ}}$ pins must be pulled up.
- *HDI16 signals*.
  - When they are configured for open-drain, the $\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ signals require a pull-up resistor. However, these pins are also sampled at power-on reset to determine the HDI16 boot mode and may need to be pulled down. When these pins must be pulled down on reset and pulled up otherwise, a buffer can be used with the $\overline{\text{HRESET}}$ signal as the enable.
  - When the device boots through the HDI16, the HDDS, HDSP and H8BIT pins should be pulled up or down, depending on the required boot mode settings.
- *I^2C signals*. The SCL and SDA signals, when programmed for I^2C, requires an external pull-up resistor.
- *General-purpose I/O (GPIO) signals*. An unused GPIO pin can be disconnected. After boot, program it as an output pin.
- Other signals.
  - The $\overline{\text{TEST0}}$ pin must be connected to ground.
  - The $\overline{\text{TPSEL}}$ pin should be pulled up to enable debug access via the EOnCE port and pulled down for boundary scan.
  - Pins labelled NO CONNECT (NC) must not be connected.
  - When a 16-pin double data rate (DDR) interface is used, the 16 unused data pins should be no connects (floating) if the used lines are terminated.
  - Do not connect DBREQ to DONE (as you would for the MSC8101 device). Connect DONE to one of the EVNT pins, and DBREQ to HRRQ.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
MSC7118	1.2 V core 2.5 V memory 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	400	300	Lead-free	MSC7118VM1200
					Lead-bearing	MSC7118VF1200