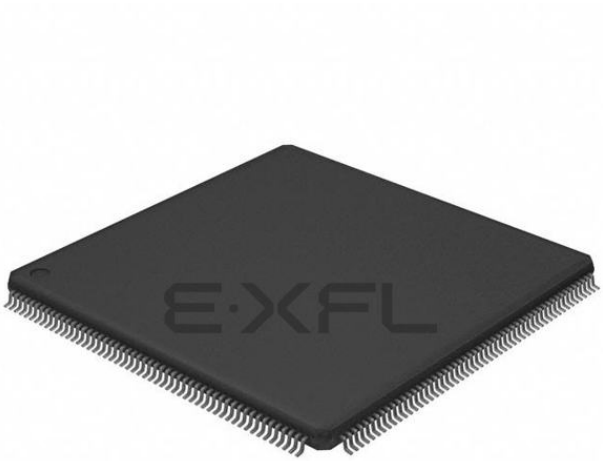

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	142
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1850fbd208-551

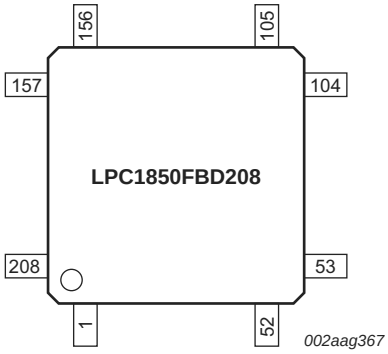


Fig 5. Pin configuration LQFP208 package

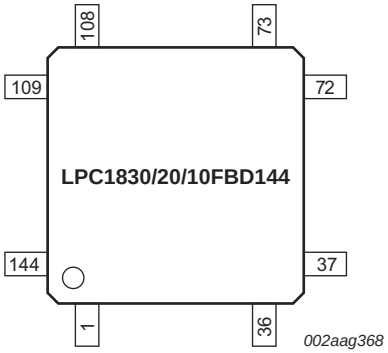


Fig 6. Pin configuration LQFP144 package

6.2 Pin description

On the LPC1850/30/20/10, digital pins are grouped into 16 ports, named P0 to P9 and PA to PF, with up to 20 pins used per port. Each digital pin can support up to eight different digital functions, including General-Purpose I/O (GPIO), selectable through the System Configuration Unit (SCU) registers. The pin name is not indicative of the GPIO port assigned to it.

Not all functions listed in Table 3 are available on all packages. See Table 2 for availability of USB0, USB1, Ethernet, and LCD functions.

Table 3. Pin description

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
Multiplexed digital pins									
P0_0	L3	K3	G2	47	32	[2]	N; PU	I/O	**GPIO0[0] —** General purpose digital input/output pin.
								I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
								I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
								I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
P0_1	M2	K2	G1	50	34	[2]	N; PU	I/O	**GPIO0[1] —** General purpose digital input/output pin.
								I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
								I	**ENET_COL —** Ethernet Collision detect (MII interface).
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
									ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
								I/O	**I2S1_TX_SDA —** I²S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
P1_0	P2	L1	H1	54	38	[2]	N; PU	I/O	**GPIO0[4] —** General purpose digital input/output pin.
								I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
								I/O	**EMC_A5 —** External memory address line 5.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								I/O	**SSP0_SSEL —** Slave Select for SSP0.
								-	**R —** Function reserved.
								-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P1_8	R7	M5	H5	71	51	[2]	N; PU	I/O	**GPIO1[1] —** General purpose digital input/output pin.
								O	**U1_DTR —** Data Terminal Ready output for UART1.
								O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
								I/O	**EMC_D1 —** External memory data line 1.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								O	**SD_VOLT0 —** SD/MMC bus voltage select output 0.
P1_9	T7	N5	J5	73	52	[2]	N; PU	I/O	**GPIO1[2] —** General purpose digital input/output pin.
								O	**U1_RTS —** Request to Send output for UART1.
								O	**CTOUT_11 —** SCT output 11. Match output 3 of timer 2.
								I/O	**EMC_D2 —** External memory data line 2.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								I/O	**SD_DAT0 —** SD/MMC data bus line 0.
P1_10	R8	N6	H6	75	53	[2]	N; PU	I/O	**GPIO1[3] —** General purpose digital input/output pin.
								I	**U1_RI —** Ring Indicator input for UART1.
								O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
								I/O	**EMC_D3 —** External memory data line 3.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								I/O	**SD_DAT1 —** SD/MMC data bus line 1.
P1_11	T9	P8	J7	77	55	[2]	N; PU	I/O	**GPIO1[4] —** General purpose digital input/output pin.
								I	**U1_CTS —** Clear to Send input for UART1.
								O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
								I/O	**EMC_D4 —** External memory data line 4.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								I/O	**SD_DAT2 —** SD/MMC data bus line 2.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P5_6	T13	M11	-	89	63	[2]	N; PU	I/O	**GPIO2[15] —** General purpose digital input/output pin.
								O	**MCOB1 —** Motor control PWM channel 1, output B.
								I/O	**EMC_D10 —** External memory data line 10.
								-	**R —** Function reserved.
								O	**U1_TXD —** Transmitter output for UART1.
								O	**T1_MAT2 —** Match output 2 of timer 1.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
P5_7	R12	N11	-	91	65	[2]	N; PU	I/O	**GPIO2[7] —** General purpose digital input/output pin.
								O	**MCOA2 —** Motor control PWM channel 2, output A.
								I/O	**EMC_D11 —** External memory data line 11.
								-	**R —** Function reserved.
								I	**U1_RXD —** Receiver input for UART1.
								O	**T1_MAT3 —** Match output 3 of timer 1.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
P6_0	M12	M10	H7	105	73	[2]	N; PU	-	**R —** Function reserved.
								O	**I2S0_RX_MCLK —** I^2S receive master clock.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								I/O	**I2S0_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
P6_1	R15	P14	G5	107	74	[2]	N; PU	I/O	**GPIO3[0] —** General purpose digital input/output pin.
								O	**$\overline{\text{EMC\_DYCS1}}$ —** SDRAM chip select 1.
								I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
								I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
								-	**R —** Function reserved.
								I	**T2_CAP0 —** Capture input 2 of timer 2.
								-	**R —** Function reserved.
								-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P7_4	C8	C6	-	189	132	[5]	N; PU	I/O	**GPIO3[12] —** General purpose digital input/output pin.
								O	**CTOUT_13 —** SCT output 13. Match output 3 of timer 3.
								-	**R —** Function reserved.
								O	**LCD_VD16 —** LCD data.
								O	**LCD_VD4 —** LCD data.
								O	**TRACEDATA[0] —** Trace data, bit 0.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								AI	**ADC0_4 —** ADC0 and ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_5	A7	A7	-	191	133	[5]	N; PU	I/O	**GPIO3[13] —** General purpose digital input/output pin.
								O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
								-	**R —** Function reserved.
								O	**LCD_VD8 —** LCD data.
								O	**LCD_VD23 —** LCD data.
								O	**TRACEDATA[1] —** Trace data, bit 1.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								AI	**ADC0_3 —** ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_6	C7	F5	-	194	134	[2]	N; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
								O	**CTOUT_11 —** SCT output 1. Match output 3 of timer 2.
								-	**R —** Function reserved.
								O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
								-	**R —** Function reserved.
								O	**TRACEDATA[2] —** Trace data, bit 2.
								-	**R —** Function reserved.
								-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PF_6	E7	-	-	192	-	[5]	N; PU	-	**R —** Function reserved.
								I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
								I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
								O	**TRACEDATA[1] —** Trace data, bit 1.
								I/O	**GPIO7[20] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								I/O	**I2S1_TX_SDA —** I^2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
								AI	**ADC1_3 —** ADC1 and ADC0, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_7	B7	-	-	193	-	[5]	N; PU	-	**R —** Function reserved.
								I/O	**U3_BAUD —** Baud pin USART3.
								I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
								O	**TRACEDATA[2] —** Trace data, bit 2.
								I/O	**GPIO7[21] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
								AI/O	**ADC1_7 —** ADC1 and ADC0, input channel 7 or band gap output. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_8	E6	-	-	-	-	[5]	N; PU	-	**R —** Function reserved.
								I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
								I	**CTIN_2 —** SCT input 2. Capture input 2 of timer 0.
								O	**TRACEDATA[3] —** Trace data, bit 3.
								I/O	**GPIO7[22] —** General purpose digital input/output pin.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								-	**R —** Function reserved.
								AI	**ADC0_2 —** ADC0 and ADC1, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP208	LQFP144	Reset state [1]	Type	Description
VSSA	B2	A3	C2	196	135	-	-	Analog ground.
Not connected								
-	B9	B8	-	-	-	-	-	n.c.

[1] N = neutral, input buffer disabled; no extra VDDIO current consumption if the input is driven midway between supplies; set the EZI bit in the SFS register to enable the input buffer; I = input; OL = output driving LOW; OH = output driving HIGH; AI/O = analog input/output; IA = inactive; PU = pull-up enabled (weak pull-up resistor pulls up pin to VDDIO; F = floating. Reset state reflects the pin state at reset without boot code operation.

[2] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength (see Figure 45).

[3] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels, and hysteresis; high drive strength (see Figure 45).

[4] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides high-speed digital I/O functions with TTL levels and hysteresis (see Figure 45).

[5] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input or output (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V). When configured as an ADC input or DAC output, the pin is not 5 V tolerant and the digital section of the pad must be disabled by setting the pin to an input function and disabling the pull-up resistor through the pin's SFSP register.

[6] 5 V tolerant transparent analog pad.

[7] For maximum load C_L = 6.5 μF and maximum pull-down resistance R_{pd} = 80 kΩ, the VBUS signal takes about 2 s to fall from VBUS = 5 V to VBUS = 0.2 V when it is no longer driven.

[8] Transparent analog pad. Not 5 V tolerant.

[9] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only).

[10] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus Fast Mode Plus specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines.

[11] 5 V tolerant pad with 20 ns glitch filter; provides digital I/O functions with open-drain output with weak pull-up resistor and hysteresis (see Figure 46).

[12] If not pinned out, VPP is internally connected to VDDIO.

[13] On the TFBGA100 and LQFP208 packages, VSS is internally connected to VSSIO.

7.11 One-Time Programmable (OTP) memory

The OTP provides 32 bit of memory for general-purpose use.

7.12 General-Purpose I/O (GPIO)

The LPC1850/30/20/10 provides eight GPIO ports with up to 31 GPIO pins each.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

All GPIO pins default to inputs with pull-up resistors enabled and input buffer disabled on reset. The input buffer must be turned on in the system control block SFS register before the GPIO input can be read.

7.12.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request.
- Two GPIO group interrupts can be triggered by any pin or pins in each port.

7.13 AHB peripherals

7.13.1 State Configurable Timer (SCT) subsystem

The SCT allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCT are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCT can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of Match/Capture registers, plus reload or capture control values

In the two-counter case, the following operational elements are global to the SCT, but the last three can use match conditions from either counter:

- MultiMedia Cards (MMC version 4.4)

7.13.5 External Memory Controller (EMC)

The LPC1850/30/20/10 EMC is a Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and NOR flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals.

7.13.5.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and NOR flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines-wide static memory support. On parts LPC1820/10 only 8/16 data lines are available.
- 16-bit and 32-bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKEOUT and EMC_CLK signals to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. Those are typically 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.13.6 High-speed USB Host/Device/OTG interface (USB0)

Remark: USB0 is available on parts LPC1850/30/20 (see Table 2).

The USB OTG module allows the part to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode.

7.13.6.1 Features

- On-chip UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.

- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock can be generated from the peripheral clock, or from a clock input pin.

7.13.9 Ethernet

Remark: Ethernet is available on parts LPC1850/30 (see Table 2).

7.13.9.1 Features

- 10/100 Mbit/s
- DMA support
- Power management remote wake-up frame and magic packet detection
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Support for IEEE 1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

- Smart card mode conforming to ISO7816 specification

7.14.3 SSP serial I/O controller

Remark: The LPC1850/30/20/10 contain two SSP controllers.

The SSP controller can operate on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full-duplex transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.14.3.1 Features

- Maximum SSP speed in full-duplex mode of 25 Mbit/s; for transmit only 50 Mbit/s (master) and 15 Mbit/s (slave).
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- Eight-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- Connected to the GPDMA

7.14.4 I^2C-bus interface

Remark: The LPC1850/30/20/10 contain two I^2C-bus interfaces.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.14.4.1 Features

- I^2C0 is a standard I^2C-compliant bus interface with open-drain pins. I^2C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I^2C1 uses standard I/O pins with bit rates of up to 400 kbit/s (Fast I^2C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.

7.18.3 Clock Generation Unit (CGU)

The Clock Generator Unit (CGU) generates several base clocks. The base clocks can be unrelated in frequency and phase and can have different clock sources within the CGU. One CGU base clock is routed to the CLKOUT pins. The base clock that generates the CPU clock is referred to as CCLK.

Multiple branch clocks are derived from each base clock. The branch clocks offer flexible control for power-management purposes. All branch clocks are outputs of one of two Clock Control Units (CCUs) and can be controlled independently. Branch clocks derived from the same base clock are synchronous in frequency and phase.

7.18.4 Internal RC oscillator (IRC)

The IRC is used as the clock source for the WWDT and/or as the clock that drives the PLLs and the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC1850/30/20/10 use the IRC as the clock source. The boot loader then configures the PLL1 to provide a 96 MHz clock for the core and the PLL0USB or PLL0AUDIO as needed if an external boot source is selected.

7.18.5 PLL0USB (for USB0)

PLL0 is a dedicated PLL for the USB0 High-speed controller.

PLL0 accepts an input clock frequency from an external oscillator in the range of 14 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The CCO operates in the range of 4.3 MHz to 550 MHz.

7.18.6 PLL0AUDIO (for audio)

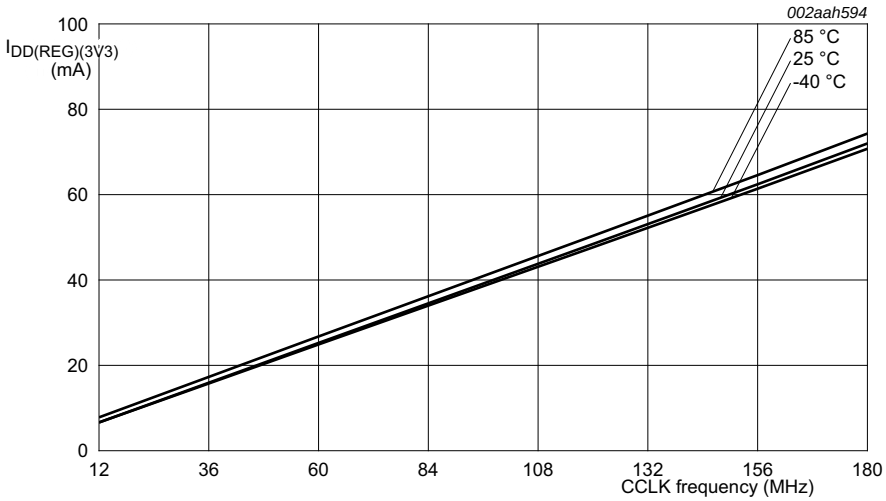
The audio PLL PLL0AUDIO is a general-purpose PLL with a small step size. This PLL accepts an input clock frequency derived from an external oscillator or internal IRC. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). A sigma-delta converter modulates the PLL divider ratios to obtain the desired output frequency. The output frequency can be set as a multiple of the sampling frequency f_s to $32 \times f_s$, $64 \times f_s$, $128 \times f_s$, $256 \times f_s$, $384 \times f_s$, $512 \times f_s$ and the sampling frequency f_s can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96,192) kHz. Many other frequencies are possible as well using the integrated fractional divider.

7.18.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

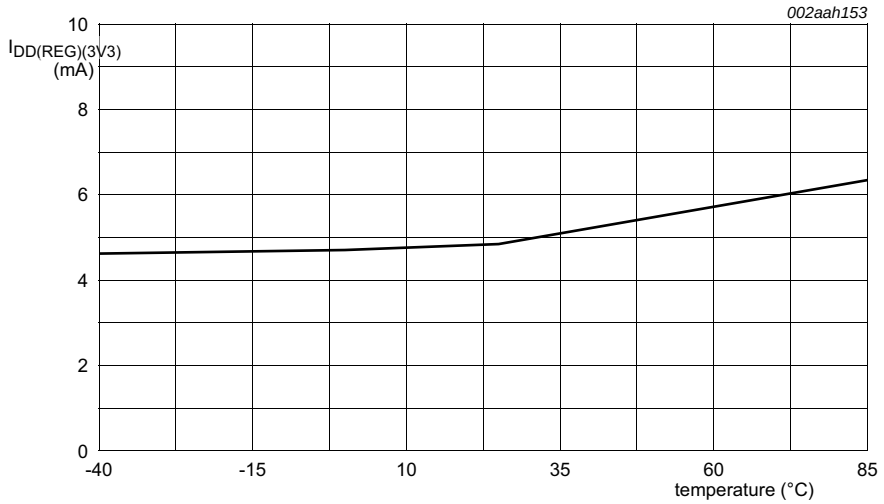
Table 10. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I/O pins - high drive strength: standard drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	32	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	32	mA
I/O pins - high drive strength: medium drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	65	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	63	mA
I/O pins - high drive strength: high drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−14	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		14	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	113	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	110	mA
I/O pins - high drive strength: ultra-high drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−20	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4$ V		20	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	165	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	156	mA
I/O pins - high-speed							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	$V_I = 0$ V; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		$V_I = 5$ V		-	1	-	nA



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; Active mode entered executing code while(1){} from SRAM; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 13. Typical supply current versus frequency in Active mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled; core clock CCLK = 12 MHz.

Fig 14. Typical supply current versus temperature in Sleep mode

11.10 External memory interface

Table 23. Dynamic characteristics: Static asynchronous external memory interface

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design. Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted resulting in multiple memory accesses.

Symbol	Parameter[1]	Conditions		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time			−3.1	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		[2]	−0.6 + $T_{cy(clk)}$ × WAITOEN	-	1.3 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1		−0.7	-	1.8	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		[2]	−0.6 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time			-	-	−16 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	ns
$t_{h(D)}$	data input hold time			−16	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1		−0.4	-	1.9	ns
t_{CSHOEH}	CS HIGH to $\overline{OE}$ HIGH time			−0.4	-	1.4	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid	PB = 1		−2.0	-	2.6	ns
t_{CSHEOR}	$\overline{CS}$ HIGH to end of read time		[3]	−2.0	-	0	ns
t_{CSLSOR}	$\overline{CS}$ LOW to start of read time		[4]	0	-	1.8	ns
Write cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time			−3.1	-	1.6	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time			−3.1	-	1.5	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	PB = 1		−1.5	-	0.2	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1		−0.7	-	1.8	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	PB = 1	[2]	−0.6 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	PB = 1	[2]	−0.9 + $T_{cy(clk)}$	-	2.3 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	PB = 1	[2] [5]	−0.4 + $T_{cy(clk)}$	-	−0.3 + $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	PB = 0		−0.7	-	1.8	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 0	[2]	−0.9 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns

11.13 SD/MMC

Table 29. Dynamic characteristics: SD/MMC

T_{amb} = −40 °C to 85 °C, 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V, C_L = 20 pF. Simulated values.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	40	-	MHz
$t_{su(D)}$	data input set-up time	on pins SD_CMD, SD_DATn as inputs	16	-	ns
$t_{h(D)}$	data input hold time	on pins SD_CMD, SD_DATn as inputs	−2		ns
$t_{d(QV)}$	data output valid delay time	on pins SD_CMD, SD_DATn as outputs		12	ns
$t_{h(Q)}$	data output hold time	on pins SD_CMD, SD_DATn as outputs	0.3	-	ns

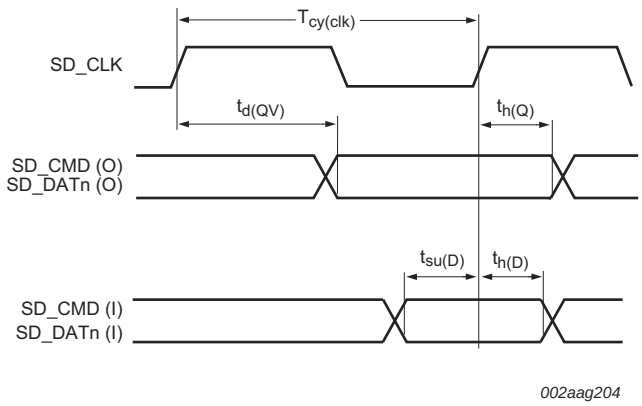


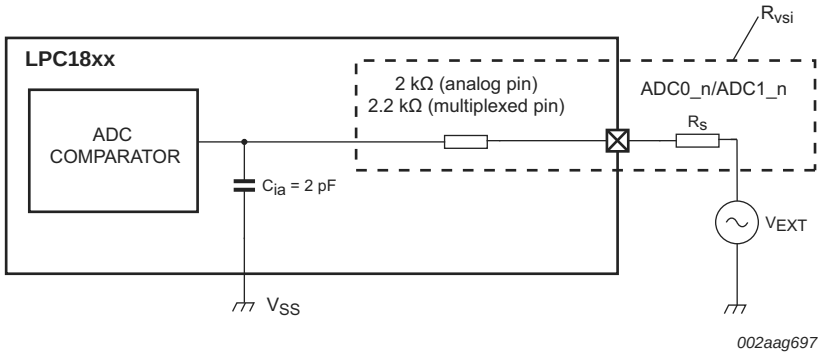
Fig 38. SD/MMC timing

11.14 LCD

Table 30. Dynamic characteristics: LCD

T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	-	MHz
$t_{d(QV)}$	data output valid delay time			-	17	ns
$t_{h(Q)}$	data output hold time		8.5	-		ns



$R_s < 1/((7 \times f_{clk(ADC)} \times C_{ia}) - 2\ k\Omega)$

Fig 41. ADC interface to pins

Table 33. DAC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	code = 0 to 975	[1]	-	±1.0	-	LSB
		2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V					
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.5	-	LSB
E_O	offset error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
E_G	gain error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.3	-	%
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	%
C_L	load capacitance			-	-	200	pF
R_L	load resistance			1	-	-	kΩ
t_s	settling time		[1]		0.4		μs

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC18xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.

Table 36. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD0	-	-	-	-	-	-	P4_1	RED0
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB /LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

13.2 Crystal oscillator

The crystal oscillator is controlled by the XTAL_OSC_CTRL register in the CGU (see *LPC18xx user manual*).

The crystal oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL.

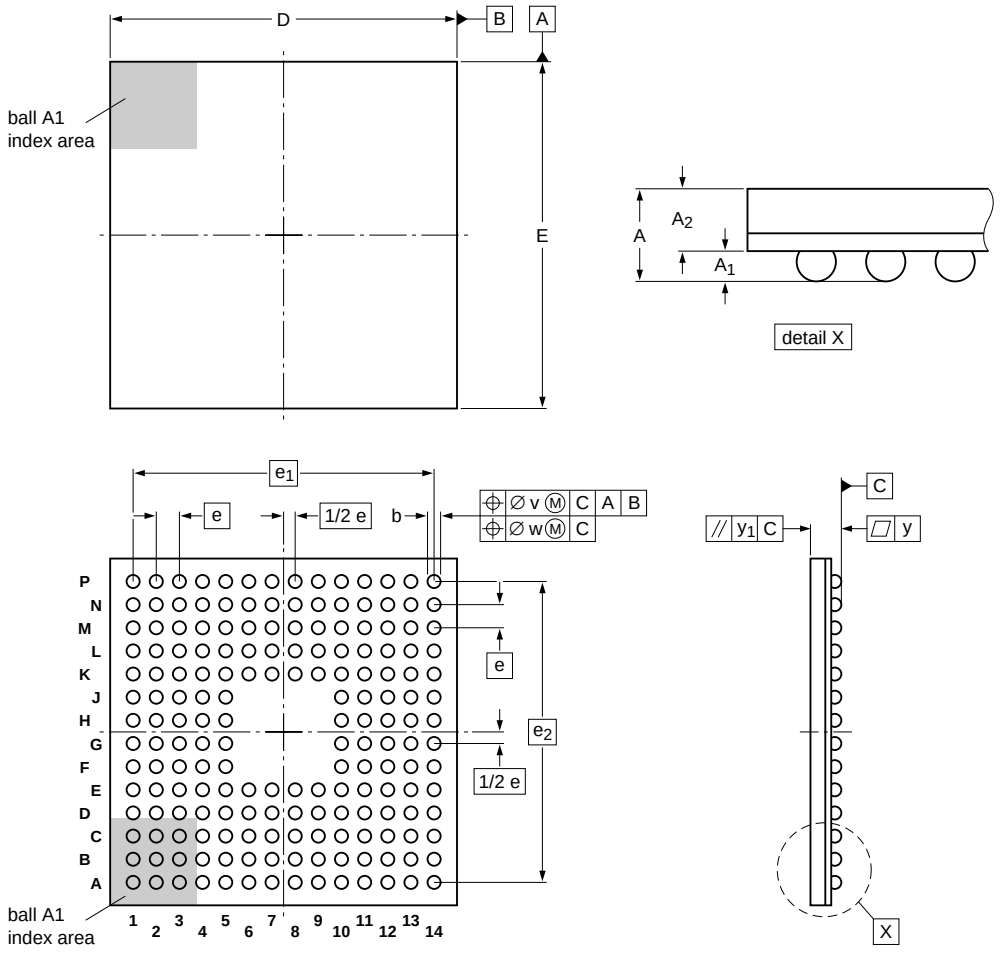
The oscillator can operate in one of two modes: slave mode and oscillation mode.

- In slave mode, couple the input clock signal with a capacitor of 100 pF (C_C in Figure 42), with an amplitude of at least 200 mV (RMS). The XTAL2 pin in this configuration can be left unconnected.
- External components and models used in oscillation mode are shown in Figure 43, and in Table 37 and Table 38. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (L, C_L and R_S represent the fundamental frequency). Capacitance C_P in Figure 43 represents the parallel package capacitance and must not be larger than 7 pF. Parameters F_C, C_L, R_S and C_P are supplied by the crystal manufacturer.

Table 37. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
2 MHz	< 200 Ω	33 pF, 33 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
4 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF
	< 200 Ω	56 pF, 56 pF
8 MHz	< 200 Ω	18 pF, 18 pF
	< 200 Ω	39 pF, 39 pF

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 48. Package outline of the TFBGA180 package

18. Revision history

Table 40. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC1850_30_20_10 v.6.1	20130207	Product data sheet	-	LPC1850_30_20_10 v.6
	• Table 13 “Band gap characteristics” and Figure 20 “Band gap voltage for different temperatures and process conditions” added. • Table 10, added Table note 2: “Dynamic characteristics for peripherals are provided for $V_{DD(REG)(3V3)} \geq 2.7$ V. • Description of ADC pins on digital/analog input pins changed. Each input to the ADC is connected to ADC0 and ADC1. See Table 3. • Use of C_CAN peripheral restricted in Section 2. • ADC channels limited to a total of 8 channels shared between ADC0 and ADC1. • Minimum value for parameter V_{IL} changed to 0 V in Table 10 “Static characteristics”. • Power consumption in active mode corrected. See parameter $I_{DD(REG)(3V3)}$ in Table 10 and graphs Figure 11, Figure 12, and Figure 13. • Parameter name $I_{DD(ADC)}$ changed to I_{DDA} in Table 10. • Added note to limit data in Table 23 “Dynamic characteristics: Static asynchronous external memory interface” to single memory accesses. • Value of parameter $I_{DD(REG)(3V3)}$ in deep power-down increased to 0.03 µA in Table 10. • Value of parameter $I_{DD(IO)}$ in deep power-down increased to 0.05 µA in Table 10.		
LPC1850_30_20_10 v.6	20121011	Product data sheet	-	LPC1850_30_20_10 v.5.2
	• Temperature range for simulated timing characteristics corrected to T_{amb} = −40 °C to +85 °C in Section 11 “Dynamic characteristics”. • SPIFI timing added. See Section 11.15. • SPIFI maximum data rate changed to 52 MB per second. • Editorial updates. • Figure 24 and Figure 25 updated for full temperature range. • The following changes were made to the TFBGA180 pinout in Table 3: – P1_13 moved from ball D6 to L8. – P7_5 moved from ball C7 to A7. – PF_4 moved from ball L8 to D6. – $\overline{\text{RESET}}$ moved from ball B7 to C7. – RTCX2 moved from ball A7 to B7. – Ball G10 changed from VSS to VDDIO. • Data sheet status changed to Product data sheet.		
LPC1850_30_20_10 v.5.2	20120904	Preliminary data sheet	-	LPC1850_30_20_10 v.5.1
	• SSP0 boot pin functions corrected in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI. • Minimum value of all supply voltages changed to −0.5 V in Table 6 “Limiting values”.			
LPC1850_30_20_10 v.5.1	20120809	Preliminary data sheet	-	LPC1850_30_20_10 v.5