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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	WDT
Number of I/O	13
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	32 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00010hec

GENERAL DESCRIPTION (Continued)

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$ (WORD is active Low, only); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

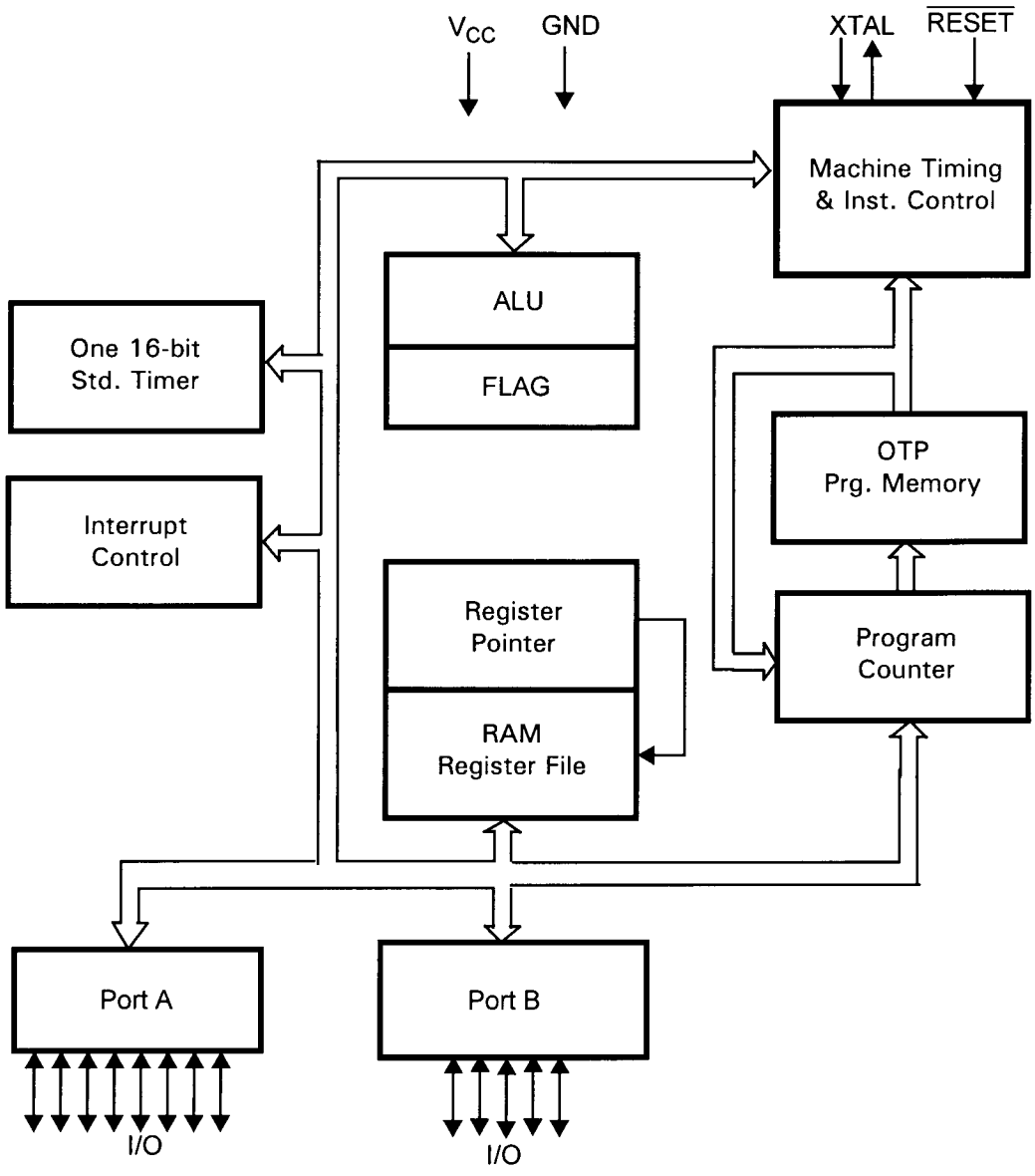


Figure 1. Functional Block Diagram

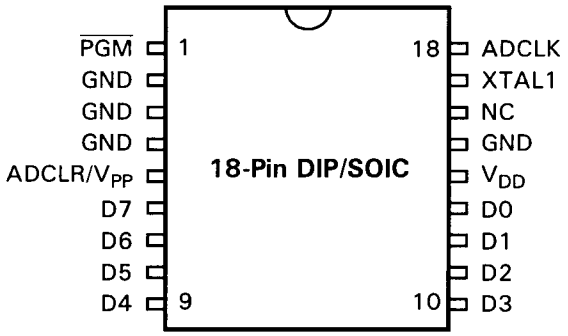


Figure 4. 18-Pin DIP/SOIC Pin Identification; EPROM Programming Mode

Table 2. 18-Pin DIP/SOIC Pin Assignments; EPROM Programmable Mode

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6–9	D7–D4	Data 7,6,5,4	In/Output
10–13	D3–D0	Data 3,2,1,0	In/Output
14	V_{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1 MHz Clock	Input
18	ADCLK	Address Clock	Input

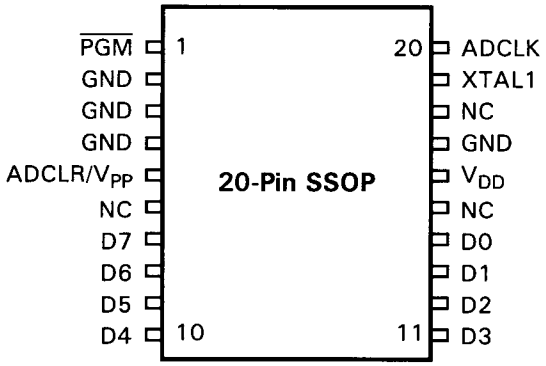


Figure 6. 20-Pin SSOP Pin Identification; EPROM Programming Mode

Table 4. 20-Pin SSOP Pin Assignments; EPROM Programming Mode

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	In/Output
11–14	D3–D0	Data 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1 MHz Clock	Input
20	ADCLK	Address Clock	Input

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on $\overline{RESET}$ Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		80	mA	
Maximum Allowable Current into V_{DD}		80	mA	
Maximum Allowable Current into an Input Pin	–600	+600	mA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	mA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	
Maximum Allowable Output Current Sourced by Port A		40	mA	
Maximum Allowable Output Current Sunk by Port B		40	mA	
Maximum Allowable Output Current Sourced by Port B		40	mA	

Notes:
1. Applies to all pins except the $\overline{RESET}$ pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. Excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

DC ELECTRICAL CHARACTERISTICS

			T_A = 0°C to +70°C					
Sym	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C[2]	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V		
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	3.5V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	3.5V		0.6	0.2	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	I_{OL} = +6 mA	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	
V_{RH}	Reset Input High Voltage	3.5V	$0.5V_{CC}$	V_{CC}	1.1	V		
		5.5V	$0.5V_{CC}$	V_{CC}	2.2	V		
V_{RL}	Reset Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.9	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.4	V		
I_{IL}	Input Leakage	3.5V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V	–10	–60	–30	µA		
		5.5V	–20	–180	–100	µA		
I_{CC}	Supply Current	3.5V		2.5	2.0	mA	@ 10 MHz	3,4
		5.5V		6.0	4.0	mA	@ 10 MHz	3,4
I_{CC1}	Standby Current	3.5V		2.0	1.0	mA	Halt Mode V_{IN} = 0V V_{CC}@10 MHz	3,4
		5.5V		6.0	4.0	mA	Halt Mode V_{IN} = 0V V_{CC}@10 MHz	3,4

Sym	Parameter	V_{CC}[1]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C[2]	Units	Conditions	Notes
I_{CC2}	Standby Current	3.5V		500	150	nA	Stop Mode V_{IN} = 0V, V_{CC}	5
		5.5V		500	250	nA	Stop Mode V_{IN} = 0V, V_{CC}	5

Notes:

1. The V_{CC} voltage specification of 3.5 V guarantees 3.5 V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
3. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
4. CL1 = CL2 = 22 pF.
5. Same as note 3 except inputs at V_{CC}.

AC ELECTRICAL CHARACTERISTICS

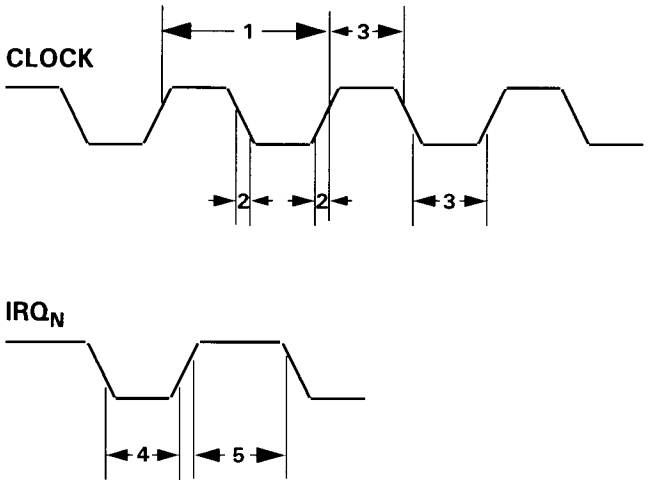


Figure 8. AC Electrical Timing Diagram

Table 5. Additional Timings

				T_A = –40°C to +105°C @ 10 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	3.5V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	TrC,TfC	Clock Input Rise and Fall Times	3.5V		15	ns	2
			5.5V		15	ns	2
3	TwC	Input Clock Width	3.5V	50		ns	2
			5.5V	50		ns	2
4	TwIL	Int. Request Input Low Time	3.5V	70		ns	2
			5.5V	70		ns	2
5	TwIH	Int. Request Input High Time	3.5V	5TpC			2
			5.5V	5TpC			2
6	Twsm	STOP Mode Recovery Width Spec.	3.5V	12		ns	
			5.5V	12		ns	
7	Tost	Oscillator Start-Up Time	3.5V		5TpC		
			5.5V		5TpC		

Notes:
1. The V_{DD} voltage specification of 3.5V guarantees 3.5V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

RESET PIN OPERATION (Continued)

Table 6. Control and Peripheral Register Reset Values

Register		Bits								
(HEX)	Register Name	7	6	5	4	3	2	1	0	Comments
D4	PortB Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$
D3	PortA Spec. Func.	0	0	0	0	0	0	0	0	Deactivates all port special functions after $\overline{\text{RESET}}$
D2	PortA Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after $\overline{\text{RESET}}$
D1	PortA Output	U	U	U	U	U	U	U	U	Output register not affected by $\overline{\text{RESET}}$
D0	PortA Input	U	U	U	U	U	U	U	U	Current sample of the input pin following $\overline{\text{RESET}}$
CF	Reserved									
CE	Reserved									
CD	Reserved									
CC	Reserved									
CB	T3VAL	U	U	U	U	U	U	U	U	
CA	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	Reserved									
C6	Reserved									
C5	Reserved									
C4	Reserved									
C3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT Enabled in HALT Mode, WDT timeout at maximum value, STOP Mode disabled
C0	TCTLLO	0	0	0	0	0	0	0	0	Standard timer is disabled

Note: *The SMR and WDT flags are set indicating the source of the RESET, as shown below:

D1	D0	Reset Source
0	0	$\overline{\text{RESET}}$ Pin
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

Z8E000 WATCH-DOG TIMER (WDT)

The Watch-Dog Timer is a retriggerable one-shot 16-bit timer that resets the Z8E000 if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer timeout periods required in applications, the WDT is only updated every 64th clock cycle. When operating in the RUN or HALT Modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H and setting the WDT flag to a one state. Coming out of $\overline{\text{RESET}}$, the WDT will be fully enabled with its timeout value set at the maximum value, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watch-dog timer registers (C2H and C3H) to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register (Figure 12). The WDT cannot be disabled except on the first cycle after $\overline{\text{RESET}}$, and if the device enters Stop mode.

The WDT instruction should be executed often enough to provide some margin before allowing the WDT registers to get near 0. Because the WDT timeout periods are relatively long, a WDT reset *will* occur in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

The WDT and SMR flags are the only flags that are affected by the external $\overline{\text{RESET}}$ pin. $\overline{\text{RESET}}$ clears both the WDT and SMR flags. A WDT timeout sets the WDT flag. The STOP instruction sets the SMR flag. This behavior enables software to determine whether a pin $\overline{\text{RESET}}$ occurred, whether a WDT timeout occurred, or whether a return from STOP Mode occurred. Reading the WDT flag does not reset it to zero. The user must clear the WDT flag via software. Failure to clear the WDT flag can result in undefined behavior.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT Mode. A "1" indicates active during HALT. A "0" prevents the WDT from resetting the part while halted.Coming out of reset, the WDT will be enabled during HALT Mode.

STOP MODE (D3). Coming out of $\overline{\text{RESET}}$, the Z8E000 will have the STOP Mode disabled. If an application requires use of STOP Mode, bit D3 must be cleared immediately upon leaving $\overline{\text{RESET}}$. If bit D3 is set, the STOP instruction will execute as a NOP. If bit D3 is cleared, the STOP instruction will enter Stop Mode. Whenever the Z8E000 wakes up after having been in STOP Mode, the STOP Mode will be disabled once again.

Bits 2, 1 and 0. These bits are reserved and must be 0.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8E000 MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT Mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active, so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter the HALT Mode, the Z8E000 only requires a HALT instruction. It is NOT necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F    HALT    ; enter HALT Mode
```

The HALT Mode can be exited by servicing an interrupt (either externally or internally). Upon completion of the interrupt service routine, the user program continues from the instruction after HALT.

The HALT Mode can also be exited via a $\overline{\text{RESET}}$ activation or a Watch-Dog Timer (WDT) timeout. In these cases, program execution will restart at the reset address 0020H.

OSCILLATOR OPERATION

The Z8E000 MCU uses a Pierce oscillator with an internal feedback circuit (Figure 14). The advantages of this circuit are low cost, large output signal, low power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back to the oscillator is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements ($A \times B = 1$, where $A = V_o/V_i$ is the gain of the amplifier and $B = V_i/V_o$ is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees). VIN must be in phase with itself. The amplifier/inverter thereby provides a 180-degree phase shift, forcing the feedback element to provide the other 180 degrees of phase shift.

R_I is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and to provide the start-up transition.

Capacitor C_2, combined with the amplifier output resistance, provides a small phase shift. It will also provide some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

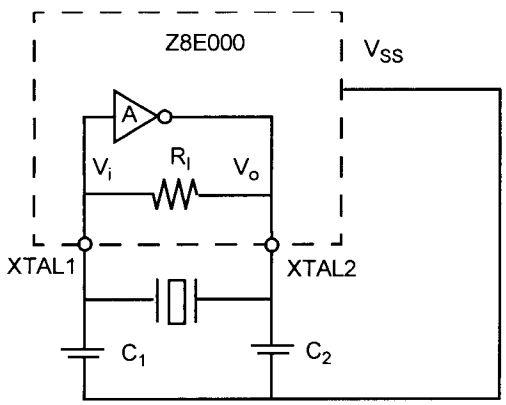


Figure 14. Pierce Oscillator with Internal Feedback Circuit

Layout

Traces connecting crystal, caps, and the Z8E000 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E000.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E000 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace of the Z8E000 V_{SS} (GND) pin. The ground side of these caps should not be shared with any other system ground trace or components except at the Z8E000 device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

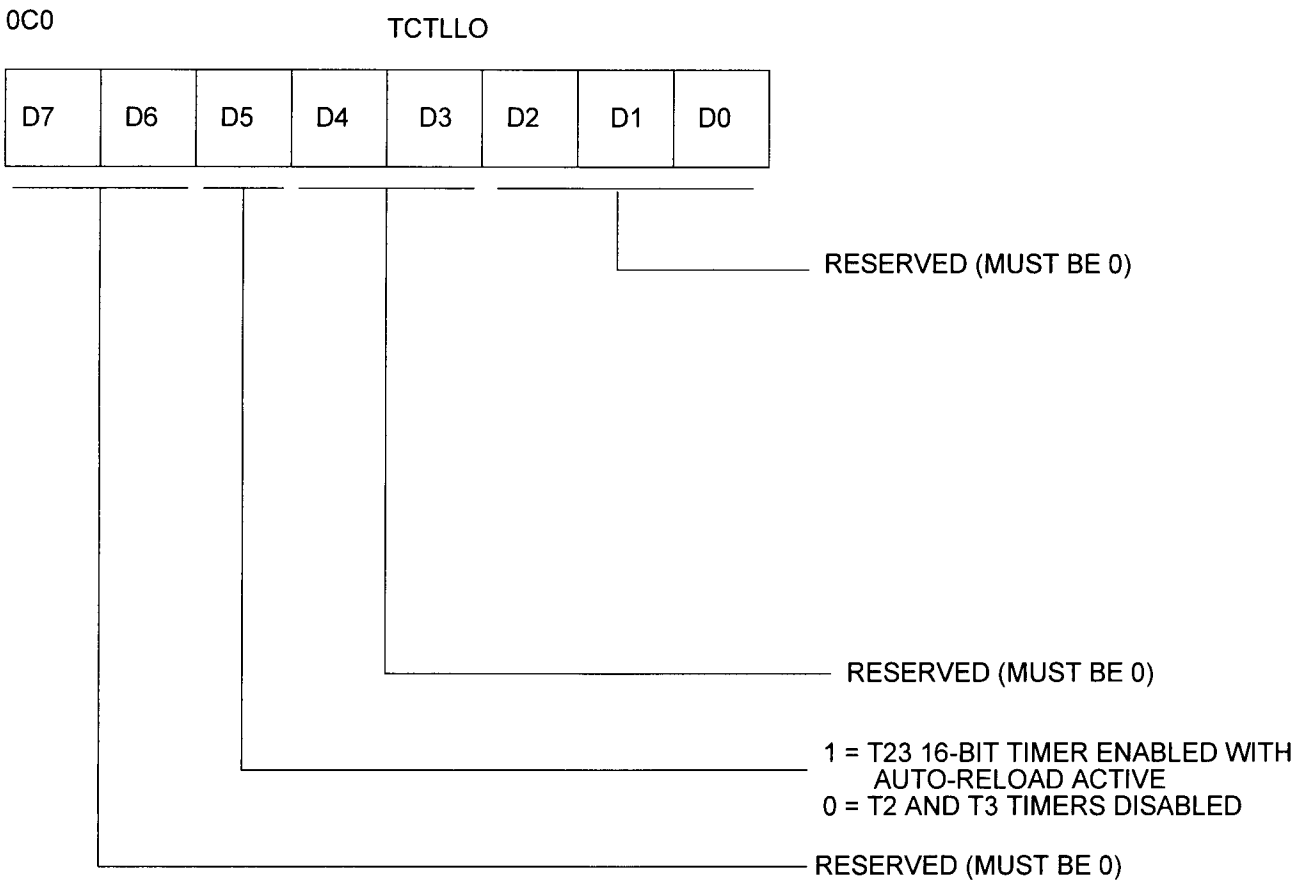
Start-up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. C_1 and C_2 require reduction if the amplifier gain is not adequate at frequency, or crystal R's are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At this point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller or a low-resistance crystal should be used.

Circuit Board Design Rules

The following circuit board design rules are suggested:

- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E000 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.



Note: Timer T23 is a standard 16-bit timer formed by cascading 8-bit timers t3(msb) and t2(lsb).

Figure 20. TCTLLO Register

Each 8-bit timer is equipped with a pair of readable and writable registers, which are both readable and writable. One of the registers is defined to contain the auto-initialization value for the timer, while the second register contains the current value for the timer. When a timer is enabled, the timer will decrement whatever value is currently held in its count register. From that point, the timer continues decrementing until it reaches 0, at which time an interrupt will be generated and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer will stop counting upon reaching 0, and control logic will clear the appropriate control register bit to disable the timer. This operation is referred to as a "single-shot". If auto-initialization is enabled, the timer will continue counting from the initialization value. Software should not attempt to use registers that are defined as having timer functionality for any other purpose.

Software is allowed to write to any register at any time, but care should be taken if timer registers are updated while the timer is enabled. If software updates the count value while the timer is in operation, the timer will continue counting based upon the software-updated value. Strange behavior can result if the software update occurred at exactly the point that the timer was reaching 0 to trigger an interrupt and/or reload.

Similarly, if software updates the initialization value register while the timer is active, the next time that the timer reaches 0, it will be initialized using the updated value. Again, strange behavior could result if the initialization value register is being written while the timer is in the process of being initialized. Whether initialization is done with the new or old value is a function of the exact timing of the write operation. In all cases, the Z8E000 will prioritize the software write above that of a decrementer writeback. Howev-

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, while the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads will not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position will contain the current synchronized input value. Thus, writes to that bit position will be overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit will retain the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The above result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read will return the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input will be disabled to save power.

Updates to the output register will take effect based upon the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and will return the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others, but care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, and setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately and all initialization has been completed.

PORT A REGISTER DEFINITIONS

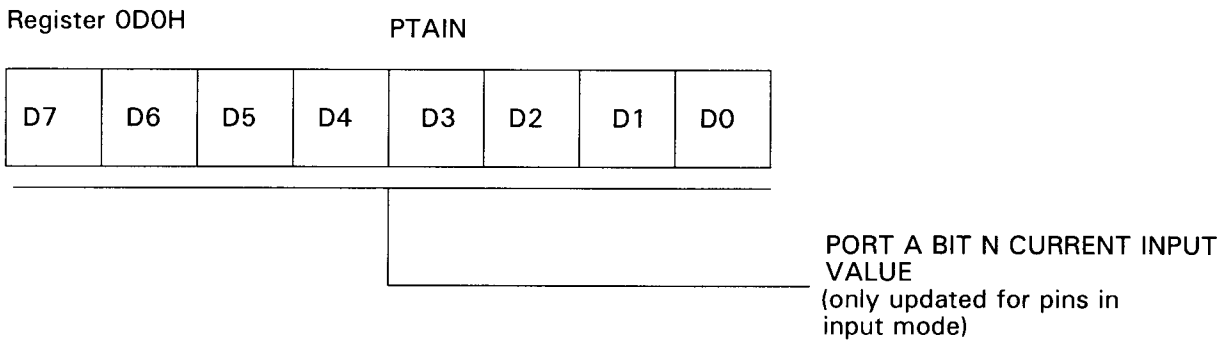


Figure 24. Port A Input Value Register

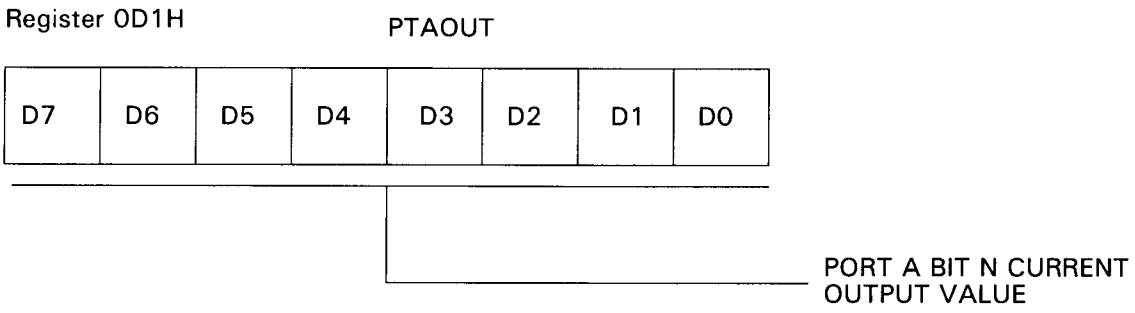


Figure 25. Port A Output Value Register

PORT B

Port B Description

Port B is a 5-bit, bidirectional, CMOS-compatible I/O port. These five I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. See Figure 29 through Figure 33 for diagrams of all five Port B pins.

In addition to standard input/output capability on all five pins of Port B, each pin provides special functionality as indicated in Table 8:

Table 8. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	None
PB2	IRQ3	None
PB3	None	None
PB4	IRQ1/IRQ4	None

Special functionality is invoked via the Port B Special Function Register. See Figure 28 for the arrangement and control conventions for this register.

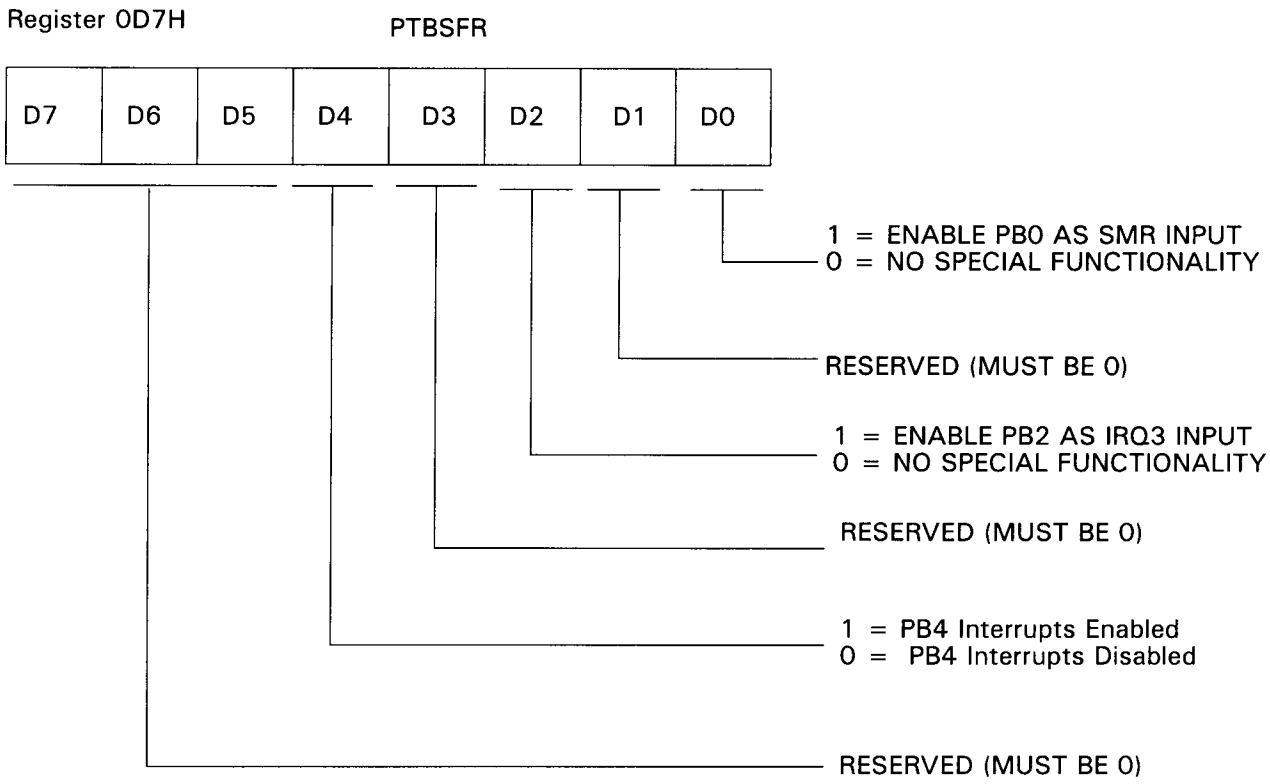


Figure 28. Port B Special Function Register

PORT B—PIN 2 CONFIGURATION

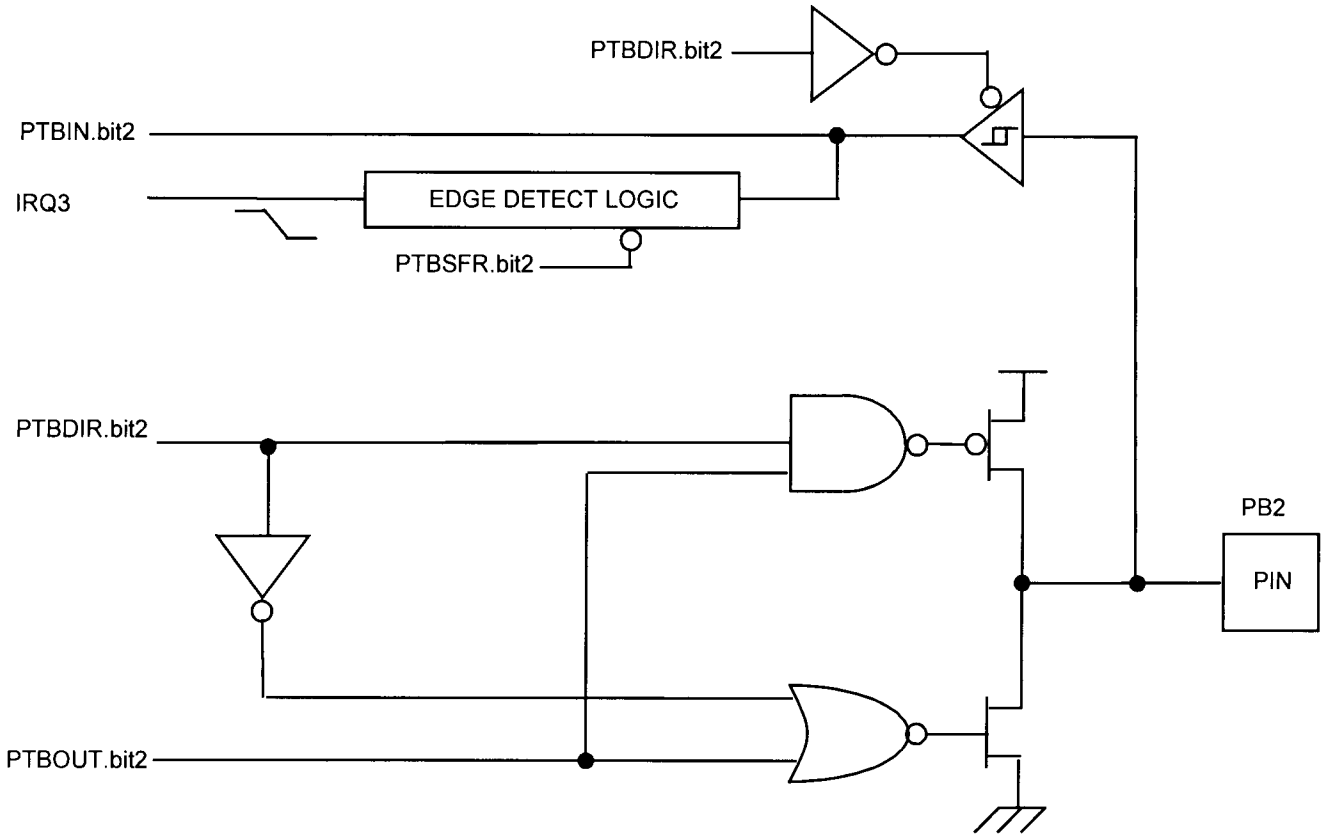


Figure 31. Port B Pin 2 Diagram

PORT B CONTROL REGISTER DEFINITIONS

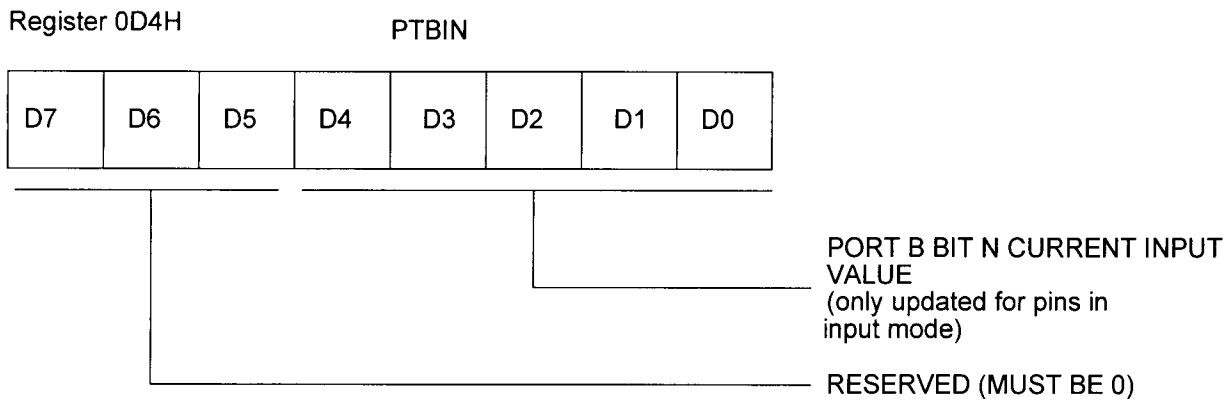


Figure 33. Port B Input Value Register

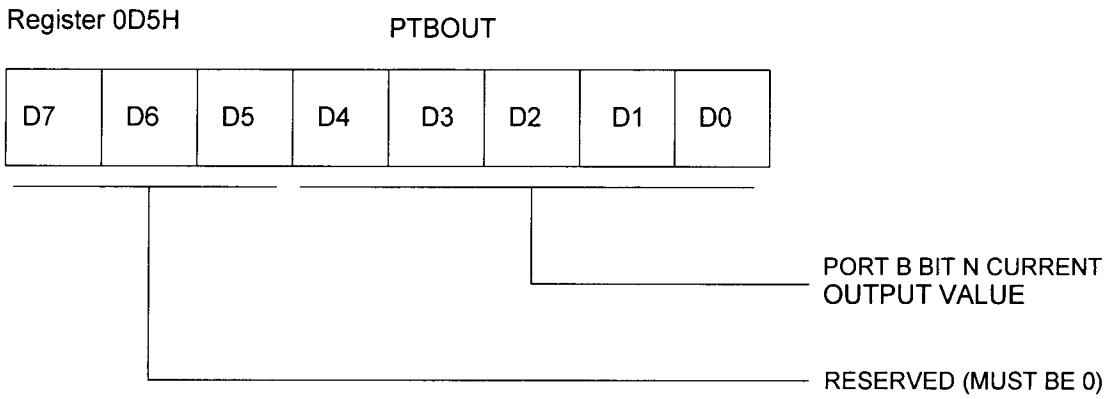


Figure 34. Port B Output Value Register

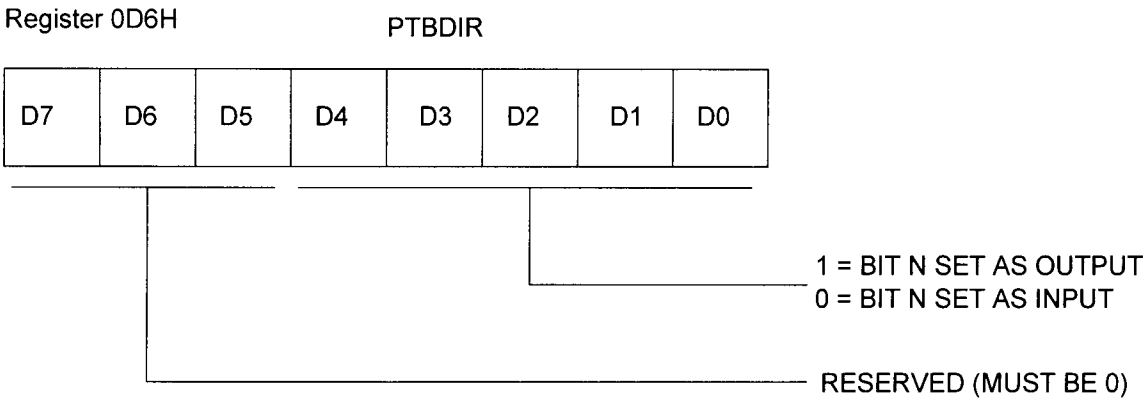
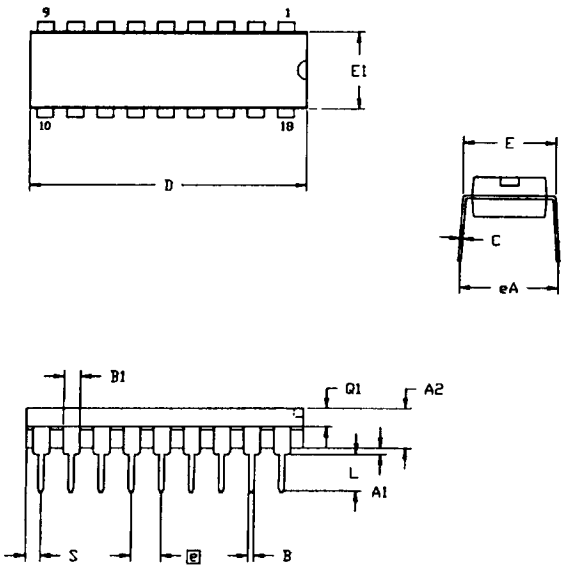


Figure 35. Port B Directional Control Register

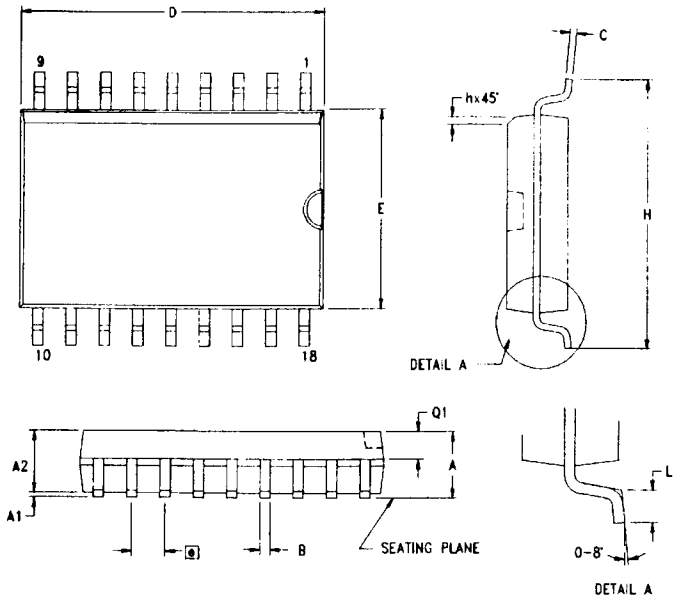
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

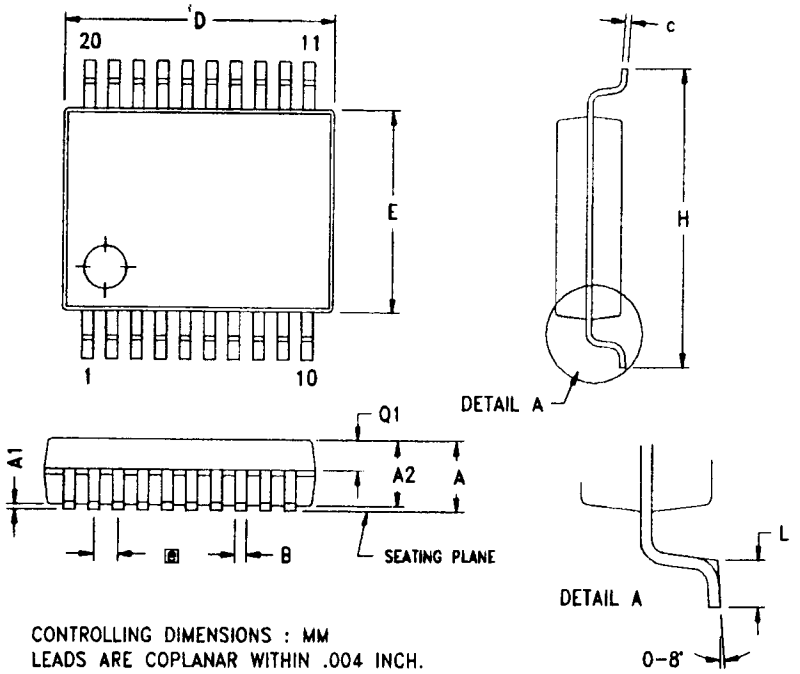
Figure 39. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 40. 18-Pin SOIC Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 41. 20-Pin SSOP Package Diagram

ORDERING INFORMATION

Standard Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PSC	Z8E00010SSC	Z8E00010HSC

Extended Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PEC	Z8E00010SEC	Z8E00010HEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes	
Preferred Package	P = Plastic DIP
Longer Lead Time	S = SOIC
	H = SSOP
Preferred Temperature	S = 0°C to +70°C
	E = –40°C to +105°C
Speed	10 = 10 MHz
Environmental	C = Plastic Standard

Example:

Z 8E000 10 P S C is a Z86E000, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow