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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	WDT
Number of I/O	13
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	32 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00010heg

GENERAL DESCRIPTION (Continued)

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$ (WORD is active Low, only); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

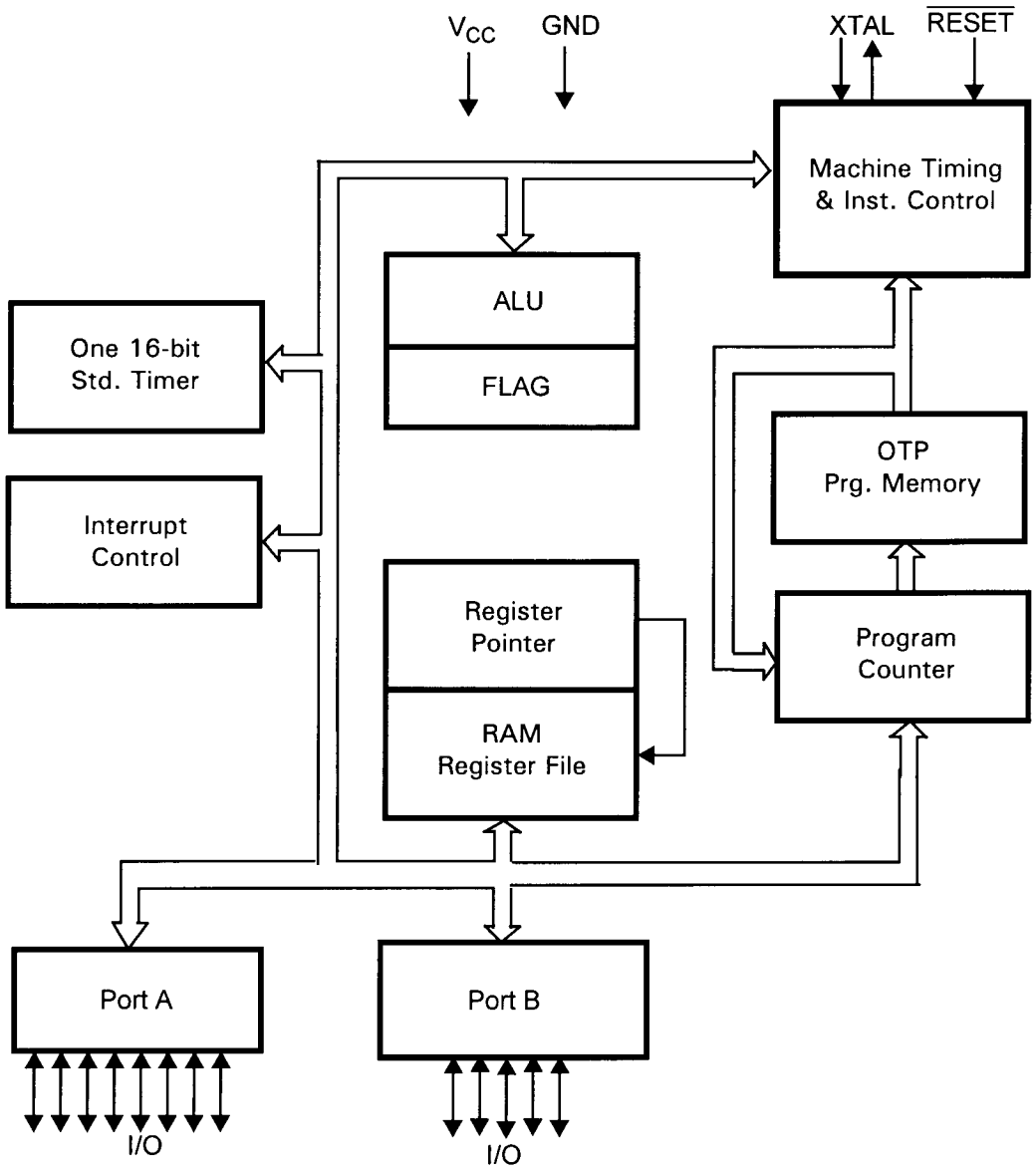


Figure 1. Functional Block Diagram

PIN DESCRIPTION

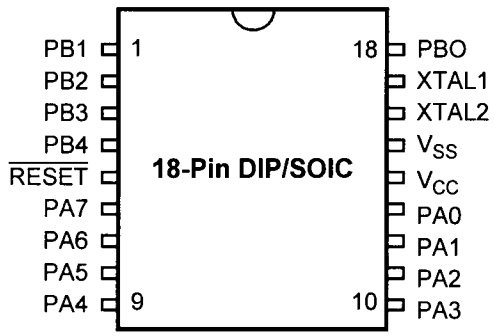


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. 18-Pin DIP/SOIC Pin Assignments

Standard Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	$\overline{\text{RESET}}$	Reset	Input
6–9	PA7–PA4	Port A, Pins 7,6,5,4	In/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	In/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	In/Output

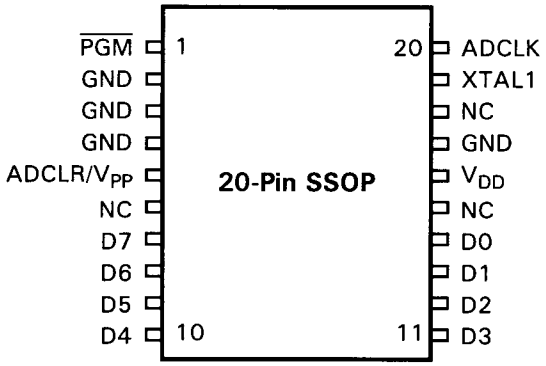


Figure 6. 20-Pin SSOP Pin Identification; EPROM Programming Mode

Table 4. 20-Pin SSOP Pin Assignments; EPROM Programming Mode

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	In/Output
11–14	D3–D0	Data 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1 MHz Clock	Input
20	ADCLK	Address Clock	Input

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

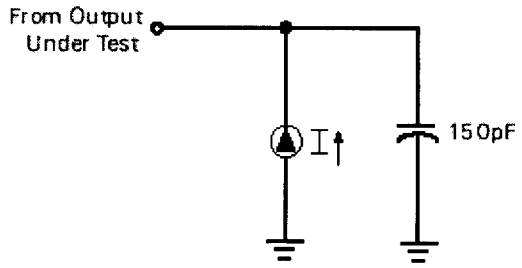


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS (Continued)

			T_A = –40°C to +105°C					
Sym	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C [2]	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA,	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA,	
V_{RH}	Reset Input High Voltage	4.5V	0.5V_{CC}	V_{CC}	1.1	V		
		5.5V	0.5V_{CC}	V_{CC}	2.2	V		
I_{IL}	Input Leakage	4.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	4.5V	–18	–180	–112	mA		
		5.5V	–18	–180	–112	mA		
I_{CC}	Supply Current	4.5V		7.0	4.0	mA	@ 10 MHz	3,4
		5.5V		7.0	4.0	mA	@ 10 MHz	3,4
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	3,4
		5.5V		2.0	1.0	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 10 MHz	3,4

		T_A = –40°C to +105°C						
Sym	Parameter	V_{CC} [1]	Min	Max	Typical @ 25°C [2]	Units	Conditions	Notes
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP Mode V_{IN} = 0V, V_{CC}	5
		5.5V		700	250	nA	STOP Mode V_{IN} = 0V, V_{CC}	5

Notes:

1. The V_{CC} voltage specification of 4.5 V and 5.5 V guarantees 5.0 V ±0.5 V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V.
3. All outputs unloaded, I/O pins floating, and all inputs are at V_{CC} or V_{SS} level.
4. CL1 = CL2 = 22 pF.
5. Same as note 3 except inputs at V_{CC}.

RESET PIN OPERATION (Continued)

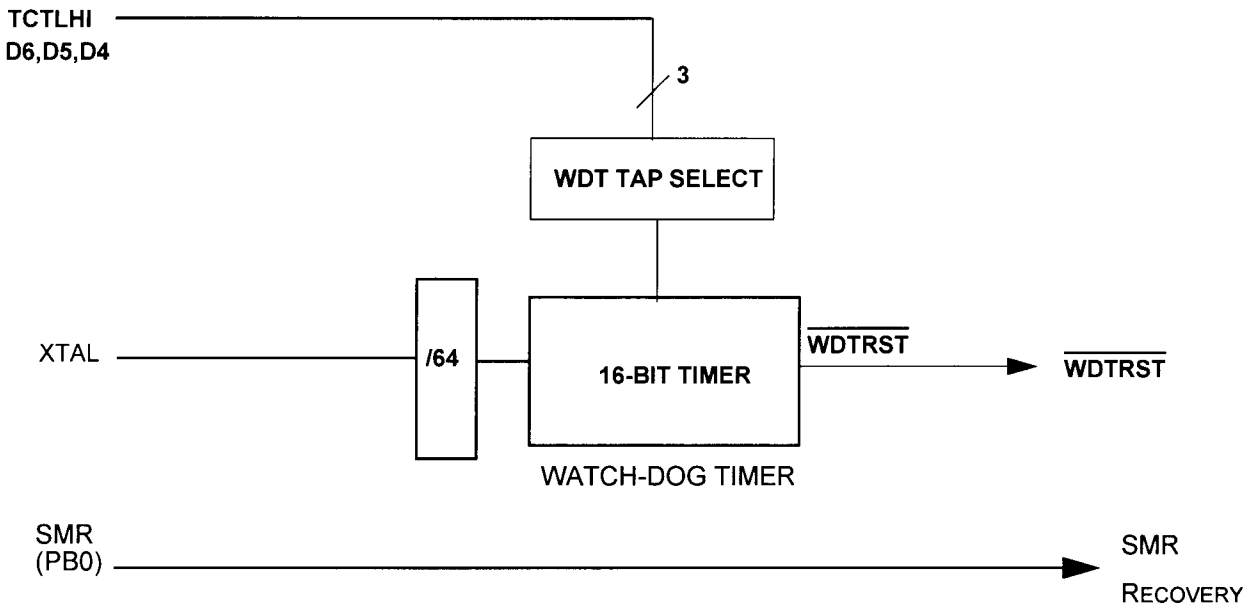


Figure 11. Z8E000 Reset Circuitry with WDT and SMR

Z8E000 WATCH-DOG TIMER (WDT)

The Watch-Dog Timer is a retriggerable one-shot 16-bit timer that resets the Z8E000 if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer timeout periods required in applications, the WDT is only updated every 64th clock cycle. When operating in the RUN or HALT Modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H and setting the WDT flag to a one state. Coming out of $\overline{\text{RESET}}$, the WDT will be fully enabled with its timeout value set at the maximum value, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watch-dog timer registers (C2H and C3H) to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register (Figure 12). The WDT cannot be disabled except on the first cycle after $\overline{\text{RESET}}$, and if the device enters Stop mode.

The WDT instruction should be executed often enough to provide some margin before allowing the WDT registers to get near 0. Because the WDT timeout periods are relatively long, a WDT reset *will* occur in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

The WDT and SMR flags are the only flags that are affected by the external $\overline{\text{RESET}}$ pin. $\overline{\text{RESET}}$ clears both the WDT and SMR flags. A WDT timeout sets the WDT flag. The STOP instruction sets the SMR flag. This behavior enables software to determine whether a pin $\overline{\text{RESET}}$ occurred, whether a WDT timeout occurred, or whether a return from STOP Mode occurred. Reading the WDT flag does not reset it to zero. The user must clear the WDT flag via software. Failure to clear the WDT flag can result in undefined behavior.

OSCILLATOR OPERATION

The Z8E000 MCU uses a Pierce oscillator with an internal feedback circuit (Figure 14). The advantages of this circuit are low cost, large output signal, low power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

One draw back to the oscillator is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements ($A \times B = 1$, where $A = V_o/V_i$ is the gain of the amplifier and $B = V_i/V_o$ is the gain of the feedback element). The total phase shift around the loop is forced to zero (360 degrees). VIN must be in phase with itself. The amplifier/inverter thereby provides a 180-degree phase shift, forcing the feedback element to provide the other 180 degrees of phase shift.

R_I is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and to provide the start-up transition.

Capacitor C_2, combined with the amplifier output resistance, provides a small phase shift. It will also provide some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides additional phase shift.

C_1 and C_2 can affect the start-up time if they increase dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it does not start up any more.

It is recommended for fast and reliable oscillator start-up (over the manufacturing process range) that the load capacitors be sized as low as possible without resulting in overtone operation.

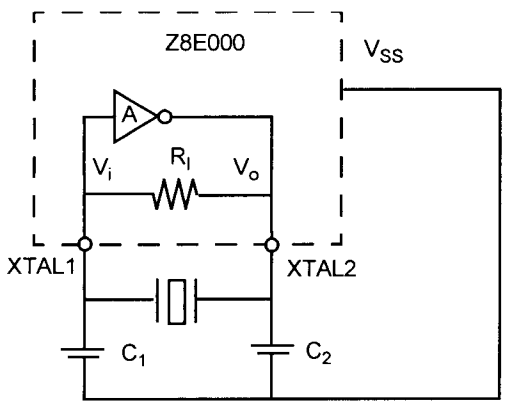


Figure 14. Pierce Oscillator with Internal Feedback Circuit

Layout

Traces connecting crystal, caps, and the Z8E000 oscillator pins should be as short and wide as possible, to reduce parasitic inductance and resistance. The components (caps, crystal, resistors) should be placed as close as possible to the oscillator pins of the Z8E000.

The traces from the oscillator pins of the IC and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8E000 device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace of the Z8E000 V_{SS} (GND) pin. The ground side of these caps should not be shared with any other system ground trace or components except at the Z8E000 device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. C_1 and C_2 require reduction if the amplifier gain is not adequate at frequency, or crystal R's are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At this point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller or a low-resistance crystal should be used.

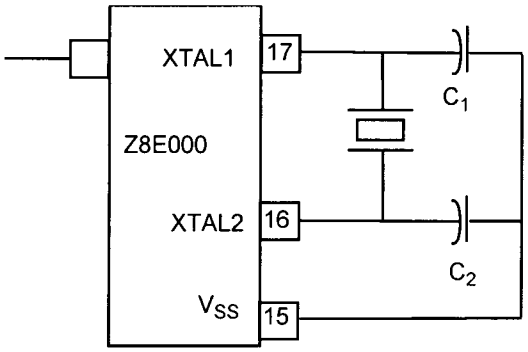
Circuit Board Design Rules

The following circuit board design rules are suggested:

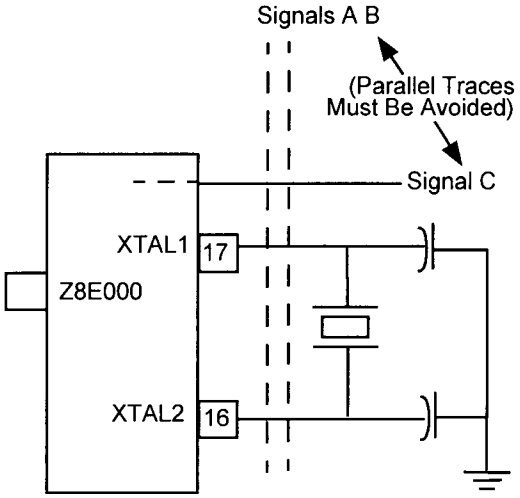
- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8E000 as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.

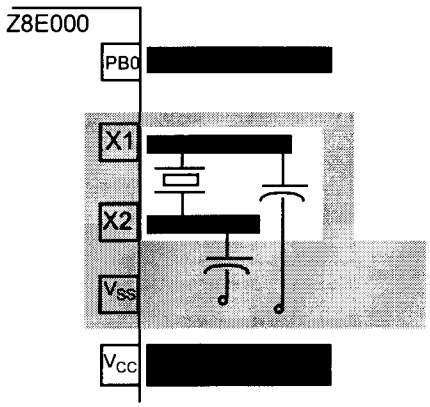
OSCILLATOR OPERATION (Continued)

- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistance between XTAL1 or XTAL2 and the other pins should be greater than 10 MΩ.



Clock Generator Circuit





Board Design Example
(Top View)

Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should have the following characteristics to ensure proper oscillator operation:

Crystal Cut	AT (crystal only)
Mode	Parallel, Fundamental Mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF, 15 typical
Resistance	100 ohms max

Depending on operation frequency, the oscillator can require the addition of capacitors C_1 and C_2 (shown in Figure 17 and Figure 18). The capacitance values are dependent on the manufacturer's crystal specifications.

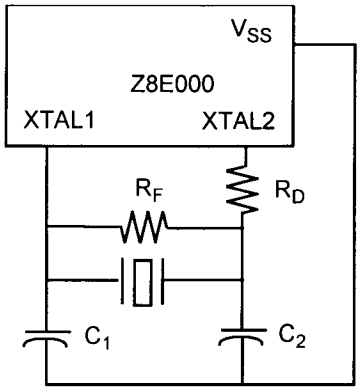


Figure 16. Crystal/Ceramic Resonator Oscillator

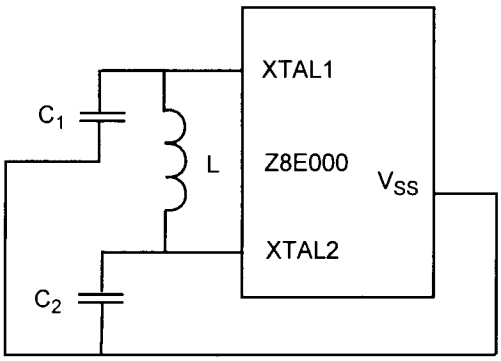


Figure 17. LC Clock

In most cases, the R_D is zero ohms (0Ω), and R_F is infinite. The set value is determined and specified by the crystal/ceramic resonator manufacturer. R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. R_D can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8E000 oscillator already has an internal shunt resistor in parallel to the crystal/ceramic resonator.

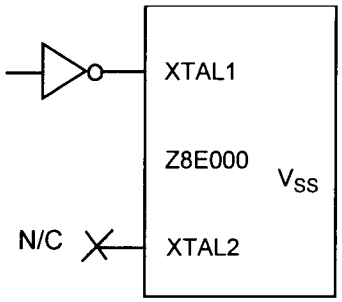


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8E000, thereby ensuring that no system noise is injected into the Z8E000 clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8E000.

Note: A parallel resonant crystal or resonator data sheet will specify a load capacitor value that is the series combination of C_1 and C_2, including all parasitics (PCB and holder).

LC OSCILLATOR

The Z8E000 oscillator can use a LC network to generate a XTAL clock (Figure 18).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics and C_T is the total series capacitance including the parasitics.

Simple series capacitance is calculated using the following equation:

$1/C_T$	$= 1/C_1 + 1/C_2$
If C_1	$= C_2$
$1/C_T$	$= 2\ C_1$
C_1	$= 2\ C_T$

A sample calculation of capacitance C_1 and C_2 for 5.83-MHz frequency and inductance value of 27 uH is illustrated as follows:

$$5.83\ (10\text{^}6) = \frac{1}{2\pi\ [2.7\ (10^{-6})\ C_T]\ 1/2}$$

$$C_T = 27.6\ \text{pf}$$

Thus C_1 = 55.2 pf and C_2 = 55.2 pf.

TIMERS

Two 8-bit timers (T2 and T3), are provided but can only operate in cascade to function as a 16-bit standard timer (Figure 19).

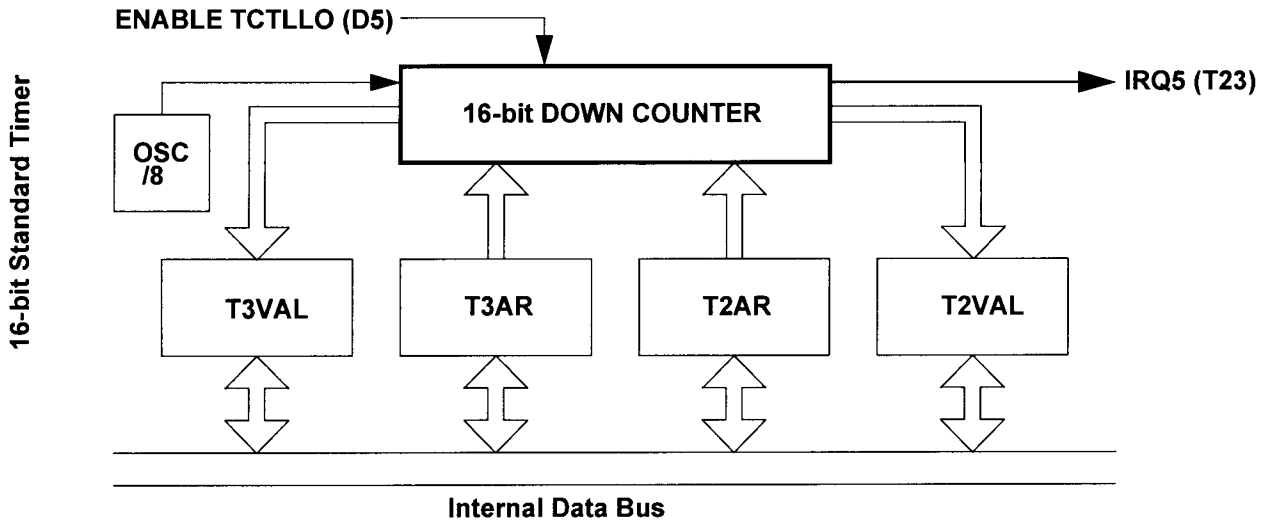


Figure 19. Timer Block Diagram

TIMERS (Continued)

er, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit will override a software write. Reading either register can be done at any time, and will have no effect on the functionality of the timer.

When defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt will be generated, and the interrupt will correspond to the even 8-bit timer. For example, timers T2 and T3 are cascaded to form a single 16-bit timer, so the interrupt for the combined timer will be defined to be that of timer T2 rather than T3 (Figure 20). When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T2) will be defined to hold the timer's least significant byte. Conversely, the odd timer in the pair (timer T3) will hold the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value will be initialized by copying the contents of the auto-initialization value register to the count value register.

Note: Any time that a timer pair is defined to act as a single 16-bit timer, the auto-reload function will be performed automatically. All 16-bit timers will continue counting while their interrupt requests are active, and will operate in a free-running manner.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt has been responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the write will begin counting using the value that is held in their count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source only. Each timer that is enabled will be updated every 8th XTAL clock cycle.

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, while the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads will not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position will contain the current synchronized input value. Thus, writes to that bit position will be overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit will retain the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The above result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read will return the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input will be disabled to save power.

Updates to the output register will take effect based upon the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and will return the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others, but care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, and setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately and all initialization has been completed.

PORT A

Port A is a general-purpose port (Figure 23). Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 22. A bit set to a "1" in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to "0" configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27.)

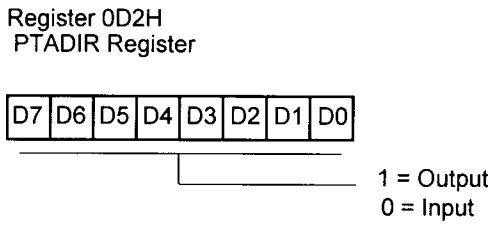


Figure 22. Port A Directional Control Register

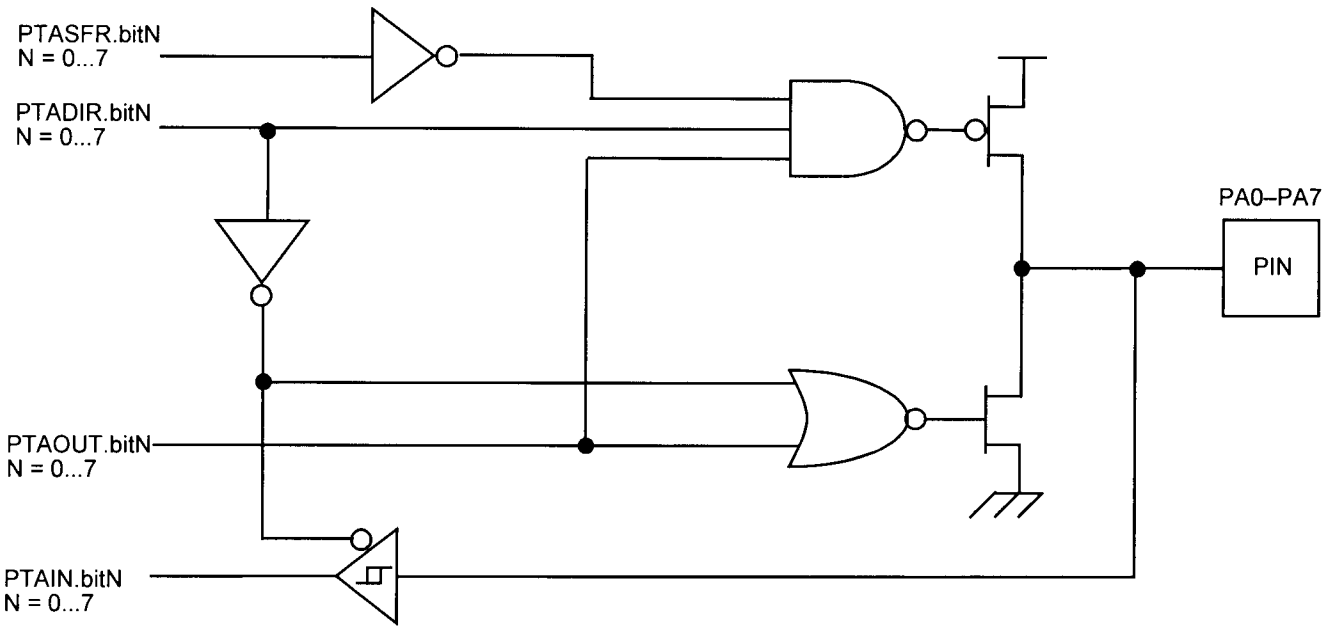


Figure 23. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

PORT A REGISTER DEFINITIONS

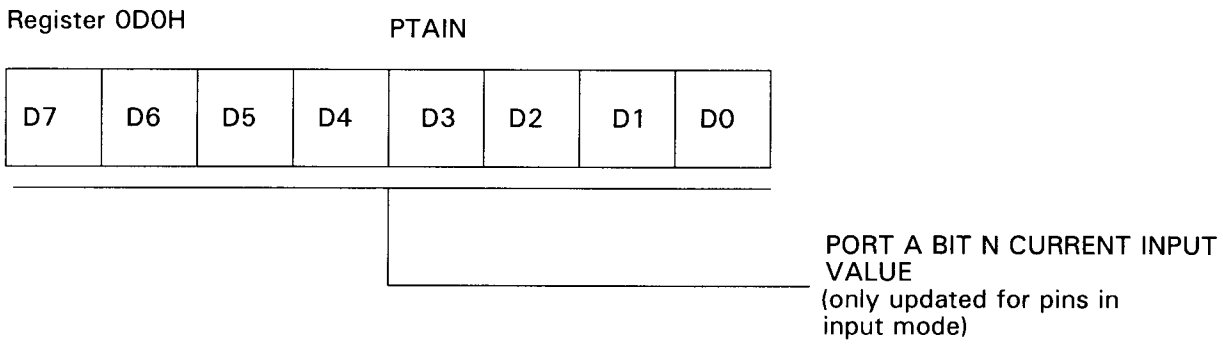


Figure 24. Port A Input Value Register

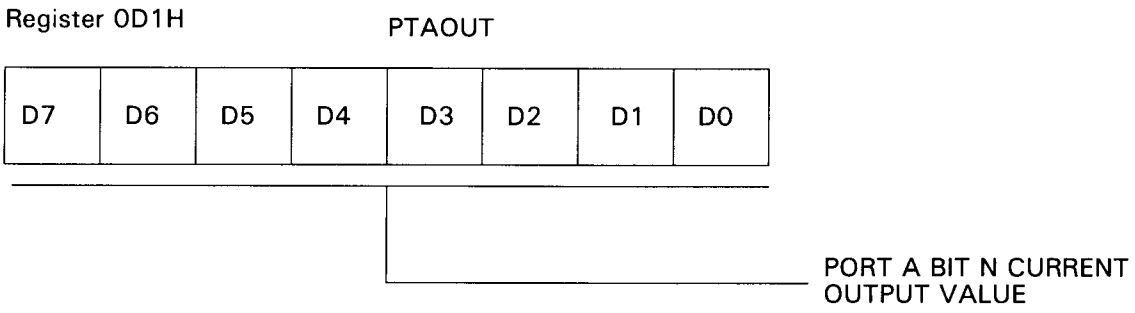


Figure 25. Port A Output Value Register

PORT B—PIN 0 CONFIGURATION

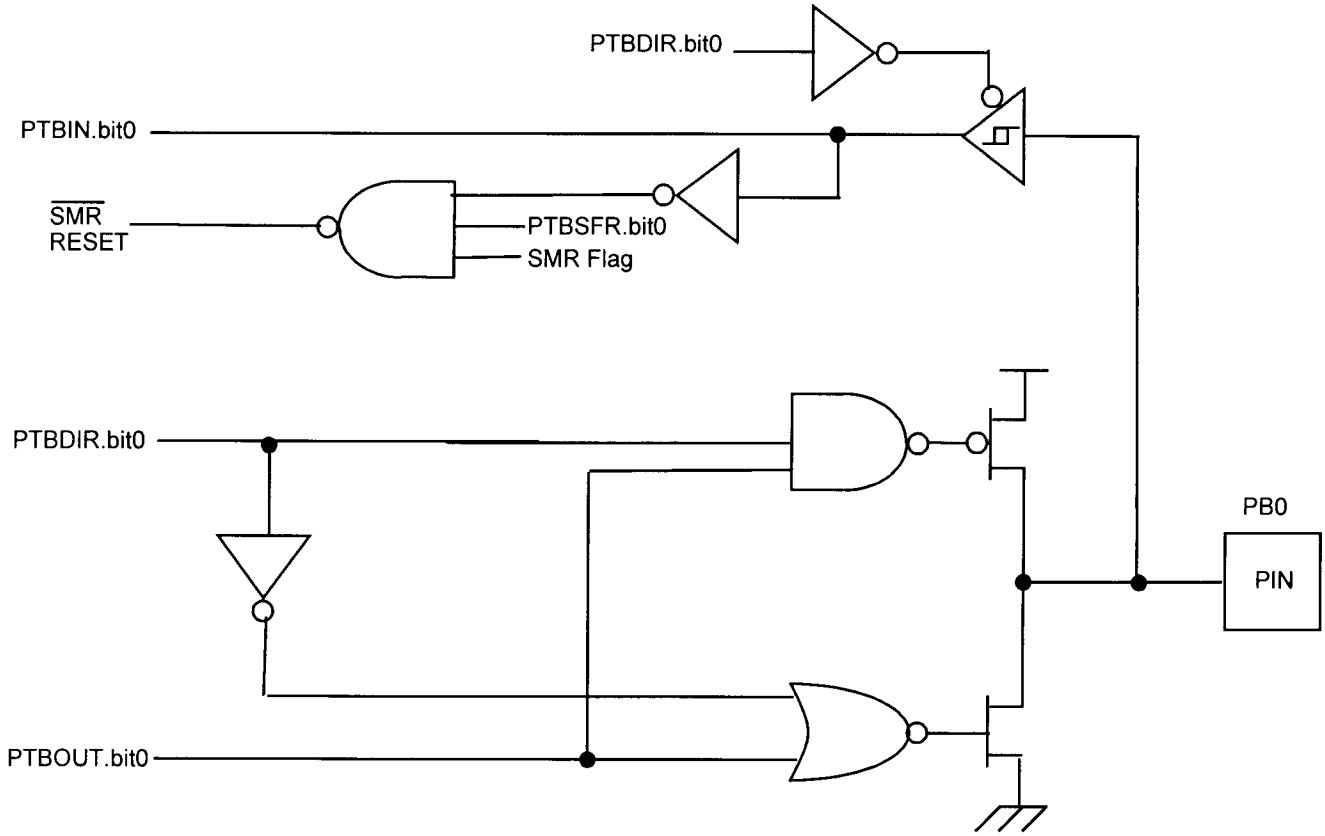


Figure 29. Port B Pin 0 Diagram

PORT B—PIN 1 CONFIGURATION

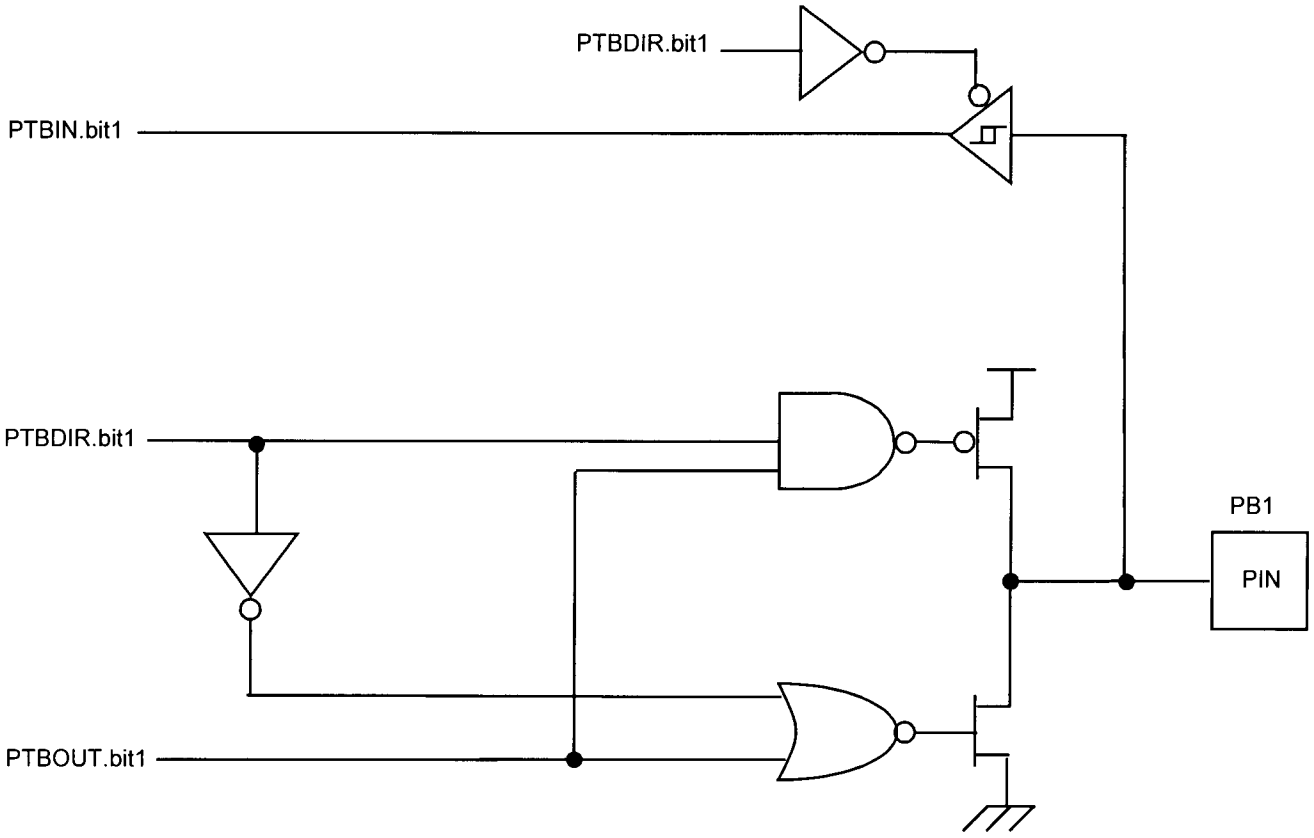


Figure 30. Port B Pin 1 Diagram

PORT B CONTROL REGISTER DEFINITIONS

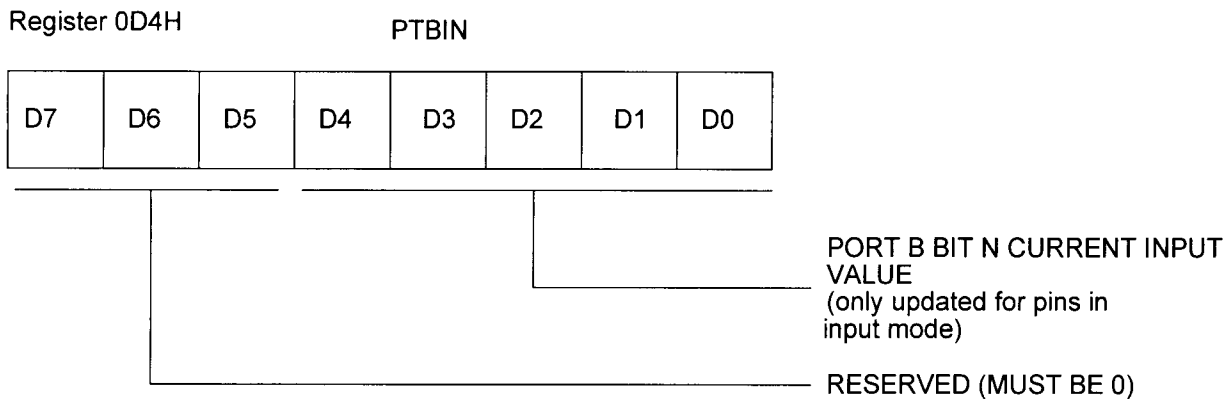


Figure 33. Port B Input Value Register

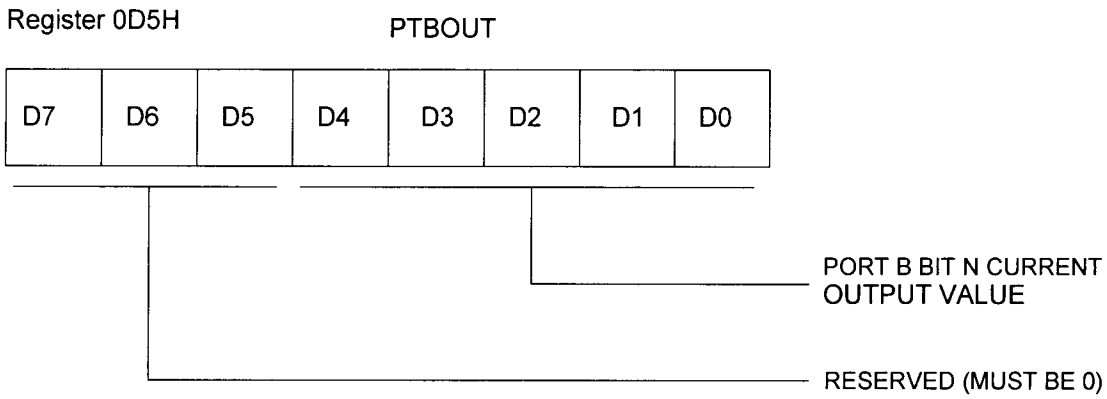


Figure 34. Port B Output Value Register

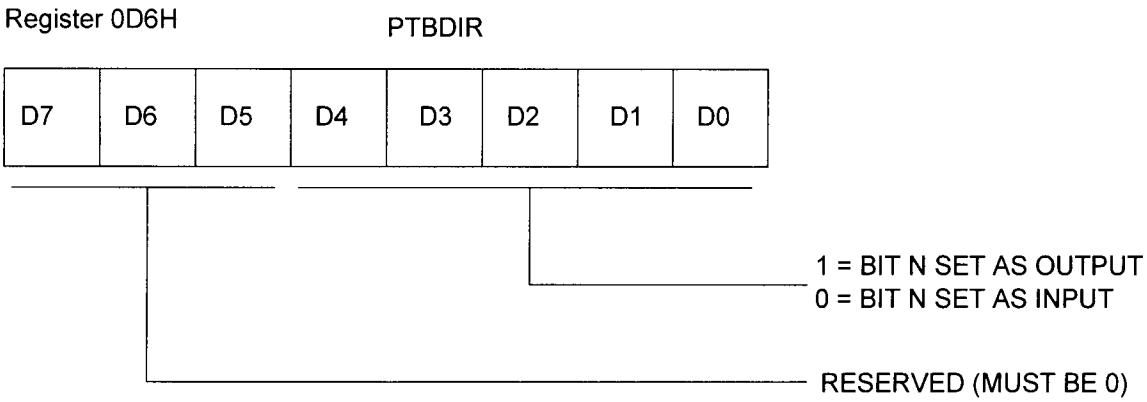


Figure 35. Port B Directional Control Register

PORT B CONTROL REGISTER DEFINITIONS (Continued)

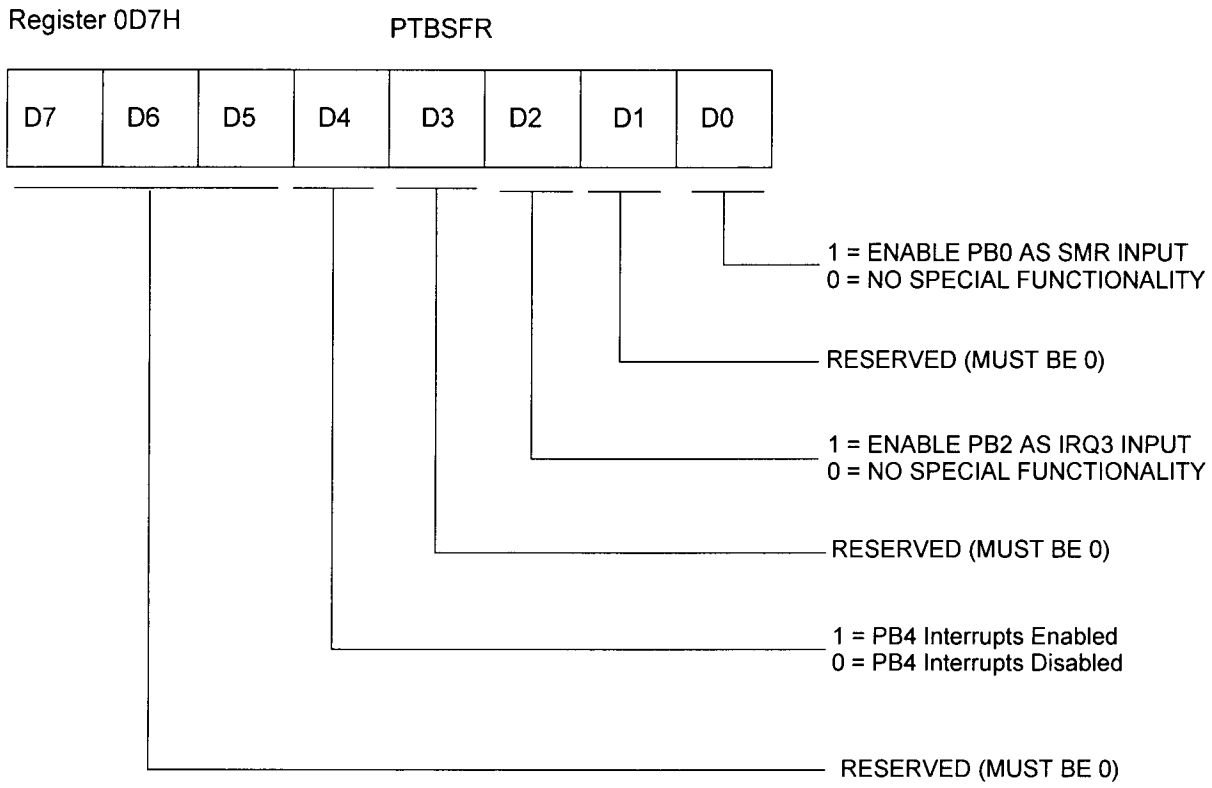


Figure 36. Port B Special Function Register