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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	WDT
Number of I/O	13
Program Memory Size	512B (512 x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	32 x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8e00010hsc00tr

GENERAL DESCRIPTION (Continued)

Note: All signals with an overline, "‾", are active Low. For example, B/$\overline{W}$ (WORD is active Low, only); $\overline{B}$/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

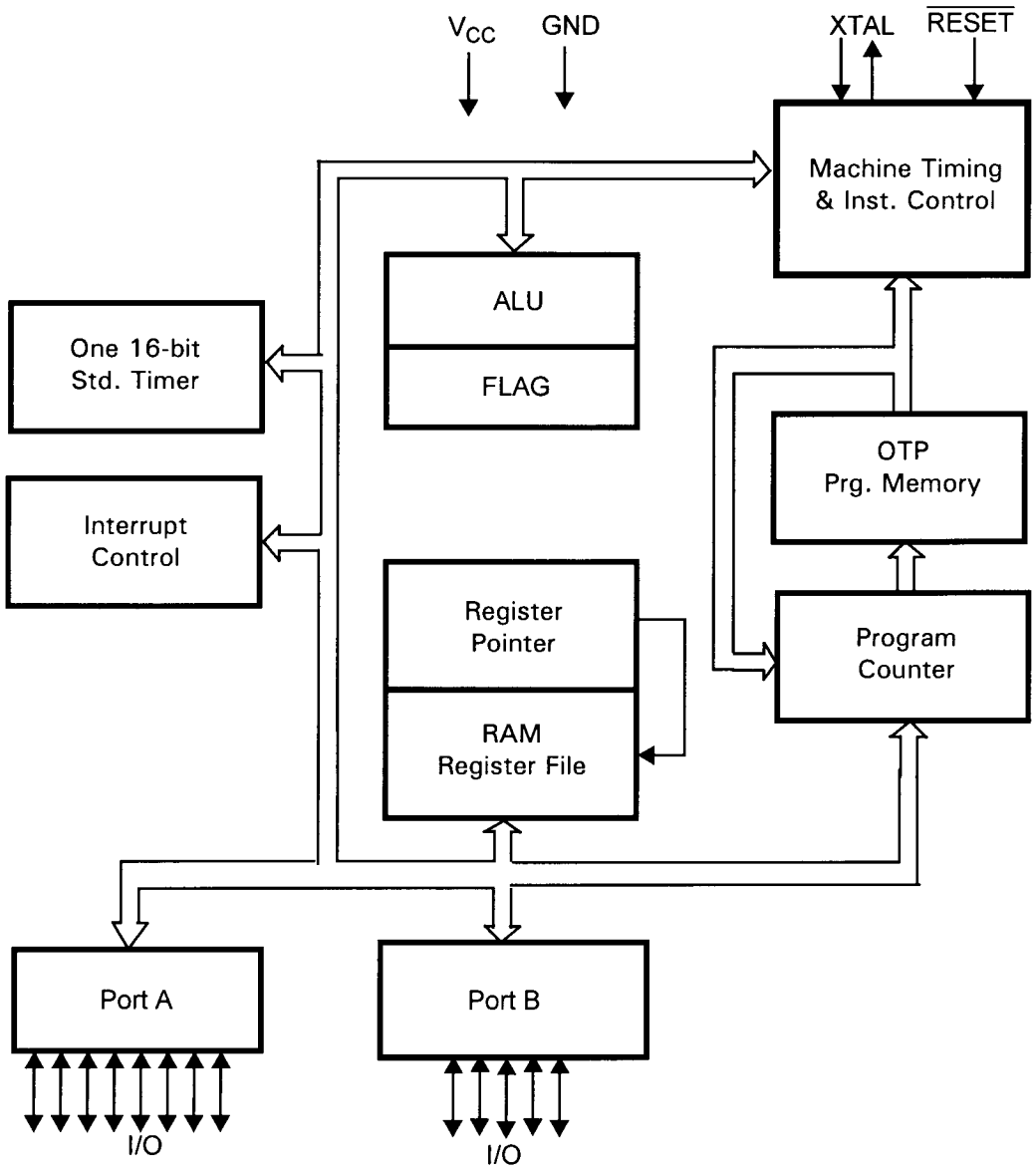


Figure 1. Functional Block Diagram

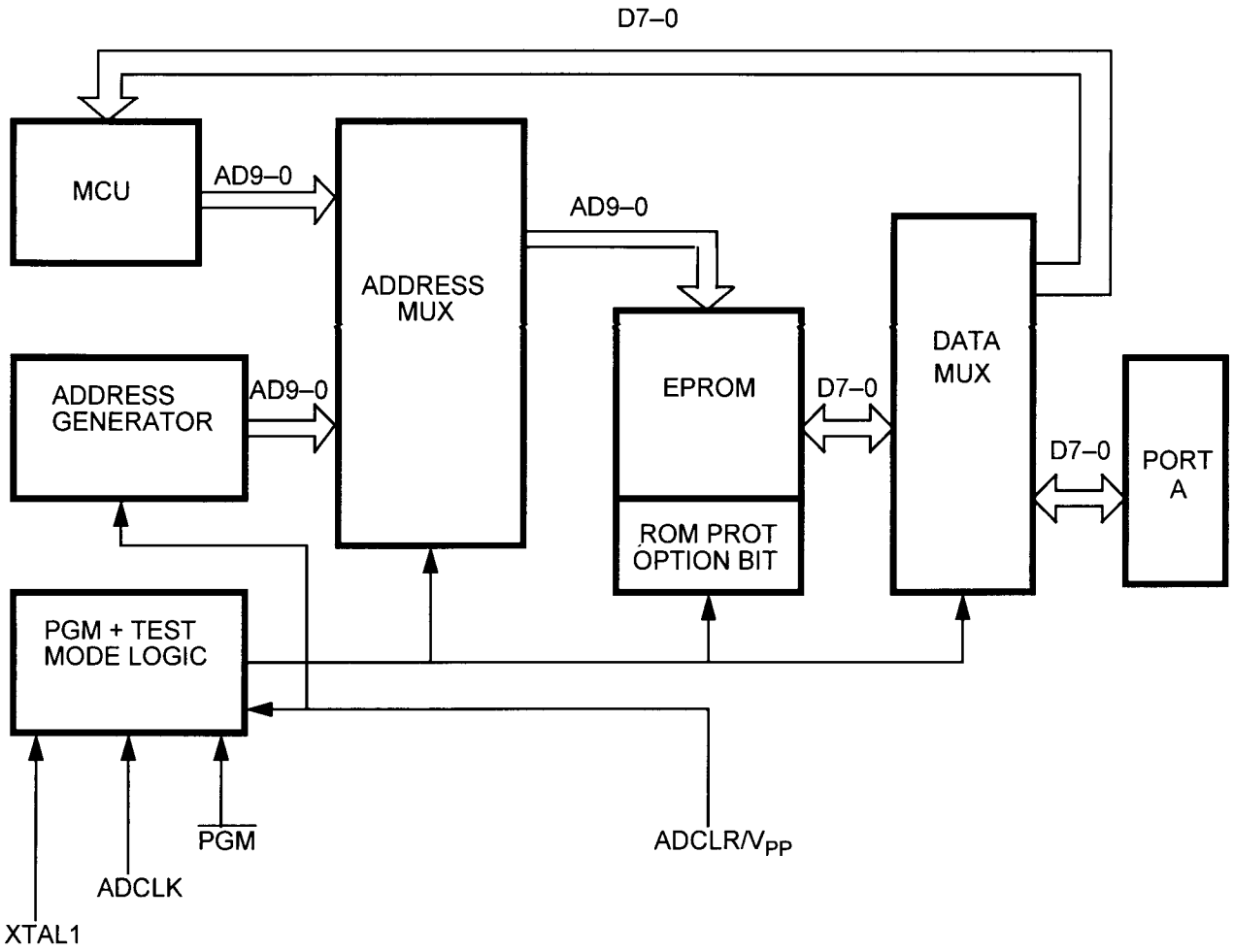


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

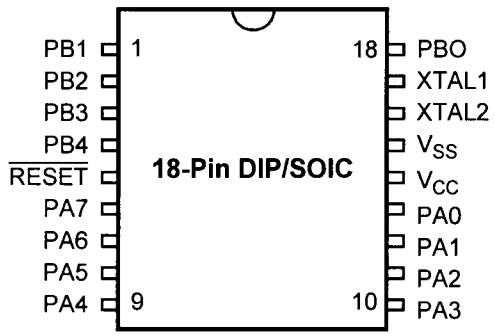


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. 18-Pin DIP/SOIC Pin Assignments

Standard Mode			
Pin #	**Symbol**	**Function**	**Direction**
1–4	PB1–PB4	Port B, Pins 1,2,3,4	In/Output
5	$\overline{\text{RESET}}$	Reset	Input
6–9	PA7–PA4	Port A, Pins 7,6,5,4	In/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	In/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	In/Output

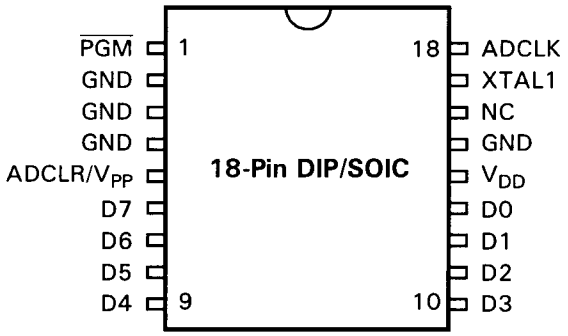


Figure 4. 18-Pin DIP/SOIC Pin Identification; EPROM Programming Mode

Table 2. 18-Pin DIP/SOIC Pin Assignments; EPROM Programmable Mode

EPROM Programming Mode			
Pin #	**Symbol**	**Function**	**Direction**
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6–9	D7–D4	Data 7,6,5,4	In/Output
10–13	D3–D0	Data 3,2,1,0	In/Output
14	V_{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1 MHz Clock	Input
18	ADCLK	Address Clock	Input

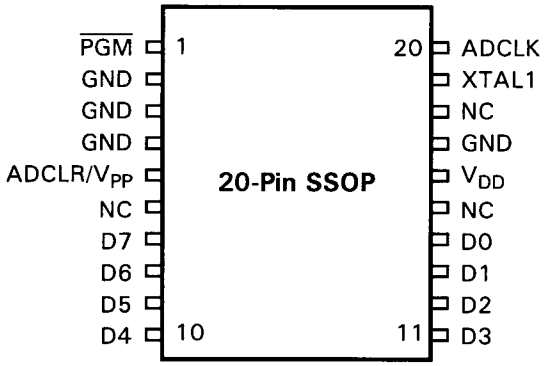


Figure 6. 20-Pin SSOP Pin Identification; EPROM Programming Mode

Table 4. 20-Pin SSOP Pin Assignments; EPROM Programming Mode

EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	In/Output
11–14	D3–D0	Data 3,2,1,0	In/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1 MHz Clock	Input
20	ADCLK	Address Clock	Input

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on $\overline{RESET}$ Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		80	mA	
Maximum Allowable Current into V_{DD}		80	mA	
Maximum Allowable Current into an Input Pin	–600	+600	mA	3
Maximum Allowable Current into an Open-Drain Pin	–600	+600	mA	4
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	
Maximum Allowable Output Current Sourced by Port A		40	mA	
Maximum Allowable Output Current Sunk by Port B		40	mA	
Maximum Allowable Output Current Sourced by Port B		40	mA	

Notes:
1. Applies to all pins except the $\overline{RESET}$ pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. Excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{0L} \times I_{0L})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

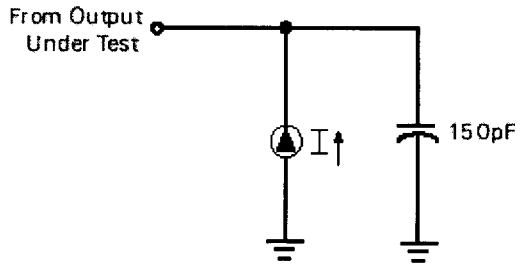


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

			T_A = 0°C to +70°C					
Sym	Parameter	V_{CC}[1]	Min	Max	Typical @ 25°C[2]	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.5V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.5V	$0.7V_{CC}$	V_{CC}+0.3	1.3	V		
		5.5V	$0.7V_{CC}$	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.7	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	3.5V	V_{CC}–0.4		3.1	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	3.5V		0.6	0.2	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	I_{OL} = +6 mA	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	
V_{RH}	Reset Input High Voltage	3.5V	$0.5V_{CC}$	V_{CC}	1.1	V		
		5.5V	$0.5V_{CC}$	V_{CC}	2.2	V		
V_{RL}	Reset Input Low Voltage	3.5V	V_{SS}–0.3	$0.2V_{CC}$	0.9	V		
		5.5V	V_{SS}–0.3	$0.2V_{CC}$	1.4	V		
I_{IL}	Input Leakage	3.5V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.064	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	0.114	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.5V	–10	–60	–30	µA		
		5.5V	–20	–180	–100	µA		
I_{CC}	Supply Current	3.5V		2.5	2.0	mA	@ 10 MHz	3,4
		5.5V		6.0	4.0	mA	@ 10 MHz	3,4
I_{CC1}	Standby Current	3.5V		2.0	1.0	mA	Halt Mode V_{IN} = 0V V_{CC}@10 MHz	3,4
		5.5V		6.0	4.0	mA	Halt Mode V_{IN} = 0V V_{CC}@10 MHz	3,4

RESET PIN OPERATION (Continued)

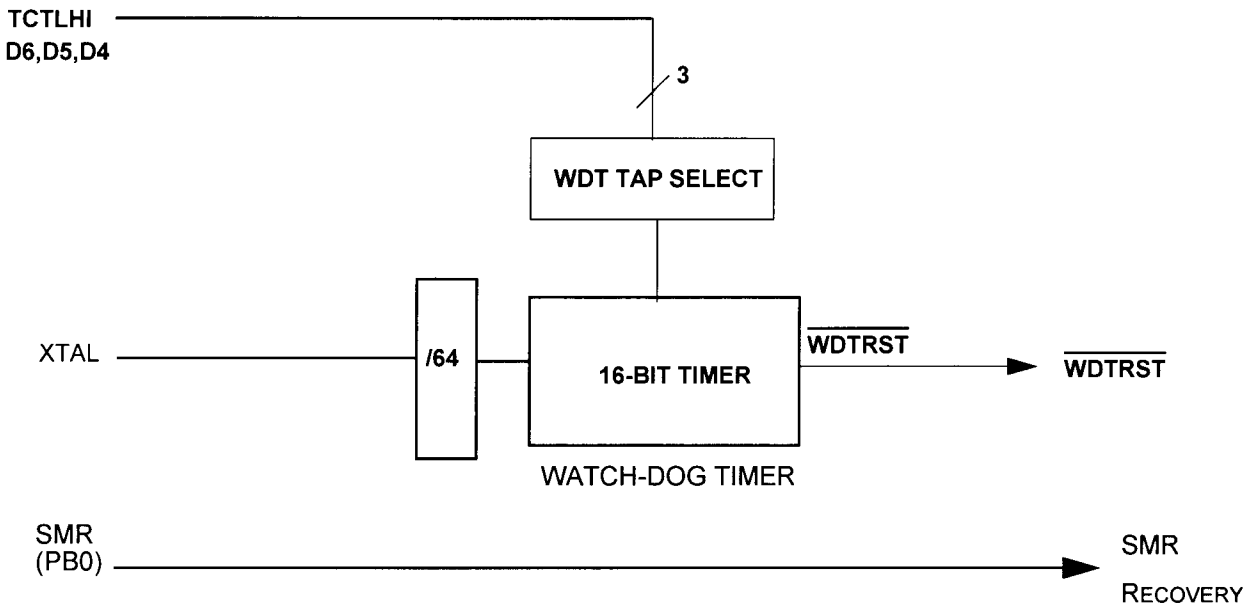


Figure 11. Z8E000 Reset Circuitry with WDT and SMR

STOP MODE OPERATION

The STOP Mode provides the lowest possible device stand-by current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP Mode, the Z8E000 only requires a STOP instruction. It is NOT necessary to execute a NOP instruction immediately before the STOP instruction.

```
6F    STOP    ;enter STOP Mode
```

The STOP Mode is exited by any one of the following resets: $\overline{\text{RESET}}$ pin or a STOP-Mode Recovery source. Upon reset generation, the processor will always restart the application program at address 0020H, thereby setting the STOP Mode Flag. Reading the STOP-Mode flag does not clear it. The user must clear the STOP-Mode flag with software.

Note: Failure to clear the STOP-Mode flag can result in undefined behavior.

The Z8E000 provides a dedicated STOP Mode Recovery (SMR) circuit. In this case, a low level applied to input pin PB0 will trigger a SMR. To use this mode, pin PB0 (I/O Port B, bit 0) must be configured as an input before the STOP Mode is entered. The low level on PB0 must be held for a minimum pulse width T_{WSM}, in addition to any oscillator startup time. Program execution starts at address 0020H after PBO is raised back to a high level.

Notes: Use of the PB0 input for the STOP mode recovery does not initialize the control registers.

The STOP Mode current (I_{CC2}) will be minimized when:

- V_{CC} is at the low end of the device's operating range.
- Output current sourcing is minimized.
- All inputs (digital and analog) are at the Low or High rail voltages.

CLOCK

The Z8E000 MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, a divide-by-two shaping circuit, a divide-by-four shaping circuit, and a divide-by-eight shaping circuit. Figure 13 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

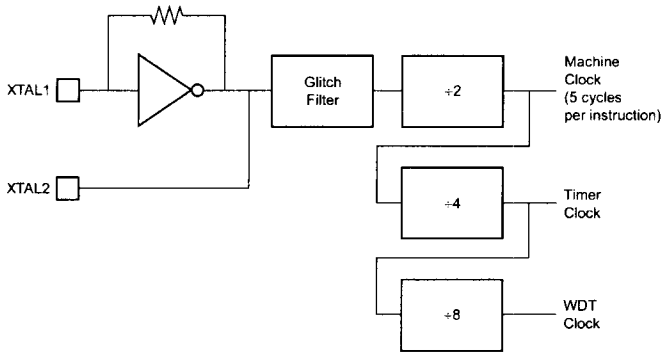


Figure 13. Z8E000 Clock Circuit

LC OSCILLATOR

The Z8E000 oscillator can use a LC network to generate a XTAL clock (Figure 18).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics and C_T is the total series capacitance including the parasitics.

Simple series capacitance is calculated using the following equation:

$1/C_T$	$= 1/C_1 + 1/C_2$
If C_1	$= C_2$
$1/C_T$	$= 2\ C_1$
C_1	$= 2\ C_T$

A sample calculation of capacitance C_1 and C_2 for 5.83-MHz frequency and inductance value of 27 uH is illustrated as follows:

$$5.83\ (10\text{^}6) = \frac{1}{2\pi\ [2.7\ (10^{-6})\ C_T]\ 1/2}$$

$$C_T = 27.6\ \text{pf}$$

Thus C_1 = 55.2 pf and C_2 = 55.2 pf.

TIMERS

Two 8-bit timers (T2 and T3), are provided but can only operate in cascade to function as a 16-bit standard timer (Figure 19).

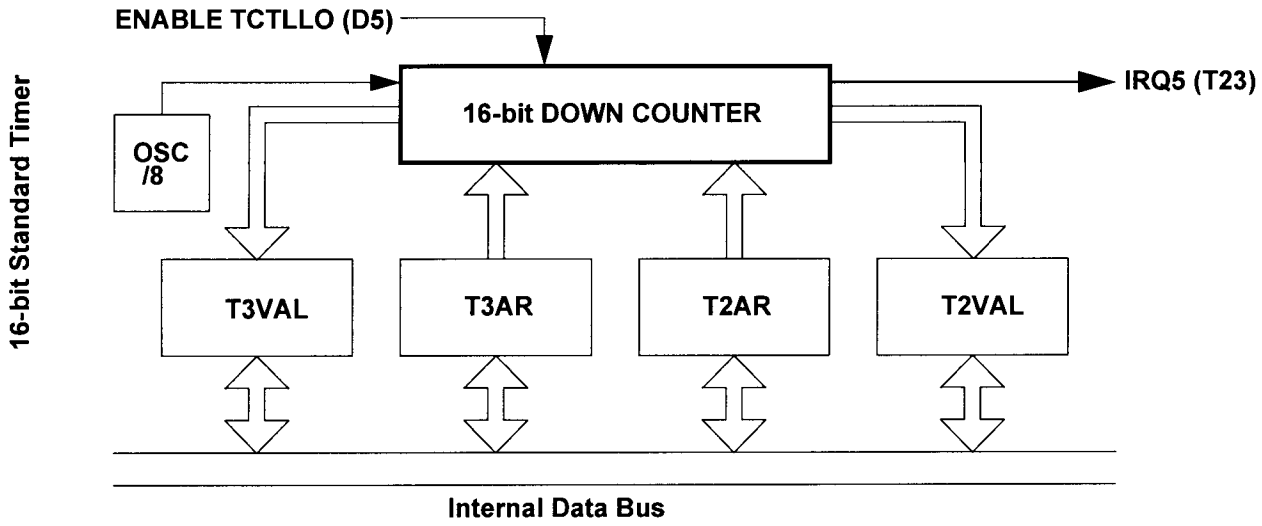


Figure 19. Timer Block Diagram

RESET CONDITIONS

After a hardware $\overline{\text{RESET}}$, the timers are disabled. See Table 5 for timer control, value, and auto-initialization register status after $\overline{\text{RESET}}$.

I/O PORTS

The Z8E000 has 13 lines dedicated to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port that is bit-programmable as either inputs or outputs. Port B can be programmed to provide standard input/output or the following special functions: SMR input and external interrupt inputs.

All ports have push-pull CMOS outputs. In addition, the outputs of Port A, on a bit-wise basis, can be configured for open-drain operation. As such, the register values for "/" at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers. See Figure 21.

Directional Control and Special Function Registers

Each port on the Z8E000 has an associated and dedicated Directional Control Register that determines on a bit-wise basis whether a given port bit will operate as an input or as an output.

Each port on the Z8E000 has a Special Function Register that, in conjunction with the directional control register, implements on a bit-wise basis, and supports special functionality that can be defined for each particular port bit.

Input and Output Value Registers

Each port has an Output Value Register and an Input Value Register. For port bits configured as an input by means of the Directional Control Register, the Input Value Register for that bit position will contain the current synchronized input value.

REGISTER	ADDRESS	IDENTIFIER
Port B SPECIAL FUNCTION	0D7H	PTBSFR
Port B DIRECTIONAL CONTROL	0D6H	PTBDIR
Port B OUTPUT VALUE	0D5H	PTBOUT
Port B INPUT VALUE	0D4H	PTBIN
Port A SPECIAL FUNCTION	0D3H	PTASFR
Port A DIRECTIONAL CONTROL	0D2H	PTADIR
Port A OUTPUT VALUE	0D1H	PTAOUT
Port A INPUT VALUE	0D0H	PTAIN

Figure 21. Z8E000 I/O Ports Registers

For port bits configured as an output by means of the Directional Control Register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) will hold their previous value. They will not be changed by hardware nor will they have any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-wise basis. All bits are capable of operating as inputs or outputs, depending upon the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, while the output of the synchronizer is fed to the port input register, which can be read by software.

A write to a port input register has the effect of updating the contents of the input register, but subsequent reads will not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position will contain the current synchronized input value. Thus, writes to that bit position will be overwritten on the next clock cycle with the newly sampled input data. However, if the particular port bit is programmed as an output, the input register for that bit will retain the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. If such is the case, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The above result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software read will return the *required* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input will be disabled to save power.

Updates to the output register will take effect based upon the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and will return the current output value that is held. No restrictions are placed on the timing of reads and/or writes to any of the port registers with respect to the others, but care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register should first be disabled. If this precaution is not taken, spurious events could take place as a result of the change in port I/O status. This precaution is especially important when defining changes in Port B, as the spurious event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, and setting the SFR register should be the final step in the port configuration process. To ensure deterministic behavior, the SFR register should not be written until the pins are being driven appropriately and all initialization has been completed.

PORT A

Port A is a general-purpose port (Figure 23). Each of its lines can be independently programmed as input or output via the Port A Directional Control Register (PTADIR at 0D2H) as seen in Figure 22. A bit set to a "1" in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to "0" configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open drain by setting the corresponding bit in the Special Function Register (PTASFR, Figure 27.)

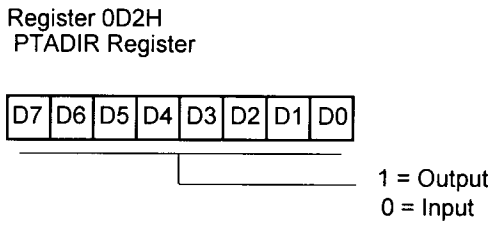


Figure 22. Port A Directional Control Register

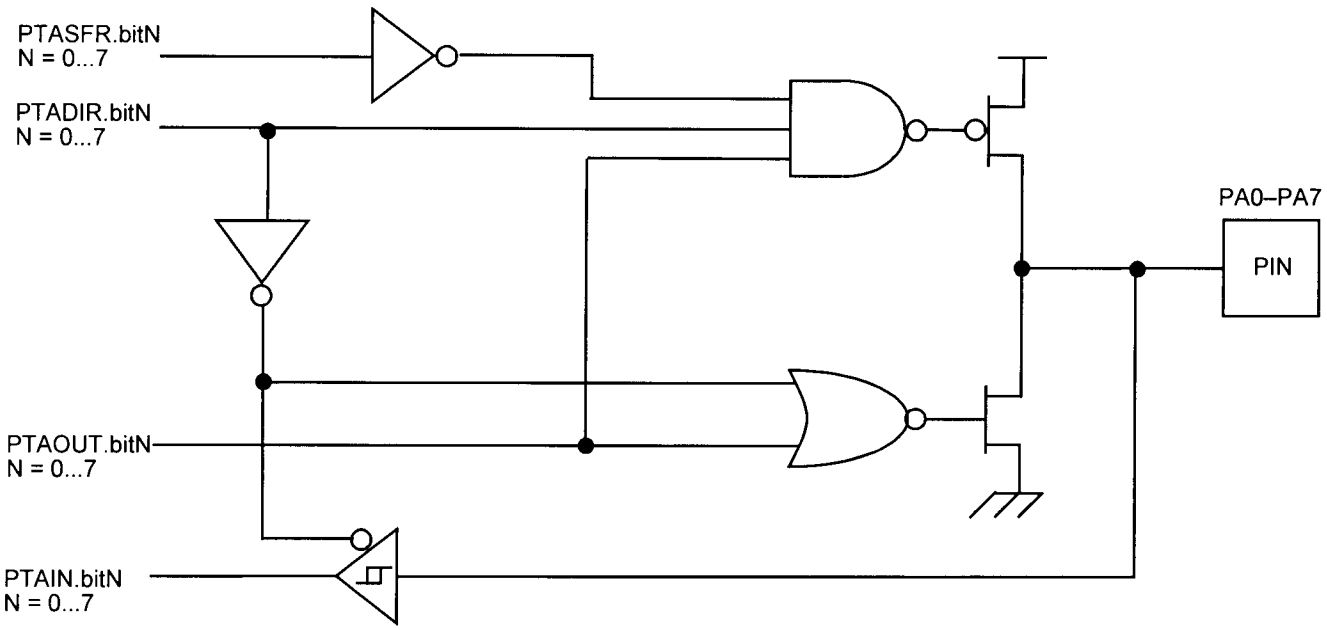


Figure 23. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

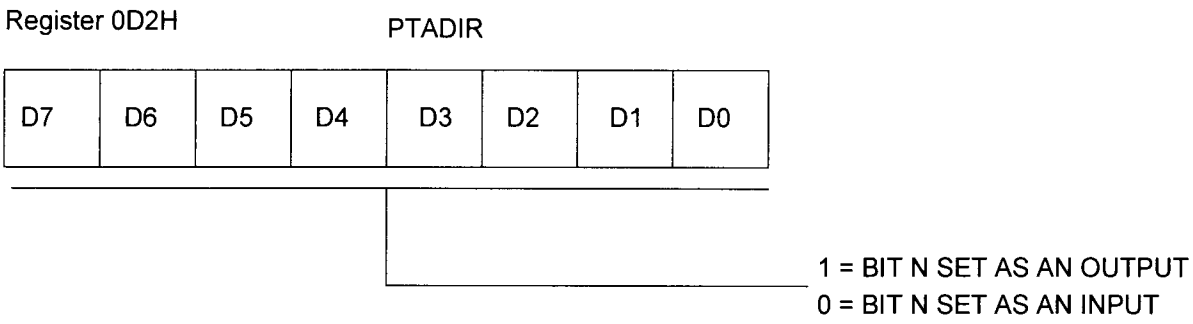


Figure 26. Port A Directional Control Register

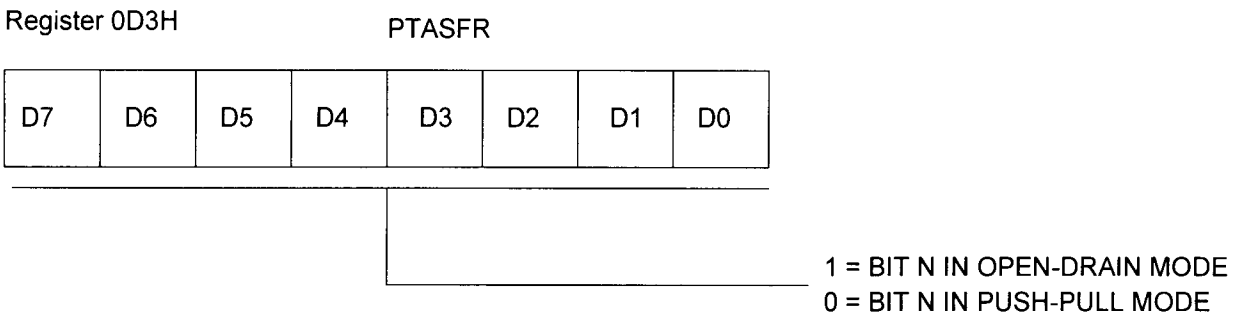


Figure 27. Port A Special Function Register

PORT B

Port B Description

Port B is a 5-bit, bidirectional, CMOS-compatible I/O port. These five I/O lines can be configured under software control to be an input or output, independently. Input buffers are Schmitt-triggered. See Figure 29 through Figure 33 for diagrams of all five Port B pins.

In addition to standard input/output capability on all five pins of Port B, each pin provides special functionality as indicated in Table 8:

Table 8. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	None
PB2	IRQ3	None
PB3	None	None
PB4	IRQ1/IRQ4	None

Special functionality is invoked via the Port B Special Function Register. See Figure 28 for the arrangement and control conventions for this register.

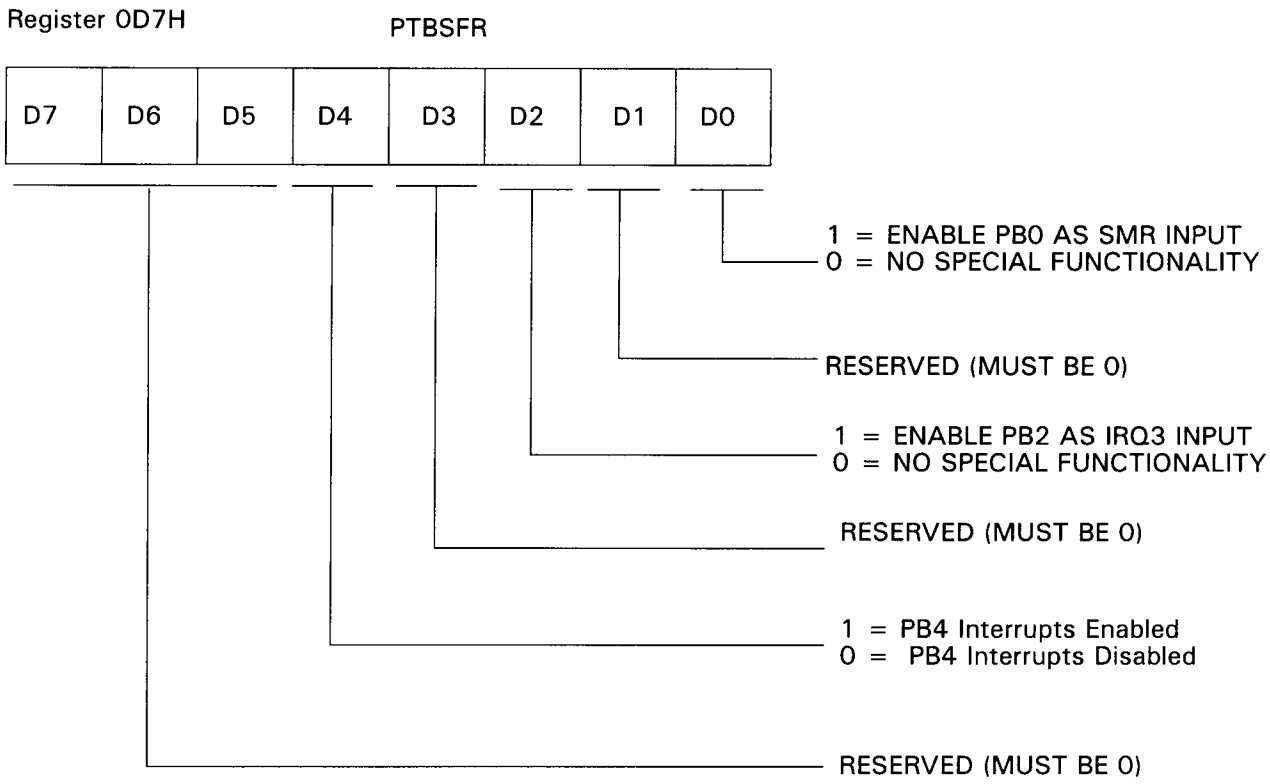


Figure 28. Port B Special Function Register

PORT B—PIN 2 CONFIGURATION

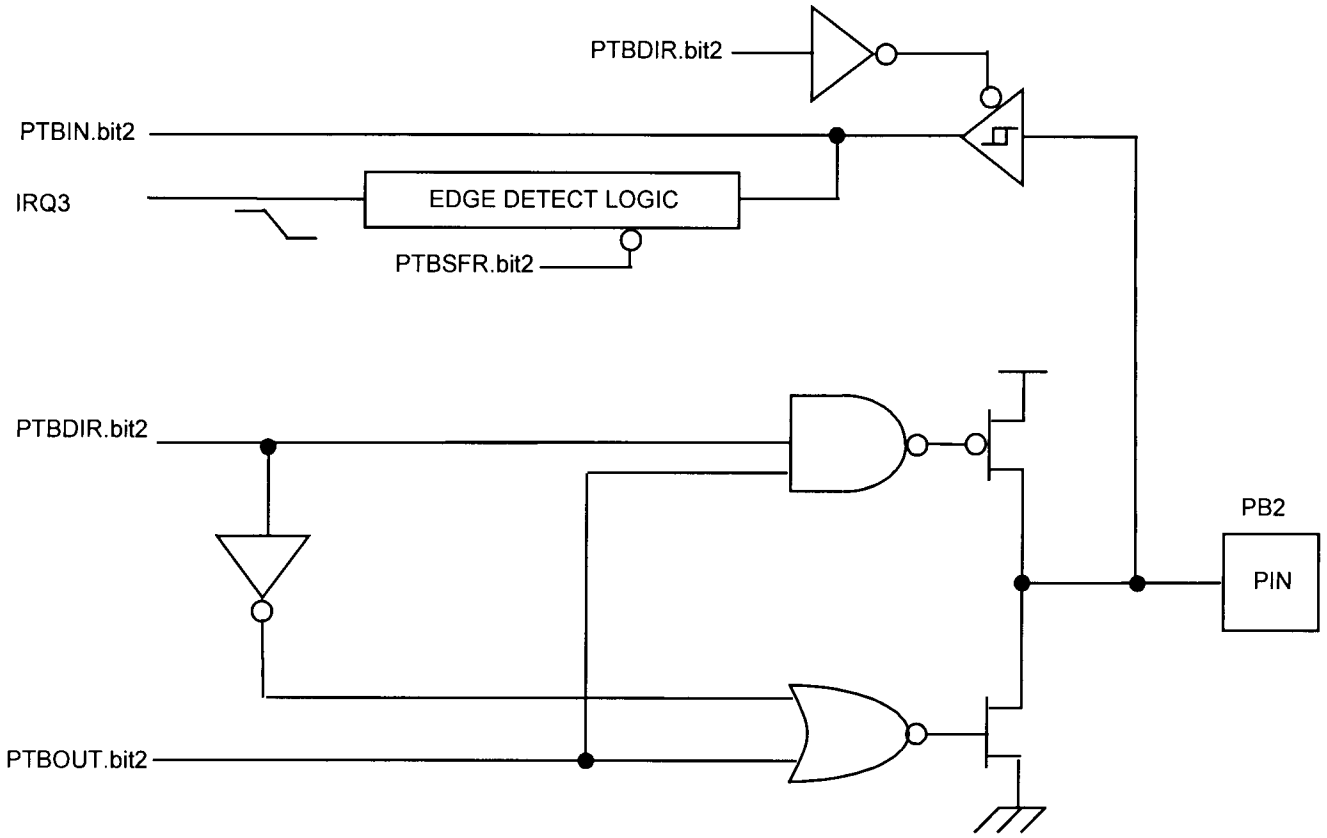


Figure 31. Port B Pin 2 Diagram

PORT B—PINS 3 AND 4 CONFIGURATION

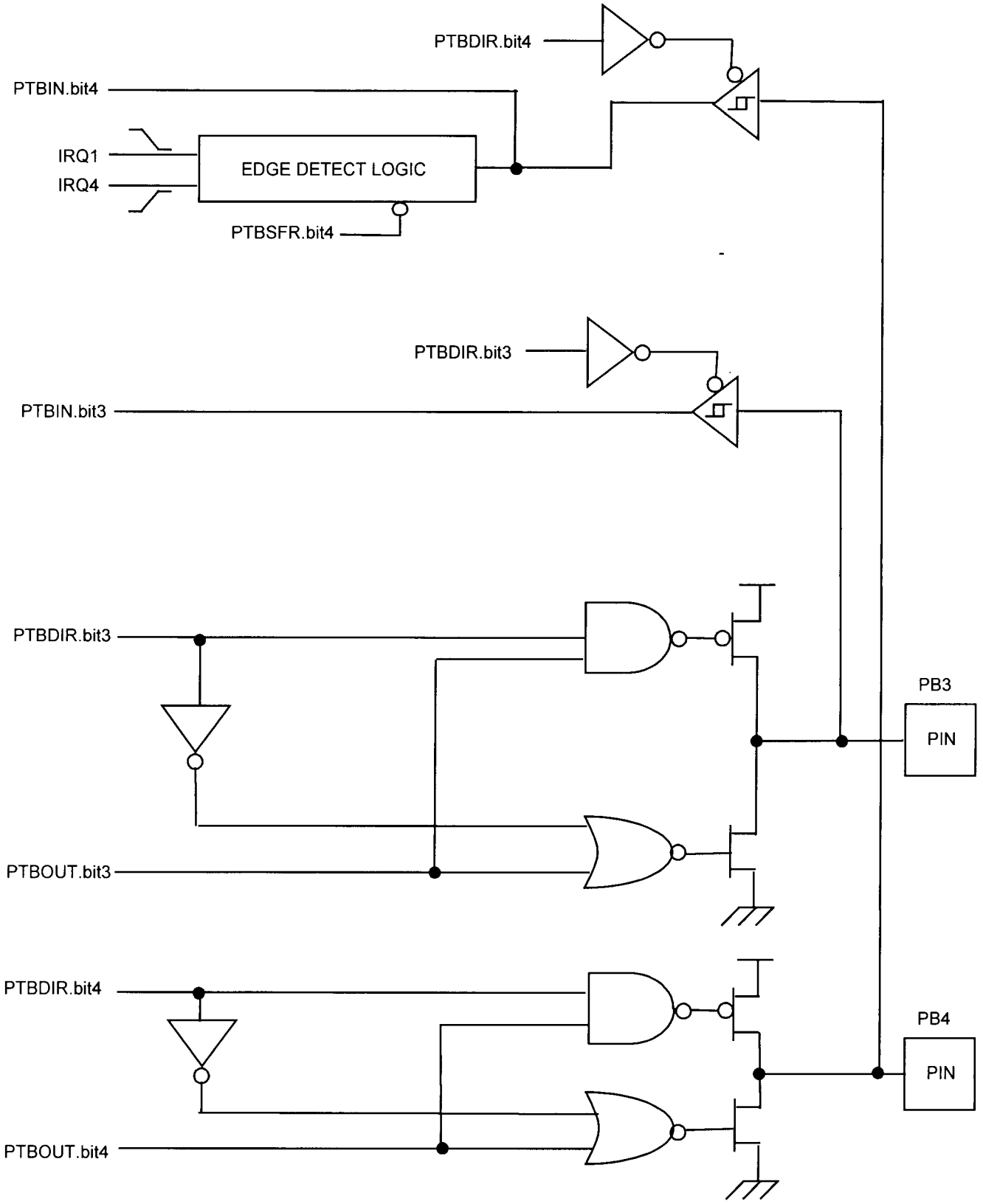


Figure 32. Port B Pins 3 and 4 Diagram

ORDERING INFORMATION

Standard Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PSC	Z8E00010SSC	Z8E00010HSC

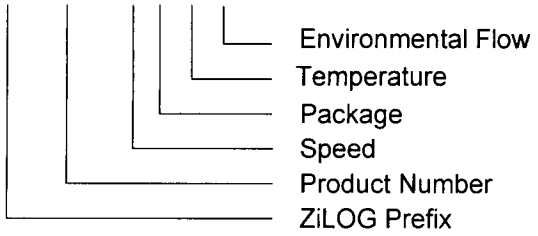
Extended Temperature		
18-Pin DIP	**18-Pin SOIC**	**20-Pin SSOP**
Z8E00010PEC	Z8E00010SEC	Z8E00010HEC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part(s) required.

Codes	
Preferred Package	P = Plastic DIP
Longer Lead Time	S = SOIC
	H = SSOP
Preferred Temperature	S = 0°C to +70°C
	E = –40°C to +105°C
Speed	10 = 10 MHz
Environmental	C = Plastic Standard

Example:

Z 8E000 10 P S C is a Z86E000, 10 MHz, DIP, 0° to +70°C, Plastic Standard Flow



Pre-Characterization Product:

The product represented by this data sheet is newly introduced and ZiLOG has not completed the full characterization of the product. The data sheet states what ZiLOG knows about this product at this time, but additional features or nonconformance with some aspects of the data sheet may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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